A 58-μW Sensor Node LSI with Synchronous MAC Protocol

Department of Computer and Systems Engineering, Kobe University
1-1, Rokkodai, Nada, Kobe, 657-8501 Japan
E-mail: shin@cs28.cs.kobe-u.ac.jp

Abstract
To shorten the preamble time and save the needless energy, we propose the isochronous media access control (I-MAC) [1], and implement it on a sensor node system LSI with a power management mechanism. Fig. 1 shows the block diagram of the proposed sensor node that includes a transceiver (TX/RX), microcontroller, and power management module (PMM). The state transition of the I-MAC can be simplified because all nodes are synchronized and predict their operations. Hence, a simple processor for the I-MAC can be implemented as dedicated hardware. As well, the PMM controls the power supplies of the components, based on the state transition of the I-MAC. The PMM is operated at 32.768 kHz and counts up the internal time. In a sleep state, only the PMM is activated. In our system, i8051 deals with only upper layers than the MAC layer.

The TX is comprised of a PLL and power amplifier (PA). We propose a higher-efficiency PA using an oscillator with multi-phase outputs. The multi-phase oscillator has four five-stage ring oscillators, connected by interpolators; 20-phase square waves are output at every 18 degrees. The PA has ten phase-modulated class-D amplifiers in parallel. Each class-D amplifier is controlled by other phases, which reduces short current through the PA in an active mode. The maximum power efficiency achieves 17.9 % at 1.45 dBm without any MEMS or inductors.

In the RX part, we adopted a low-IF architecture. The I/Q mixer also exploits the multi phases for I/Q separation. A complex band-pass delta-sigma ADC converts the I/Q signals to quantized signals. Then, a digital image rejection filter selects a desired bandwidth. The image signal rejection is digitally-assisted without analog circuits. The image rejection ratio is 60 dB. As the final stage of the RX, the baseband DSP demodulates FSK. The RX achieves a bit error rate below 10^{-5} at a data rate of 60 kbps and at an SNR of 7.8 dB.

The test chip was fabricated in a 180-nm CMOS process and the area is 3 x 3 mm². The power of each component is shown in Fig. 3. We verified the average energy in data-gathering operation on a network level using network simulator. In the network simulation, the wake-up period is 100 ms, and the data rate is 20 kbps. Randomly-deployed 100 nodes in the area of 100 x 100 m² collect data to a base station at the center. The wake-up ratio is 0.28%, and the proposed sensor node processor achieves a power of 58.0 μW on average.

References