A Single-Chip Sensor Node LSI with Synchronous MAC Protocol and Divided Data-Buffer SRAM

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Abstract — This paper presents an ultra-low-power single-chip sensor-node VLSI with a synchronous MAC protocol and divided data-buffer SRAM for wireless-sensor-network applications. One of the most challenging issues in wireless sensor networks is extension of the overall network lifetime. So a communication centric design approach has been introduced to reduce the power consumption of the RF circuits and the entire sensor network system, through a vertical cooperative design among circuits, architecture, and communication protocols. A transceiver, i8051 microcontroller, and dedicated MAC processor with divided SRAM are integrated in a single chip. The test chip occupies 3.0 x 1.7 mm² in a 180-nm CMOS process, including 0.63 M transistors. Divided data-buffer reduces 18.6% of average power and the LSI consumes 6.34 μW under a network environment.

Index Terms — Cross-layer design, sensor network, sensor node, MAC protocol, time synchronization, low power

I. INTRODUCTION

Recent advances in micro-sensors, integrated circuits, and wireless communication technologies realize wireless sensor networks (WSNs). Applications of sensor networks comprising numerous such sensor nodes include remote environmental monitoring, smart spaces, military surveillance, and precision agriculture.

A WSN consists of many wireless sensor nodes, each of which is driven by a small battery. The sensor nodes obtain environmental information and send it to a base station with a multi-hopping scheme, under the severe energy constraint. As the number of sensor nodes increases to hundreds or to thousands, the persistent necessity of changing batteries would be a considerable burden. For that reason, the most important issues on the WSNs are to extend an available period, say, network lifetime as long as possible. On the other words, it is highly desirable to reduce the power being used by each sensor node. Another issue is low cost realization of the WSNs. Thus a single chip implementation of the sensor node is also necessary.

According to Moore’s law, a power of digital portions is scaled down with the progress of process technology. On the other hand, the power consumption of analog RF circuits will not scale at the same rate. In the entire system of the sensor networks, the power consumption of the RF circuits depends on the amount of its communications. Thus, the communication centric design is strongly requested to reduce the power consumption of the RF circuits.

So a sensor node should be operated at a low duty cycle (less than 1%, [1]) to reduce the dynamic RF power consumption, which results in the increase in sleeping time. In the sleep period, sensor nodes have to hold the routing information and observed data from sensor, for instance. Therefore, it is also important to reduce a leakage power of buffer SRAM during the sleep period.

In this paper, we propose an ultralow-power sensor node processor using an Isochronous-MAC (I-MAC) protocol [2] and a divided data-buffer SRAM architecture, which reduces both the dynamic power during the operating period and the leakage power during the sleep period.

The rest of this paper is organized as follows: The communication protocol and its implementation are explained in Sect. II. The architecture of proposed data-buffer SRAM is addressed in Sect. III. Section IV and V describe VLSI implementation and experimental results. These are followed by conclusion in Sect. VI.

II. COMMUNICATION CENTRIC DESIGN

To achieve communication centric design, the cross layer design between the hardware (node processor architecture) and the algorithm (communication protocol) is indispensable. In this work, we focus on MAC protocol which is a communication protocol of the data link layer. While a node communicates, MAC protocol is always executed since the function of MAC protocol is establishing communication links for data transfer. The active time of the RF circuit mainly depends on the MAC protocol.

Here, we introduced an Isochronous-MAC (I-MAC) protocol [2], which has a periodic wakeup time synchronized with the Flooding Time Synchronization
Protocol (FTSP). I-MAC reduces the active time of the RF circuits significantly resulting low power characteristics.

A. Isochronous-MAC (I-MAC)

An effective way to reduce the energy in MAC is shorten the idle listening, in which the receiver is activated even when no packet is received. To reduce the power of this idle listening, a type of MAC named Cycled Receiver MAC, which includes S-MAC [3], Low Power Listening (LPL) [4] and WiseMAC [5], has been developed. Using Cycled Receiver MAC, each node enters a receiving mode only during a specific wakeup duration time that occurs in every wakeup period. Reducing the duty cycle ratio, the power used for idle listening is also decreasing. In general, with a cycled receiver MAC, the longer the wakeup period, the longer the delay time for connection establishment. Therefore, under the condition of the same duty cycle ratio, the shorter wakeup period, the more advantageous it can be in terms of the delayed time.

The proposed Isochronous-MAC (I-MAC) [2][6] is based on LPL that has a periodic wakeup time. Since a sender can predicts a next wakeup time of an intended receiver with high accuracy, we can minimize the duration of a preamble on the sender. As well as on the receiver side, the receiving time for the preamble can be reduced thanks to the short duration of the preamble.

B. Time synchronization

In [2][6], the time on sensor nodes are adjusted to the actual time using the long-wave standard time code. However, external hardware is required for this method, and it does not work indoors.

In contrast, packet exchanging methods do not require external hardware or signal, although a communication overhead is required. Flooding Time Synchronization Protocol (FTSP) [9] is one of the packet exchanging method and it correct the time by using time stamp packet communication. As the time synchronous technique of the proposal sensor node, we chose FTSP in consideration of the cost of hardware and power overhead.

Figure 2 shows the synchronization method of the FTSP algorithm. First, the synchronous packet is flooding from the root node. At this time, the time stamp of T1 is send to the receiver node. Next, the receiver node records the time stamp of T2 at the end of the synchronous packet. Then the propagation delay is calculated from T2 - T1. However, note that, until the synchronous packet is recognized by a system, there is a time of Tb as a byte alignment time. This can be calculated by the data rate, and after that, the time error is corrected with T2 - T1 - Tb in the receiver node. The time lag among sensor nodes is suppressed within 250 \( \mu \) seconds, when the nodes synchronize 50 times, in a day. From [2], time lag of 250 \( \mu \) seconds is sufficiently small value in order to operate I-MAC.

In addition to the above, there are two other reasons why we chose the FTSP for our system. The first reason is that the I-MAC does not need to synchronize the time of the entire network. Only by synchronizing the time between a node and its one-hop
neighbor, the I-MAC can organize communication. Moreover, although the power consumption of the I-MAC is dependent on a preamble length, its length can be determined only by the time drift over a one-hop neighbor [2][6].

The second reason is that we assume data collection type application in this research. In order to collect sensing data, it is necessary to construct routes from a base station to each node in the network. In many routing protocols, the route is constructed by using flooding. (e.g. Directed Diffusion [10] and Tiny Diffusion [11]). Therefore, since the time synchronization by using FTSP and the construction of a route can be executed simultaneously, the flooding operation does not become overhead.

III. DIVIDED DATA-BUFFER SRAM

Conventional sensor nodes primarily use either SRAM or flash memory for data storage. Both types of memory have their advantages and disadvantages. SRAM, for example, is easily implemented as one chip, it has low cost, and its active power consumption is small. However, SRAM must be continually driven to retain data, and, as a result, its leak current is significant.

Flash memory, in contrast, consumes no leak current while the sensor node is sleeping, but the cost of making a one-chip sensor node with flash memory is higher than that with SRAM. In addition, the active power consumption of flash memory is high, and it cannot provide high-speed memory access. Moreover, flash memory has a finite number of erase-write cycles which does not suit its application to the packet buffer, which must be written and read many times. Therefore, this paper considers an energy-efficient SRAM architecture that can be implemented in a one-chip sensor node at low cost.

To reduce the leakage power in the sleep period, we propose divided data-buffer SRAM, which is based on that leak current of SRAM increases in proportion to SRAM capacity. Figure 3 shows the architecture of divided data-buffer SRAM. Here, we assume 64 kbits of memory capacity. The data-buffer SRAM is divided by same ratio, and memory controller manages the power gating for each memory block. Memory controller extracts the data size from a header of received data and it provides a proper combination of memory block with “power on” signal, which minimizes leakage current in SRAM portion. The memory controller is activated only when the memory is accessed; therefore, the power overhead of the memory controller is quite small.

Fig. 3 Data-buffer SRAM divided with equal ratio manner

IV. IMPLEMENTATION

In the conventional sensor nodes [12][13][14], all of the communication protocol (e.g. MAC layer, network layer, and application layer) is processed by micro controller (Fig. 4 (a)). Particularly, the micro controller is dealing with the process of the MAC layer in most of the time, because the sensor networks usually employ a simple transmission method and a lower data rate to reduce power consumption of the RF circuits. Hence the processing power during data communication becomes relatively high.

To overcome the above problem, we propose a communication control processor which consists of a MAC processor, i8051 microcontroller, and data memory (Fig. 4 (b)). The MAC processor is a dedicated hardware for the communication processing in the I-MAC. Then i8051 deals with only upper layers than the MAC layer (e.g. time synchronization, rooting, and sensor input).
The overall block diagram of the sensor node LSI is shown in Fig. 5. The proposed sensor node has a power management module which controls the power gating for each function blocks, based on the state transition of MAC processor. The state of the power supply in each functional block depends on the state transition of I-MAC. For this reason, the sequencer specified for power supply management has been designed so that efficient power supply management can be realized.

The power management module consists of a clock manager, timer, and MAC state register. The state of the MAC processor is stored in the MAC-state register. According to this state register, a clock and a power supply of each block are cut off. The timer is operated at 32.768 kHz and counts up the internal time. In the sleep state, only the timer is activated. By receiving an interrupt signal from the timer, the node moves to the RX state.

A 433MHz RF transceiver [15] is also implemented in the same chip. The transceiver is comprised of transmitter (TX), receiver (RX), and TX/RX switch. The RX is based on a low-IF architecture and it contains an image rejection filter.

Figure 6 shows the chip photomicrograph. The VLSI is comprised of a transceiver (TX, RX, PLL), 8051 micro controller, power management module, dedicated MAC processor, and divided data-buffer SRAM for data storage. The test chip was fabricated in a 180-nm CMOS process and the area is 3.0 x 1.7 mm².

The overall block diagram of the sensor node LSI is shown in Fig. 5. The proposed sensor node has a power management module which controls the power gating for each function blocks, based on the state transition of MAC processor. The state of the power supply in each functional block depends on the state transition of I-MAC. For this reason, the sequencer specified for power supply management has been designed so that efficient power supply management can be realized.

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V. EXPERIMENTAL RESULT

Figure 7 shows a leakage power of divided data-buffer SRAM. The leak current during static data-hold period is linearly increases as memory capacity increases. According to the memory block size, the leakage power is varied from 1.29μW to 2.73μW. Table 1 summarizes the power consumption of each functional block and total power for every operating mode. The power of each functional block is measured value and the total power in each state is also summarized.

We evaluated the average energy in data-gathering operation on a network level using network simulator: QualNet [16]. In the network simulation, the wake-up period is 100 ms, and the data rate is 20 kbps. Randomly-deployed 100 nodes in the area of 100 x 100 m² send data to a base station at the center. The interval of data gathering is 60 minutes; means 24 times per day. The operation of a sensor node assumed on this network simulation is illustrated in Fig. 8. Sensor nodes are sleeping at most of the data gathering period by I-MAC.
protocol. In our previous work [15], the average power during data gathering time was 58.0μW. This time, the average power during data gathering time is reduced to 44.2μW using divided-data buffer SRAM.

Fig. 7 Leakage power of divided data-buffer SRAM

Table 1. Power consumption of each functional block and total power for every operating mode

<table>
<thead>
<tr>
<th>Block name</th>
<th>Block power</th>
<th>State of a sensor node</th>
<th>Dynamic [μW]</th>
<th>Leakage [μW]</th>
<th>Sleep</th>
<th>Transmitting</th>
<th>Receiving</th>
<th>Network processing</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>4264</td>
<td>OFF</td>
<td>-</td>
<td>OFF</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>RX</td>
<td>7214</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>PLL</td>
<td>1395</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>MAC Processor</td>
<td>11.7</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Memory controller</td>
<td>14.4</td>
<td>OFF</td>
<td>83.2</td>
<td>ch gating</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>Data RAM (proposed)</td>
<td>285</td>
<td>OFF</td>
<td>1287 to 2752</td>
<td>ch gating</td>
<td>ON</td>
<td>Off</td>
<td>Off</td>
<td>ON [sec]</td>
</tr>
<tr>
<td>write</td>
<td>285</td>
<td>OFF</td>
<td>1287 to 2752</td>
<td>ch gating</td>
<td>ON</td>
<td>Off</td>
<td>Off</td>
<td>ON [sec]</td>
</tr>
<tr>
<td>ISR</td>
<td>737</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>On</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Power management</td>
<td>4.52</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Power management (operating with 12.768MHz crystal)</td>
<td>6.485</td>
<td>OFF</td>
<td>OFF</td>
<td>Off</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>Total power</td>
<td>-</td>
<td>-</td>
<td>1.46μJ/sec</td>
<td>6.34μJ/sec</td>
<td>10.73mW</td>
<td>13.65mW</td>
<td>3.87mW</td>
<td></td>
</tr>
</tbody>
</table>

The average operation time of each component in a day is shown in Table 2. It is estimated that the sensor node operates at 7.79μW of one-day average power supposing the normal SRAM buffer. A comparison of the average power between normal SRAM and divided data-buffer SRAM is shown in Fig. 9. Divided SRAM can reduce the average power of 18.6%, which realizes 6.34μW of one-day average power.

Table 2. Average operation time of sensor nodes in a day.

<table>
<thead>
<tr>
<th>Gathering interval [min.]</th>
<th>Gathering times per day</th>
<th>TX active time [sec.]</th>
<th>RX active time [sec.]</th>
<th>Network processing time [sec.]</th>
<th>Sleep time [sec.]</th>
<th>Average power with divided SRAM [μW]</th>
<th>Average power with normal SRAM [μW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>24</td>
<td>0.54</td>
<td>5.12</td>
<td>0.11</td>
<td>68394.22</td>
<td>6.34</td>
<td>7.79</td>
</tr>
</tbody>
</table>

Fig. 8 Operation of sensor node on network.

Fig. 9 Comparison of the average power between normal SRAM and divided data-buffer SRAM.

Figure 10 shows the effect of the power reduction by the divided data-buffer which depends on the number of data gathering times per day. The average power in a day is also indicated in Fig.10. This result shows, the reduction ratio of leakage power is decreased when the number of data gathering time per day is increasing. It is because sleep time is decreasing. Therefore, this divided data-buffer SRAM architecture is suitable for the application which gathers the data less frequently.
This architecture is useful for long gathering interval of average power is reduced by divided data-buffer SRAM. Moreover, divided data-buffer SRAM architecture makes up long sleep time. Power management module per day.

We propose a single chip sensor node processor with communication centric design. The sensor node is comprised of a transceiver, 8051 micro controller, power management module, dedicated MAC processor, and divided data-buffer SRAM. The test chip occupies 3 x 3 mm² in a 180-nm CMOS process, including 0.63 M transistors. The sensor node LSI operates at 6.34 μW of one-day average power, supposing 24 of gathering times per day.

I-MAC and FTSP reduce the operation time of RF, and make up long sleep time. Power management module reflects I-MAC state transition and decrease the active power. Moreover, divided data-buffer SRAM architecture reduces the power of sleep state. It is estimated that 18.6% of average power is reduced by divided data-buffer SRAM. This architecture is useful for long gathering interval applications.

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