Low-Power Low-Leakage FPGA Design Using Zigzag Power Gating, Dual-VTH/VDD and Micro-VDD-Hopping

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1. Introduction

In the 90-nm era and beyond, the number of transistors on a chip outnumbers one billion and the development cost and time have been increasing rapidly. One solution for this problem is to use a reconfigurable LSI such as an FPGA (field programmable gate arrays), which is attractive because of their inherently low non-recurring engineering (NRE) cost and short time-to-market [1]. Since an FPGA uses more transistors per function than SoC (system-on-a-chip) to achieve programmability, power consumption, especially the leakage power of an FPGA is larger than that of an SoC. These days, one CLB (configurable logic block) shows a dynamic power of 2.3 μW/MHz [2]. Since an FPGA chip is supposed to have 10⁵ CLBs in a 90-nm CMOS technology, a dynamic power of 40 W is consumed at 200 MHz. Almost same amount of leakage power will be added to the dynamic power.

So far, most of studies about an FPGA have mainly focused on area and performance; and there have been little works carried out for reducing power of an FPGA. In [3], [4], dynamic power is considered assuming that the leakage power is small, which does not hold any more. Recently, there have been some works on leakage power [5]–[7], [9]. In [5], leakage power of a 90-nm FPGA is analyzed. It is shown that leakage power of a circuit depends on its inputs; for example of a 2-input multiplexer in an FPGA, leakage power varies by more than 4X depending on the values of its inputs. In [6], some low-leakage design techniques for an FPGA are evaluated; and the gate biasing, use of redundant SRAM cells, and integration of multi threshold-voltage technology reduce leakage current from 2X to 4X compared to implementation without any leakage reduction technique. In [7], [8], dual-VDD schemes are applied to FPGAs and CAD algorithms for them are described. The other work proposed a method to reduce an active leakage current by 25% on average [9].

On the other hand, there have been extensive studies on low dynamic and leakage power design techniques for an SoC such as VDD hopping [10], SCCMOS (super-cutoff CMOS) [11] and MTCMOS (multi-threshold CMOS) [12]. A trend for low-power design is to apply an adaptive control of VDD/VTH spatially and temporally in finer granularity. In this paper, integrated low-power architecture is proposed and implemented for an FPGA, which fully utilizes the fine-grain assignment of VDD/VTH in time and space domains.

In VDD hopping, supply voltage is changed adaptively just to a required speed. It is demonstrated that VDD hopping can reduce power consumption by more than 75% if a required speed is a half of the maximum speed on average. The VDD hopping method was applied to a chip level but in order to improve a save factor, it is necessary to adopt a block-level method. In this paper, a micro-VDD-hopping scheme is proposed for an FPGA.

The SCCMOS and MTCMOS can effectively cut off leakage current in a standby mode but they suffer from a long wake-up time, which is a time to recover from a standby mode to an active mode. Alternatively, the Zigzag power-gating scheme [13]–[16] can reduce the wake-up time to less than 1/5 of a clock cycle, which can be used as a substitute technique for clock gating since clock gating loses its merit in the leakage-dominant era. In other words, the Zigzag power-gating scheme can reduce an active leakage thanks to the quick wake-up. The zigzag CMOS scheme is successfully applied for an FPGA for the first time to reduce leakage power. The main cave-at to apply the zigzag CMOS to the FPGA is a sneak path problem, whose countermeasure is also proposed in this paper.
2. Architecture

Figure 1 shows the architecture of the proposed FPGA. Four
CLBs are clustered into one VDD island where the same VDD
is used. VDD in the four CLBs is either VDDH (high VDD) or
VDDL (low VDD). Only two levels of VDD are used because
testing and characterization become easier. One more merit
of confining the number of levels to two is that switching be-
tWEEN the levels is quick. If there are more than two levels,
more number of VDD lines and VDD switches are required
and overhead is unacceptable. Even if DC-DC converters
were used to generate arbitrary VDDs, a transient time be-
tWEEN different VDDs would take more time. To a clustered
block comprised of four CLBs, VDDH is applied when high
performance is required. Alternatively, VDDL is applied if
the clustered block operates at a half speed.

The size of the clustered block in this architecture is
optimized by using simulations with a number of bench-
mark circuits. If the number of CLBs in a block decreases,
a finer control is possible but area and delay overhead in-
crease. Here, four is selected as a number of the CLBs in
order to keep the area and delay overhead below 5%. One
CLB includes four BLEs (basic logic elements) and five in-
puts, three outputs. One BLE consists of one LUT (Look-up
table), one D-FF and one 2-1 MUX. This configuration is
chosen because it is one of the best configurations for delay,
area and logic utilization [1].

Although two levels of VDD are allowed to each block
of logic, the signal swing of all inter-block interconnects is
set at VDDL. If two VDDs can be used for the interconnects
in a mixed way, the signal integrity issue will ruin the op-
eration. Since VDD of a block can be VDDH and the inter-
connect uses VDDL, a level shifter is one of the keys in this
architecture. In the next section, a novel level shifter is also
described in detail.

In the proposed FPGA, if the supply voltage in a clus-
tered block is VDDH, the clock frequency of the block is f.
On the other hand, the clock frequency should be reduced to
f/2 at a supply voltage of VDDL. Since the proposed
FPGA employs a Manhattan layout, an H-tree clock system
in Fig. 2 can be easily implemented.

To cope with the jitter and minimize skew between f
and f/2, only f is distributed with an H tree, and, f/2 is gen-
erated from f in each block as shown in Fig. 3. The figure
also points out that there might be two different phases of
f/2 without any constraint. However, a Reset signal syn-
chronizes frequencies of f/2 in all four CLBs, and prevent
this synchronization issue. Figure 4 illustrates a timing chart
of the clock frequencies and supply voltages in the block.
Thanks to the Reset signal, transients of the frequency and
supply voltages always starts from a rising edge f/2 and end
in a cycle of f/2. f/R keeps on VSS during the transient.

As shown in Fig. 5, since a modern FPGA usually has a
processor inside, it can be used to control voltages and fre-
frequencies. Thus in this paper, only the reconfigurable part
(the CLB arrays and their interconnects) as a prototype is
discussed. In the proposed FPGA, there are configuration
SRAM cells added for choosing supply voltages and fre-
frequencies as shown in Fig. 1 and Fig. 3. After receiving the
speed information from an application [10], a control pro-
cessor calculates time scheduling, and dynamically renews
the contents of the configuration SRAM cells.

![Fig. 1 Proposed FPGA. A configuration SRAM cell for power switches is denoted as SC.](image)

![Fig. 2 An H-tree clock system is adopted as clock distribution.](image)

![Fig. 3 Every clustered block, f/2 is generated from f. A configuration SRAM cell for selecting clock frequency is denoted as SC.](image)
3. Circuit Design

3.1 Power Gating in CLB

There are many SRAM cells in an FPGA, but they do not need to operate at high speed since they only drive local nodes statically. Thus, $V_{THH}$ (high $V_{TH}$) can be used for SRAM cells, and a leakage current is not an issue there. On the other hand, logic blocks consume much leakage power because they have to utilize $V_{THL}$ (low $V_{TH}$) to enhance speed. The leakage current in the logic blocks can be mitigated with the Zigzag power-gating scheme.

Figure 6 shows schematics of INVs and a 2NAND to which the Zigzag power-gating scheme is applied. Voltages on a virtual $V_{DD}$ and $V_{SS}$ lines are denoted as $V_{DDV}$ and $V_{SSV}$, respectively. In a standby mode, they are neither at $V_{DD}$ nor $V_{SS}$, but stay somewhere between $V_{DD}$ and $V_{SS}$ [13]–[15]. Thus a wake-up time is shorter than the other power-gating schemes. Even if $V_{OD}$ (overdrive voltage) is zero, the leakage current can be suppressed by an order of magnitude because of the off-off stacking structure incorporated in this scheme. Therefore, zero $V_{OD}$ is one choice.

For CMOS gates such as the INV and 2NAND, straight-forward application of the Zigzag CMOS is fine. However, if the Zigzag CMOS is straightly applied to the transmission gates in Fig. 7, a sneak leakage path [17] problem occurs. In an FPGA, the multiplexers that employ transmission gate are not only used in logic blocks but also switch blocks. Therefore, at interface of a CMOS gate and transmission gate, special care needs to be taken. As shown in Fig. 8, at a LUT in a BLE, small NORs with $V_{THH}$ are added to SRAM cells’ outputs in order to set all inputs of transmission gates to a same level. Thus, the sneak leakage path

![Fig. 4](image1.png) A timing chart of the clock frequencies and the supply voltages.

![Fig. 5](image2.png) An FPGA system including a processor.

![Fig. 6](image3.png) Zigzag power-gating scheme.

![Fig. 7](image4.png) Sneak leakage path.

![Fig. 8](image5.png) Schematic of the proposed LUT. Black-painted NORs employ $V_{THH}$. 

Figure 9 shows the proposed CLB with the sneak leakage path suppressed. At the outputs of the CLB, there are level keepers in case that a CLB is cut off. These keepers are made of minimum MOSFETs with $V_{THH}$ because they only have to keep states of the CLB outputs and do not need to operate fast. It is important to maintain the output states even in a standby mode since the outputs may be connected to another active CLB. The subsequent CLB malfunctions if the states changes during the standby mode.

3.2 Interconnect

In the proposed scheme, since a swing of inter-block interconnects is $V_{DDL}$, only NMOSFET is necessary for a switch block. Therefore, the structure of the switch block is simple, and the capacitance of the interconnection can be reduced, which leads to a smaller area and lower power than a $V_{DDH}$ case.

However, the $V_{DDL}$ swing would give rise to a signal integrity issue. In normal SoC design, if some interconnects use a low-voltage signal and others use a high-voltage swing, the high-swing aggressor induces a crosstalk noise larger than a logic threshold on the low-swing victim. This is inevitable since in the SoC design, high-swing and low-swing signals are laid out in a totally intermingled way. On the other hand, in a structured LSI such as an FPGA, interconnects are laid out in an orderly fashion, and low-swing inter-block interconnects can be bundled together. Thus, the signal integrity issue among inter-block interconnects can be solved. The only remaining source of the signal integrity issue is the coupling between intra-block and inter-block interconnects as shown in Fig. 10(a).

Figure 11(a) shows the proposed level shifter, namely a BELS (bypassing enabled level shifter). To the conventional shifter, two PMOSFET and three NMOSFET are added.

3.3 Level Shifter Design

In the micro-$V_{DD}$-hopping scheme, each clustered block is operated at either $V_{DDH}$ or $V_{DDL}$ as shown in Fig. 1. Because the inter-block interconnect uses $V_{DDL}$, level shifters are needed at the inputs of the CLB. The conventional level shifter in Fig. 11(a) has a large delay since it suffers from contention between the pull-down NMOSFETs (MN1 and MN2) and pull-up PMOSFETs (MP1 and MP2). The contention problem gives rise to the increase in both delay and power due to a large crowbar current.

Figure 11(b) shows the proposed level shifter, namely a BELS (bypassing enabled level shifter). To the conventional shifter, two PMOSFET and three NMOSFET are added. The BELS has two operation modes; “SHIFT” and “NON-SHIFT” modes. When the output voltage of the BELS is $V_{DDH}$, it is in the “SHIFT” mode. In the “SHIFT” mode, by setting the Bypass signal to $V_{DDL}$, the contention at node B will be reduced and the logic value of node B is established faster. Therefore, the delay is less than the case of Bypass signal being set to 0 V. When the $V_{DD}$ is low voltage, $V_{DDL}$, the shifting function is not required and the BELS is switched to “NON-SHIFT” mode. In the “NON-SHIFT” mode, a signal, EN, is set to $V_{DDH}$ in order to activate a bypass and cut some MOSFETs out of the $V_{DP}$ and $V_{GS}$ lines. Since a signal, Bypass, is set to $V_{DDH}$ in the “NON-SHIFT” mode, $MN_{Bypass}$ can pass the input signal to the output without threshold voltage loss (assuming $V_{DDH} > V_{DDL} + V_{THH}$).
level shifter and BELS. In the "SHIFT" mode, both level shifters have almost the same delay. In the "NON-SHIFT" mode, since the input signal is bypassed via MN_Bypass, the contention problem does not occur in the BELS. Thus, the delay of the BELS is improved. It is shown from Fig. 12 that the delay of the BELS is reduced by 46% of the conventional level shifter at VDDL of 0.5 V.

Figure 13 shows power simulation in both level shifters as well. In the "NON-SHIFT" mode, the power consumption of the BELS is reduced by 32%. There are two factors that save the power of the BELS. The first factor is that the contention problem is eliminated. The second one is that non-active MOSFETs are cut off, which results in reduction of dynamic charging and discharging current.

4. Simulation and Measurement Results

Both of the proposed and conventional FPGAs were manufactured using a 0.35-μm CMOS technology with a nominal supply voltage of 3.3 V in order to demonstrate how much the proposed approach can save power. Figure 14 is a chip microphotograph. The area overhead of the proposed FPGA is 2%. Figure 15 shows the measurement conditions. An eight-bit ripple-carry adder is implemented and input vectors for measurement are also shown in the figure. To measure delay, a ring oscillator is used. Figure 16 shows the measured power and delay characteristics of the proposed and conventional FPGAs. VDD in the conventional FPGA is kept at 3.3 V. As abovementioned, VDD of the clustered block is either VDDH or VDDL in the proposed FPGA. It should be noted that VDDL is changed from 1.8 V to 2.5 V. Power and delay of the conventional FPGA are also shown with the broken lines.

At VDDL of 1.8 V, the power of the proposed FPGA is reduced by 86% compared with that of the conventional FPGA. Therefore, if the required speed is a half of the maximum achievable speed, the power can be reduced by 86%.
Fig. 17  Leakage-power simulation in the proposed FPGA for 3 cases: $V_{DD} = V_{DDH}$, $V_{DD} = V_{DDL}$ and when the Zigzag power-gating is adopted. Leakage power in the conventional FPGA is also shown with the broken line.

Even when $V_{DD}$ in the clustered block supply is $V_{DDH}$ of 3.3 V, the power of the proposed FPGA is smaller than that of the conventional one by 10%, in that case the delay overhead then is only 3%. This power reduction comes from the reduced swing on the inter-block interconnects.

To compare leakage power of the proposed FPGA with that of the conventional FPGA, simulations using 90-nm CMOS technology with dual $V_{TH}$ ($V_{THL}$=0.22 V, $V_{THH}$=0.32 V) are carried out. The circuit used in the simulation has the same structure as the circuit fabricated using 0.35-$\mu$m CMOS technology. Only technology parameters are changed. The nominal supply voltage is 1.0 V. Figure 17 shows the simulated leakage power of the conventional and proposed FPGA. When the supply voltage of clustered block $V_{DD}$ is $V_{DDL}$, the leakage power of the proposed FPGA can be reduced by 70%. It is interesting that the leakage power is strongly dependent on $V_{DDL}$. This is due to the DIBL (drain induced barrier lowering) effect by which $V_{TH}$ of MOSFETs is reduced. If the zigzag power-gating scheme is also used, the leakage power of the proposed FPGA can be further reduced by 97% compared to that of the conventional FPGA.

Figure 18 shows the simulated waveform of $V_{DDV}$ and $V_{SSV}$ for the power-gating scheme. The wake-up time of the power-gating is 620 ps. If the clock frequency of FPGA is 500 MHz, the clustered block can be forced into an active mode within one clock cycle.

5. Conclusion

A low-power FPGA based on micro-$V_{DD}$-hopping was proposed. In the proposed FPGA, fine-grain $V_{DD}$ and clock frequency controls at a block level are integrated to provide a low-power solution for an FPGA. In addition, with the Zigzag power-gating scheme, the quick control in a time domain is possible as a substitution for clock gating. We showed that power in the proposed FPGA can be reduced by 86% of the conventional FPGA, when a required speed of the clustered block is a half of the maximum achievable speed. We also proposed a novel level shifter in order to make micro-$V_{DD}$-hopping more effective.

Simulation using a 90-nm CMOS technology shows that leakage power of the proposed FPGA is reduced by 70% of the conventional FPGA, when supply voltage $V_{DD}$ in the clustered block is $V_{DDL}$. If the Zigzag power-gating scheme is also used, leakage power can be further reduced by 97%. The wake-up time of the proposed clustered block from the standby mode is within one clock. The proposed method is effective to reduce leakage power in a leakage-dominant era.

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