A Vth-Variation-Tolerant SRAM with 0.3-V Minimum Operation Voltage for Memory-Rich SoC under DVS Environment

Yasuhiro Morita[1], Hidehiro Fujiwara[2], Hiroki Noguchi[3], Kentaro Kawakami[2], Junichi Miyakoshi[2], Shinji Mikami[1], Koji Nii[2], Hiroshi Kawaguchi[3], and Masahiko Yoshimoto[3]
[1] Graduate School of Natural Science and Technology, Kanazawa University
[2] Graduate School of Science and Technology, Kobe University [3] Faculty of Engineering, Kobe University
1-1 Rokkodai-Cho, Nada-Ku, Kobe 657-8501, Japan
Phone & Fax: +81-78-803-6234 E-mail: y-morita@mics.ee.t.kanazawa-u.ac.jp

Abstract

This paper proposes a voltage-control scheme for an SRAM that makes a minimum operation voltage down to 0.3 V even on a future memory-rich SoC. A self-aligned timing control guarantees stable operation in a wide range of Vdd under DVS environment. A measurement result of a 64-kb SRAM in a 90-nm process technology shows that 30% power reduction is achieved at 100 MHz. The area overhead is only 5.6%.

Keywords: SRAM, DVS, and low power

Introduction

In order to save power of an SoC, DVS that adaptively controls operation frequency and supply voltage (Vdd) has been implemented in a mobile system [1]. However, a minimum operation voltage (Vmin) is becoming higher due to threshold-voltage (Vth) variation as fabrication technology is scaled down. On a future SoC, since a chip area of 90% or more is supposed to be occupied with memories, Vmin will be restricted by the Vth variation of the memories, which hinders wide-range power scaling of an SoC with DVS. In this paper, we report an optimum voltage-control scheme that lower Vmin, and a self-aligned timing control for the Vth-variation-tolerant SRAM.

Optimum Voltage-Control Scheme

Under DVS environment, a variable supply voltage (Va) is adaptively controlled, which is between Vmin and Vmax. In this paper, Vmax is set to 1.0 V as a nominal voltage in a 90-nm process technology. In order to decrease Vmin, the voltage controls of the conventional 6T memory cell summarized in TABLE I, but not a 7T memory cell with area overhead [2], are applied to the SRAM. A supply voltage of the memory cells is set to Vmax in a read operation to maximize read margin. Alternatively in a write cycle, a wordline (WL) voltage is set to Vmax to obtain write margin. An n-well bias (Vbp) for load pMOSFETs in the memory cells is tied to Vmax, which increases the pMOSFET Vth and write margin when Va is less than Vmax. Although the negative Vbp is utilized, a serious problem of a gate-induced drain leakage (GIDL) or negative bias temperature instability (NBTI) does not occur since Vbp does not exceed Vmax.

Fig. 1 shows milky-way plots of memory cells obtained by simulation. A Vth variation with a 6σ variance is considered in both global (wafer-to-wafer variation) and local (random variation) components. For stable operation, four process corners (FF, FS, SF, and SS) must be between the read and write limits. In the conventional SRAM, the margins become smaller as Va is decreased (see Fig. 1 (a)). To the contrary as shown in Fig. 1 (b), the proposed scheme ensures sufficient read and write margins.

Circuit Design

Fig. 2 illustrates a block diagram of the novel SRAM that the optimum voltage-control scheme is applied. In the proposed SRAM, a memory cell array is divided into 64 blocks so that one block has 128 words by 8 bits, in which the voltage controls are done by block-by-block basis since Vdd lines in the memory cells are along with bitlines (BLs) [3] unlike the row-by-row Vdd control [4]. Vdd selectors are implemented in order to vary the voltages (Vmc and WL voltage), and level shifters are introduced just after X decoders in order to amplify WL voltages to Vmax in the write cycle. In addition, the divided WL structure [5] that can hierarchically access to a local WL is applied since the voltage conditions in the write cycle destroy stored data in other blocks if the conventional single WL structure is used. In the proposed SRAM, a channel length of access transistors is set to 0.15 μm, which is longer than the minimum rule of 0.10 μm. This does not only improve the read margin, but also reduces a BL leakage current within a marginal delay overhead.

Self-Aligned Timing Control

A proper sequence of the voltage controls is of importance to avoid unexpected flips in the memory cells. When a cycle is changing from write (or non access) to read operation, it should be noted that a destructive read occurs if a WL voltage gets higher than Vmc. In order to clear this issue, a timing-adjustment mechanism between the WL voltage and Vmc in Fig. 3 (a) is necessary. Moreover as shown in Fig. 3 (b), another sequence that a WE signal is negated after a WL voltage is grounded, is also necessary when the write operation is concluded. In order to secure these sequences, a self-aligned timing control in Fig. 2 is implemented with a dummy WL and its feedback.

Simulation and Measurement Results

A 64-kb SRAM test chip was designed and fabricated in a 90-nm CMOS process technology to verify the feasibility of the proposed scheme. Fig. 4 shows a micrograph of the test chip and a layout view of a memory-cell block. The area overhead of the proposed SRAM is 5.6%, which is basically caused by the Vdd selectors and level shifters.

Fig. 5 (a) demonstrates the proposed scheme improving the operation margins by means of a measured fail bit count (FBC). The clock cycle time in this measurement is as slow as 1 μs in order to evaluate Vmin, which is 0.55 V in the conventional SRAM while the proposed one is as low as 0.3 V at the CC process corner. In the conventional scheme, the Vth variation of memory cells governs Vmin. However in the proposed scheme, the value of 0.3 V means a lower limit of peripheral circuits, but not memory cells, since the memory cells have a larger margin as Va is decreased as shown in Fig. 1. Note that in the conventional scheme, Vmin gets higher at the worst case of FS corner as shown in Fig. 5 (b) which is estimated by simulation. If a memory capacity is assumed to be 64 Mb, the conventional scheme does not work below 0.68 V, which hinders the DVS advantages.

Fig. 6 (a) shows power dependences on an operation frequency (P-f curves). Va is implicitly adjusted according to the operation frequency. A performance penalty by applying the proposed scheme is 1% when Va is 1.0 V. The proposed P-f curve has the advantage of low power in a low operation-frequency region, and 30% power reduction at 100 MHz was confirmed by the measurement. Since the proposed scheme makes Vmin much lower as memory capacity increases, DVS can be enjoyed even on a future memory-rich SoC as indicated in Fig. 6 (b).

Acknowledgments

The VLSI chip in this study was fabricated through the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo, with the collaboration by STARC, Fujitsu Limited, Matsushita Electric Industrial Company Limited, NEC Electronics Corporation, Renesas Technology Corporation, and Toshiba Corporation. The authors would like to appreciate Prof. K. Kobayashi of Kyoto University and Kyoto VDEC Sub-Center for measuring the test chips.

References

[1] H. Ohira, et al., IEICE Trans. Electron., Vol.E87-C, No.4, pp.457-465, Apr. 2004.
[2] K. Takeda, et al., IEEE ISSCC, pp.478-479, Feb. 2005.
[3] K. Osada, et al., IEEE JSSC, Vol.36, No.11, pp.1738-1744, Nov. 2001.
[4] F. R. Saliba, et al., IEEE Symp. VLSI Circ., pp.162-165, June 2005.
[5] M. Yoshimoto, et al., IEEE JSSC, Vol.18, No.5, pp.479-485, Oct. 1983.

TABLE I
Details of voltage controls.

State / Part	Conv.	Optimum		
		Read	Write	Non-access
Peripheral Vdd	Va	Va	Va	Va
BL pre-charge level	Va	Va	Va	Va
WL swing	Va	Va	Vmax	-
MC Vdd	Va	Vmax	Va	Va
MC Vbp	Va	Vmax	Vmax	Vmax

Vmax: Maximum supply voltage
Va: Variable supply voltage under the DVS environment

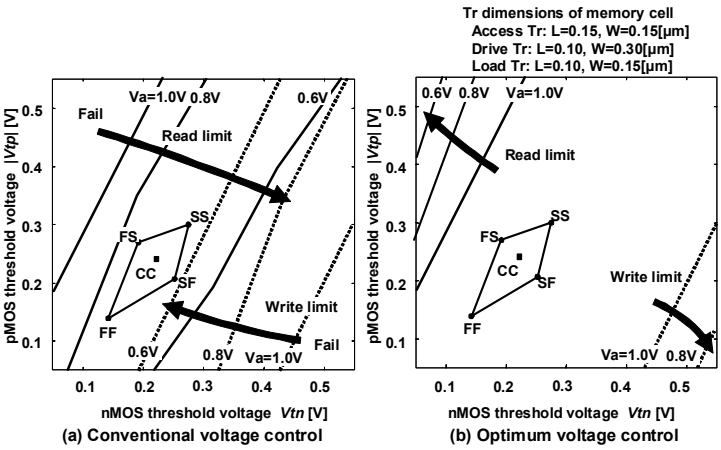

Fig. 1. Milky-way plots of (a) the conventional memory cell, and (b) proposed memory cell using optimum voltage-control scheme.

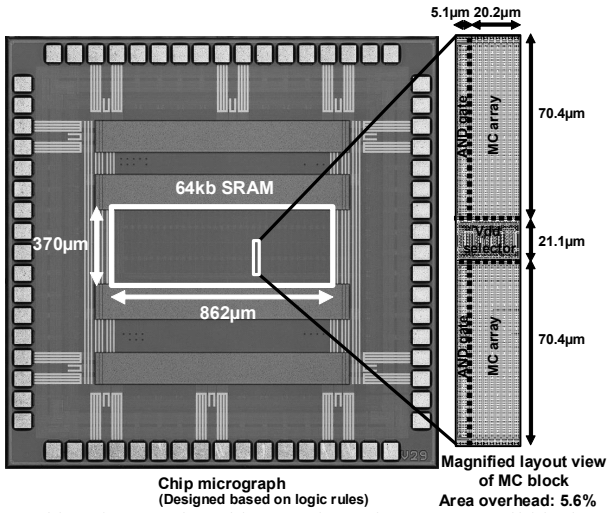

Fig. 4. Chip micrograph and layout view of a memory-cell block.

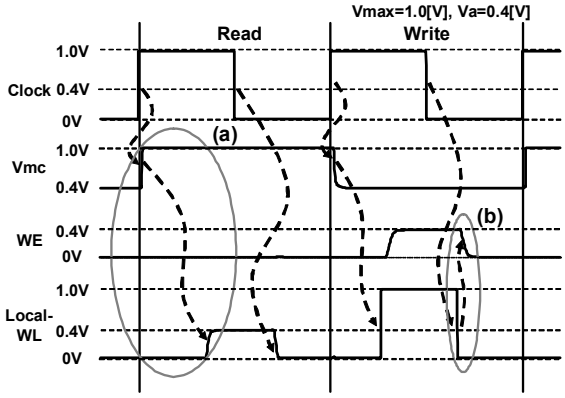

Fig. 3. Timing chart of voltage controls.

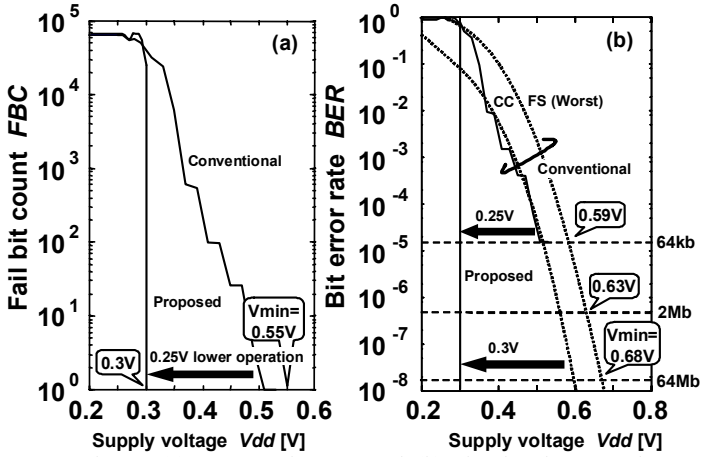

Fig. 5. (a) Measured FBC, and (b) simulated BER when a process corner and memory capacity are varied.

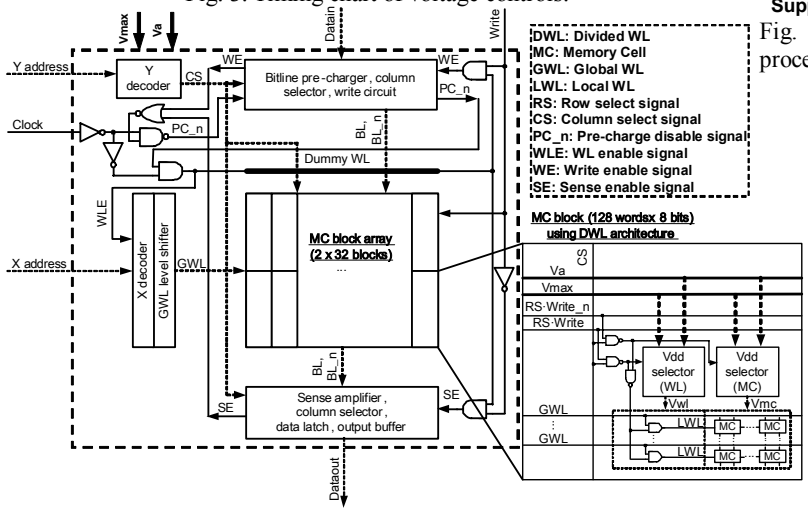

Fig. 2. Block diagram of the proposed 64-kb SRAM.

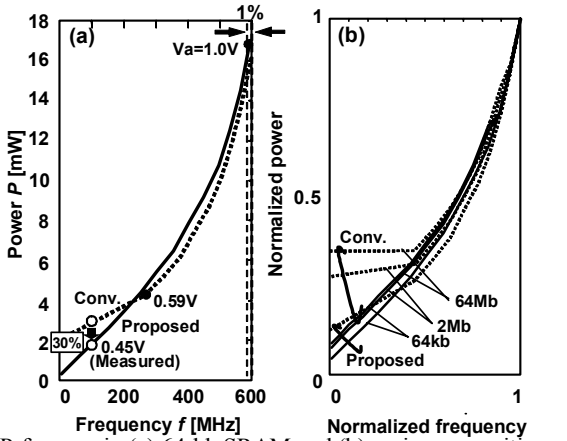

Fig. 6. P-f curves in (a) 64-kb SRAM and (b) various capacities.