A Power-Variation Model for Sensor Node and

the Impact against Life Time of Wireless Sensor Networks

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Abstract— **We introduce manufacturing variation into a power model for a wireless sensor network node. Network protocols for the wireless sensor networks such as media access control and routing should be evaluated in terms of life time in a whole system. In fact, there exists power variation node by node due to the manufacturing variation. In the previous researches, however, this effect has not been investigated at all since it has been supposed that all nodes have a same power. In this paper, we develop a power model for a sensor node, in which we consider threshold-voltage variation derived from a manufacturing process. We take both a microprocessor and an RF part into account for the model, and implement it to QualNet in order to evaluate the impact against a life time of a wireless sensor network. The simulation results show that the conventional model has overestimated the life time longer than our model when nodes are randomly deployed. In contrast, if we make an optimum deployment of nodes by exploiting the power variation, the network life time is extended by 12.7% compared to the case of the conventional model.**

Keywords- Sensor networks; Analytical modeling, performance analysis, optimization, and simulation.

I. INTRODUCTION

In wireless sensor networks (WSNs), expansion of available time, i.e. life time, is one of the most important subjects. Network protocols for the WSNs such as media access control and routing should be evaluated in terms of life time in a whole system. Therefore, many researchers have implemented their proposed protocols into network simulators such as NS-2 and QualNet [1] [2]. In their studies, all nodes have a same power performance. However in fact, there exists power variation node by node due to manufacturing variation, where only a few nodes with high power consumption may shorten the network life time. To the best of our knowledge, this aspect has not been addressed at all so far.

Process, voltage, and temperature (PVT) are major factors of variation on a CMOS LSI. The process variation is called a manufacturing variation, which is twofold: systematic variation, i.e. global variation, and random variation, i.e. local variation. Although both the variations take the form of a threshold-voltage variation, behaviors are different. The random variation appears as a transistor-by-transistor variation while the systematic one is observed as a chip-by-chip variation. The random variation is mitigated in a chip power since millions of transistors are distributed on a chip. In this paper, therefore, we consider only the systematic variation as a first step. As far as we know, quantitative data about the global threshold-voltage variation has not been published. We infer a standard deviation of the threshold-voltage variation in a latest CMOS process technology from [3], and utilize it for the modeling and network simulation.

In this paper, we describe the effect of the power variation of sensor nodes. First, we develop a power model for a sensor node considering the threshold-voltage variation in a microprocessor and an RF (radio frequency) part, which we call the *threshold-voltage variation (TV) model*. We then implement the model into QualNet that is one of network simulators, and evaluate a network life time as a metric of a system-level performance.

In a recent scaled-down microprocessor, the threshold-voltage variation gives a strong impact on subthreshold-leakage current that is a source of a leakage power. The leakage power is dominant in a standby mode and affects a life time of a sensor node since it intermittently function to save an operating power. On the other hand in an RF part, the threshold-voltage variation takes the form of a bias-current variation, and its power would be dominant in a transceiver operation. In our model, we account for both a microprocessor and RF part.

The rest of the paper is organized as follows: In Section II, we show a typical architecture of a sensor node, and mention power components on it. In Section III, we describe the TV model and expand it to power-variation models. In Section IV, we compare the TV model with the conventional *threshold-voltage constant (TC) model* from the viewpoint of network life time using a simulator. Finally, we summarize the paper in Section 5.

II. SENSOR NODE ARCHITECTURE AND POWER COMPONENTS

Fig. 1 shows a typical schematic of a sensor node. A small battery, solar cell, or even energy scavenging such as vibration energy [4] is utilized as a power source, and thus its output voltage is not regulated. The step-down DC-DC converter in the figure regulates the output voltage of the power source down to a lower one, which is supplied to a node chip as a nominal supply voltage (V_{dd}). Once the output voltage of the power source becomes lower than V_{dd}, the node chip does not function since the step-down DC-DC converter cannot compensate the negative voltage gap. If the power consumption of the node chip is varied node by node, it means that its life time is varied as well.

As illustrated in Fig. 1, a node chip is generally comprised of two blocks: a microprocessor and an RF part. The RF part receives/transmits data and control packets from/to other sensor nodes by means of radio waves, and the microprocessor handles the data and control packets. The microprocessor can be further divided into logic circuits and memory. Hence, the sensor chip consists of three components. The logic circuits, memory, and RF part, however, have different characteristics in terms of power.
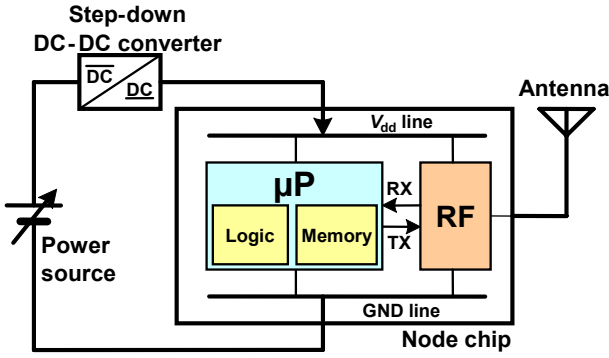

Fig. 1. A typical sensor node. A µP signifies a microprocessor.

A. Dynamic Power in Logic Circuit

The logic circuits are comprised of digital circuits. Since the logic circuits are always clocked and data are frequently alternated between logic "low" and "high", the activation ratio is large. Fig. 2 represents a digital circuit, in which a dynamic power consumed by charge and discharge is dominant. The dynamic power (P_{dyn}) is proportional to the square of V_{dd}, and is given as follow [5]:

$$P_{dyn} = K_{dyn} V_{dd}^2 , \qquad (1)$$

where $K_{dyn}=p_a f_{op} C_{total}$. p_a is an average activation ratio (typically around 0.3), f_{op} is an operating frequency, and C_{total} is a total gate capacitance (+ other parasitic capacitance) in a circuit.

B. Leakage Power in Memory

As a memory element, an SRAM is widely utilized because it is compatible with a CMOS process technology. In an SRAM, a dynamic power is small since only some memory cells are accessed. Even though almost all memory cells are on standby, leakage currents flow through the standby memory cells and bitlines as illustrated in Fig. 3.

Consequently, the leakage power caused by the subthreshold-leakage currents becomes dominant in the SRAM. Other than the memory cells, the logic circuits, of course, draws other leakage current (see Fig. 2), however, the mechanism of the leakage current is the same.
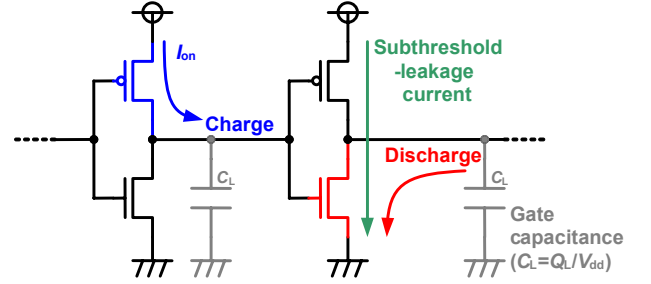

Fig. 2. A digital circuit. A on-current of a pMOS transistor (I_{on}) charges up C_L (load capacitance: gate capacitance + other parasitic capacitance), and then turns on an nMOS transistor at a next logic gate, which in turn discharges its own charge.
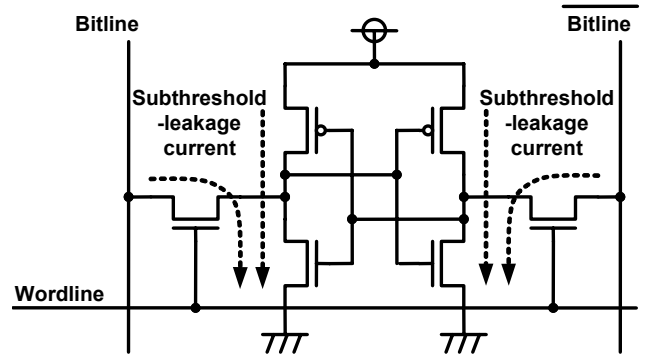

Fig. 3. An SRAM memory cell. In a standby state, subthreshold-leakage currents flow through cross-coupled inverters, as well as from bitlines although a wordline is logic "low".

Even when a transistor is turned off and is in a subthreshold region, a subthreshold-leakage current flows through the transistor. The leakage power (P_{leak}) is expressed as follows [5]:

$$P_{leak} = K_{leak} V_{dd} 10^{-\frac{V_{th}}{s}} , \qquad (2)$$

where K_{leak} is a constant. V_{th} is a subthreshold voltage of a transistor. s is a subthreshold swing, and is about 0.1 V/decade in a recent process technology. This implies that a subthreshold-leakage current ten times goes up when V_{th} is reduced by 0.1 V.

C. Analog Power in RF Part

The dynamic power and leakage power mentioned in the previous subsections are the major power components in the microprocessor operating digitally. In contrast, an RF circuit is a kind of analog circuit, and its behavior is different from that of the microprocessor. Fig. 4 illustrates a low-noise amplifier that is representative analog circuit utilized widely in a receiver. Even in a transmitter, a same type of

configuration is also adopted as a power amplifier. In the low-noise amplifier as well as other analog circuit, an amplifying transistor is biased to an intermediate voltage by a bias circuit and hence is in a saturation region, which means it always draws a bias current. The power caused by the bias current is dominant in the amplifier.

In an analog-circuit design, long-channel transistors are used to avoid the channel-length modulation effect, and to obtain the ideal saturation characteristics as expressed with the Shockley model. The analog power consumed by the bias current (P_{analog}) is given as follows [6]:

$$P_{analog} = K_{analog} V_{dd} V_{OD}^{\alpha}$$
$$= K_{analog} V_{dd} (V_{gs} - V_{th})^2, \qquad (3)$$

where K_{analog} is a constant. V_{OD} is called an overdrive voltage and is defined as $V_{gs}-V_{th}$. α is a velocity saturation index and is set to two for a long-channel transistor used in an analog-circuit design [7].
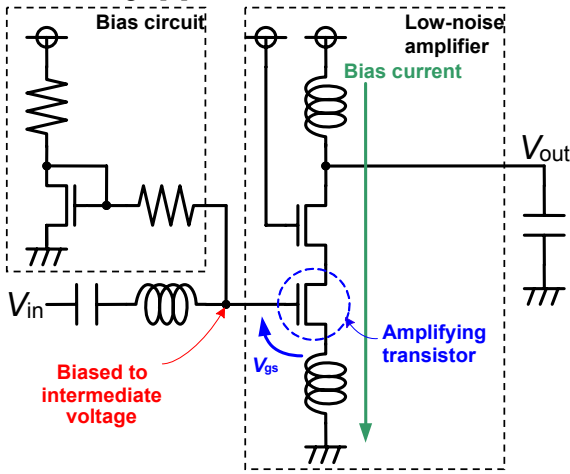

Fig. 4 A low-noise amplifier.

III. THRESHOLD-VOLTAGE VARIATION AND POWER-VARIATION MODEL

In a CMOS process technology, doping concentration and oxide thickness turn out to be different chip by chip, which causes threshold-voltage variation as manufacturing variation. Since a microprocessor and an RF part are supposed to be located on a same chip for a low-cost solution, the threshold-voltage variation gives impacts of power variation to a whole chip. The sizes of the impacts are, however, different in the three power components.

In this section, we introduce a threshold-voltage variation into the power variations of the three power components, and discuss their models. Note that an energy variation in a power source (e.g. battery or super capacitor) is not considered, but we can carry out a similar analysis if its variation is known.

The threshold-voltage variation has a standard distribution as exemplified in Fig. 5. Process engineers and circuit designers can select an average value of a threshold voltage (μ_{Vth}) as a design choice to optimize circuit performance. In contrast, a standard deviation of a threshold voltage (σ_{Vth})

depends on a process technology, and thus they can not easily control it. In this paper, we set μ_{Vth} to 0.3 V supposing a low-power microprocessor, and infer that σ_{Vth} is 0.025 V from an Intel's research [3] (see Appendix A.1 and A.2 for more detail). σ_{Vth} could become larger in a process technology that is not so recent as Intel.

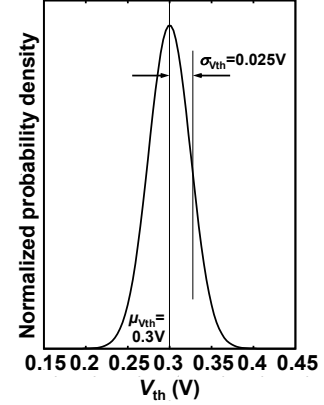Fig. 5. An example of threshold-voltage distribution assumed in this paper.

A   Dynamic-Power Variation

If z is a function of V_{th} and is given by the following expression:

$$z = g(V_{th}), \qquad (4)$$

the standard deviation of z (σ_z) can be derived with the first-order approximation as follows:

$$\sigma_z = g'(\mu_{Vth})\sigma_{Vth}. \qquad (5)$$

Since the dynamic power is not a function of V_{th} as given in (1), the standard deviation of P_{dyn} (σ_{Pdyn}) becomes zero:

$$\sigma_{Pdyn} = 0. \qquad (6)$$

B   Leakage-Power Variation

Unlike the dynamic power, the leakage power is varied by the threshold-voltage variation since it is a function of V_{th}. From (2), the standard deviation of the leakage power (σ_{Pleak}) is obtained as follows:

$$\sigma_{Pleak} = K_{leak} V_{dd} \frac{\ln[10]}{s} 10^{-\frac{\mu_{Vth}}{s}} \sigma_{Vth}. \qquad (7)$$

C   Analog-Power Variation

Based on (3), the standard deviation of the analog power ($\sigma_{Panalog}$) is given as follows:

$$\sigma_{Panalog} = 2K_{analog} V_{dd} (V_{gs} - \mu_{Vth})\sigma_{Vth}. \qquad (8)$$

D   Total-Power Variation

The abovementioned discussion leads the total-power variation to a standard-distribution model. We can approximately obtain the average value and standard deviation of the node power (μ_{Ptotal} and σ_{Ptotal}) from (1), (2), (3), and from (6), (7), (8), respectively:

$$\mu_{Ptotal} = K_{dyn} V_{dd}^2$$
$$+ K_{leak} V_{dd} 10^{-\frac{\mu_{Vth}}{s}} ,\qquad (9)$$
$$+ K_{analog} V_{dd} (V_{gs} - \mu_{Vth})^2$$

$$\sigma_{\text{Ptotal}} = \sigma_{\text{Pdyn}} + \sigma_{\text{Pleak}} + \sigma_{\text{Panalog}} . \quad (10)$$

The parameters in the expressions can be given by process engineer and circuit designers. Once the parameters are fixed, this model gives insight to the power distribution, and we can evaluate it more elaborate than the conventional model.

Fig. 6 shows an example of the power variations on a node chip. The three power components have different scenarios for the subthreshold-leakage variation:

1. Dynamic power: Supposing that $V_{\text{dd}}=1.2$ V and $\mu_{\text{Pdyn}}=1.2$ mW, K_{dyn} becomes $1/1200$ according to (1). The value of 1.2 mW is reasonable compared with [8].

2. Leakage power: As for memory, we assume a small portion in this design. The SRAM consumes much less than the logic circuits. We set μ_{Pleak} to 0.16 mW. Thereby, K_{leak} is 0.133 when s is 0.1 V. σ_{Pleak} becomes $-3.68\times10^{-3}\sigma_{\text{Vth}}$.

3. Analog power: To draw the curve of the analog-power variation, we carried out a circuit simulation of the low-noise amplifier in Fig. 4. We assumed that μ_{Panalog} is equal to the power of the microprocessor at the threshold voltage of μ_{Vth} ($\therefore\mu_{\text{Panalog}}=\mu_{\text{Pdyn}}+\mu_{\text{Pleak}}=1.36$ mW), and obtained the following linear characteristics of the analog power in terms of V_{th}:[1]

$$P_{\text{analog}} = -4.12\times10^{-3}V_{\text{th}} + 2.60 . \quad (11)$$

As a result, σ_{Panalog} is $-4.12\times10^{-3}\sigma_{\text{Vth}}$.

In the conventional TC model that does not consider the threshold-voltage variation, V_{th} only takes 0.3 V and the total power would be 2.72 mW ($=1.2+0.16+1.36$ mW) on all node chips.
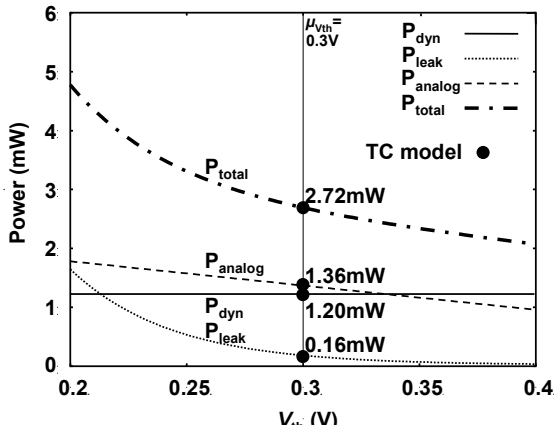

Fig. 6. An example of power variations in the TV and TC models.

Fig. 7 summarizes the exact distribution of the total power, and the approximation model using (9) and (10). We can

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[1] If $V_{\text{OD}}\gg\mu_{\text{Vth}}-V_{\text{th}}$, (3) is approximated as follows:

$$
\begin{aligned}
P_{\text{analog}} &= K_{\text{analog}}V_{\text{dd}}(V_{\text{OD}} + \mu_{\text{Vth}} - V_{\text{th}})^2 \\
&= K_{\text{analog}}V_{\text{dd}}\left(V_{\text{OD}}^2 + 2V_{\text{OD}}(\mu_{\text{Vth}} - V_{\text{th}}) + (\mu_{\text{Vth}} - V_{\text{th}})^2\right) \\
&\approx K_{\text{analog}}V_{\text{dd}}\left(V_{\text{OD}}^2 + 2V_{\text{OD}}(\mu_{\text{Vth}} - V_{\text{th}})\right)
\end{aligned}
$$

analytically obtain the exact distribution from (1), (2), (3), and Fig. 5, but the exact distribution is not a strict standard distribution because (2) and (3) are not linear functions of V_{th}. Besides, the other standard distribution approximated with (9) and (10) are the first-order approximation. The approximation is, however, quite reasonable since the curves in Fig. 6 exhibit linearity around μ_{Vth}, and thus it fits well into the exact distribution (compare the curves in Fig. 7). The average powers in the TV and TC models are almost the same, but their network life times are not as will be described in the next section.
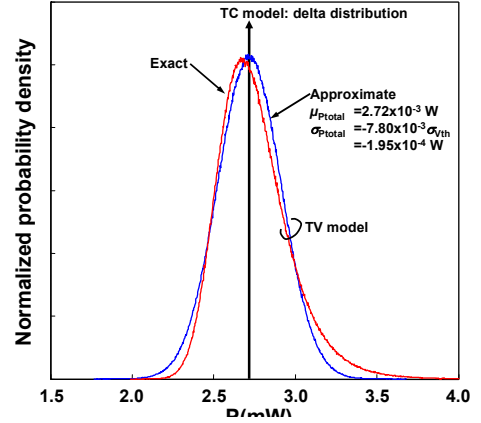

Fig. 7. Power distributions in the TV and TC models. The conventional TC model has a delta distribution while the approximated TV model has a standard distribution.

IV. VERIFICATION WITH NETWORK SIMULATOR

A. Influence of Node Variation on WSNs

In this section, we implement both the TV and TC models to a network simulator, and investigate the impact of the power variation on system-level performance from the viewpoint of life time. The network simulator used is QualNet [2]. In a field of 100×100 m^2, 256 sensor nodes are deployed at random, and a base station is placed in the center. We assume that the application is data gathering, where each sensor node transfers its sensed data to the base station every round which is set to 1,000 seconds. A physical layer protocol is Low Power Listening [9], and its duty cycle ratio is set to 0.5%. The MAC layer protocol is PAMAS [10]. The network layer protocol is Tiny Diffusion [11], and an interest is flooded only once at the beginning of a simulation trial. We define a life time as a duration for which a successful data received rate is 90% or more.

Fig. 8 shows the characteristics of the successful data received rates in cases of the TV and TC power models. The average power of a microprocessor ($\mu_{\text{Pdyn}}+\mu_{\text{Pleak}}$) and an RF part ($\mu_{\text{Panalog}}$) are set to the same for both power models in Fig. 8 (a). In Fig. 8 (b), the ratio of the microprocessor power to the RF power is 0.9:0.1. In a future sensor node, a microprocessor power may increase in order to handle encryption/decryption, and Fig. 8 (b) predicts such a case.

Recall that the TV model consumes almost the same power as the TC model on average. However, we observe that the proposed TV model results in a shorter life time than the conventional TC model by 10.8% in Fig. 8 (b) because in the TV model, some nodes have inefficient power performances. This fact can make the network vulnerable. By contrast, this effect is not involved in the TC model. This is the reason why the figures show that the TC model indicates the optimistic results compared with the TV model. By comparison between Figs. 8 (a) and (b), we find that the successful received data rate shown in Fig. 8 (b) starts to drop earlier than that in Fig. 8 (a). This implies that the microprocessor power is distributed more widely than the RF power.
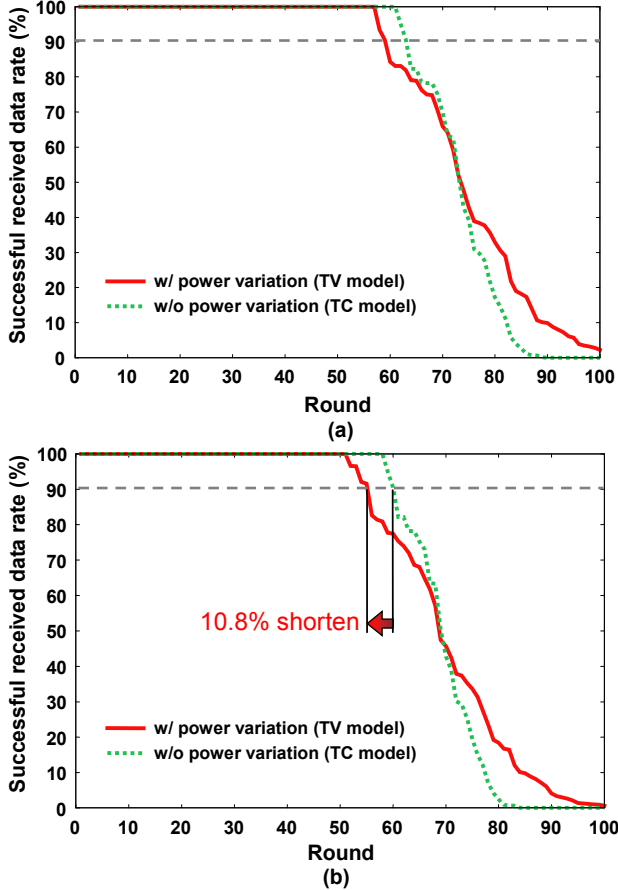

Fig. 8. Successful data received rates in cases of (a) $\mu_{Pdyn}+\mu_{Pleak}$:$\mu_{Panalog}$ = 0.5:0.5, and (b) $\mu_{Pdyn}+\mu_{Pleak}$:$\mu_{Panalog}$ = 0.9:0.1.

B. Optimum Deployment of Sensor Nodes

The optimum deployment of sensor nodes with the power variation maximizes its life time in WSNs. The nodes near a base station very often communicate to relay packets from other nodes, and consume more power than ones away from the base station [12]. Fortunately, we can infer a threshold voltage from a leakage test (I_{DDQ} test) in a burn-in phase, and thus can sort node chips into some bins. It is preferable that low-power nodes are deployed near the base station, and high-power ones are disposed away from the base station. We demonstrate the network simulation result of this optimum

deployment in Fig. 9. The network life time is extended by 12.7%, and it can be said that this optimum deployment exploits the power variation well.
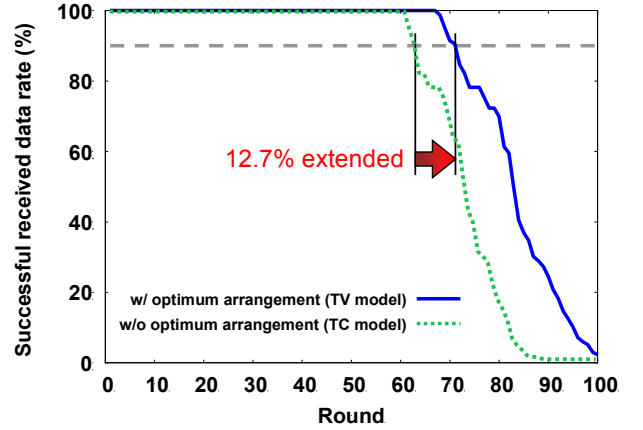

Fig. 9. Life time in the optimum deployment ($\mu_{Pdyn}+\mu_{Pleak}$:$\mu_{Panalog}$ = 0.5:0.5).

V. SUMMARY

In this paper, we developed a power model considering manufacturing variation of a subthreshold voltage in a microprocessor and an RF part, which we named the TV model. We implemented the model to QualNet, and the simulation results showed that the conventional model which we call the TC power model optimistically estimated a network life time longer than our proposed TV model by 10.8%. We have also demonstrated that the optimum deployment of sensor nodes with the power variation extends the network life time by 12.7% compared to the case of the conventional TC model.

ACKNOWLEDGMENT

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APPENDIX

A.1 Threshold-Voltage Variation in Intel High- Performance Microprocessor

The distribution of the maximum operating frequencies in the chip dies of the Intel high-performance microprocessors was reported in [3]. Fig. A1 (a) is the systematic variation of the operating frequency reported. Thereby, we can infer its threshold-voltage variation with the following critical-path delay model:

In a CMOS digital circuit illustrated in Fig. 2, a gate delay (T_p) is time to take Q_L to be charged/discharged by a transistor on-current (I_{on}). In a critical path, there are n logic gates connected in series, and thus the maximum operating frequency (f_{max}) is given by the inverse of the critical-path delay as follows:

$$f_{max} \propto \frac{1}{nT_p} = \frac{I_{on}}{nQ_L} = \frac{(V_{dd}-V_{th})^{\alpha}}{nC_LV_{dd}}$$
$$= K_1 \frac{(V_{dd}-V_{th})^{1.5}}{nV_{dd}}, \qquad (A1)$$

where $I_{on}=(V_{dd}-V_{th})^{\alpha}$, and α is a velocity saturation index [7]. In a scaled-down process technology, α is less than two and we set it to 1.5 in this paper [13]. Then, (A1) turns out (A2):

$$V_{th} = V_{dd} - \sqrt[1.5]{\frac{nf_{max}V_{dd}}{K_1}}. \qquad (A2)$$

As design parameters of the Intel microprocessor, we further infer that V_{dd} and μ_{Vth} are 0.9 V and 0.15 V, respectively. They have reported that the critical path has 14

logic gates (n=14). Therefore, a constant (K_1) is 23.3×10^6 in (A2). Fig. A1 (b) is the estimated distribution of the threshold voltage. The standard deviation of the threshold voltage (σ_{Vth}) in the Intel microprocessor is 0.025 V.

A.2 Threshold-Voltage Variation in Sensor Node

Since the operating frequency of 1.2 GHz and the threshold voltage of 0.15 V in the Intel microprocessor are too fast and leaky for a node chip, we modify the design parameters. The critical-path depth (n) in the Intel microprocessor is also fewer due to micro pipelining. We mitigate n and increased it to a triple in the node chip. As for the threshold voltage of the node chip, μ_{Vth} is shifted to 0.3 V as already illustrated in Fig. 5, in order to suppress a subthreshold-leakage current. V_{dd} is set to 1.2 V. Fig. A2 illustrates the estimated distribution of the maximum operating frequency under those conditions, where μ_{fmax}=394 MHz and σ_{fmax}=16 MHz. TABLE A1 summaries the design parameters.
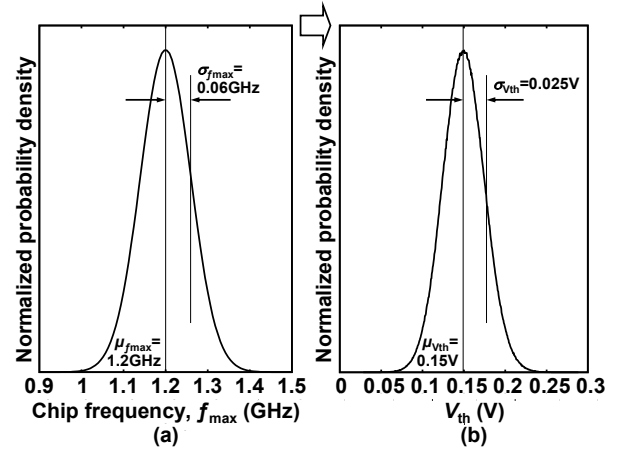

Fig. A1. (a) A maximum frequency distribution in Intel high-performance microprocessors, and (b) its estimated distribution of the threshold voltage.
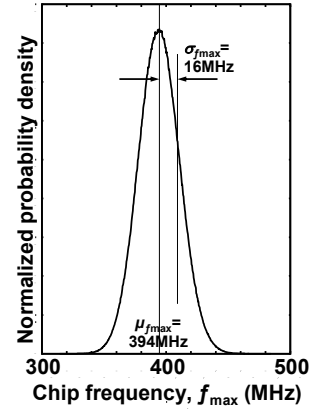

Fig. A2. A distribution of the maximum operating frequency in node chips.

TABLE A1. Design parameter comparison between Intel high-performance processor and node chip.

	n	V_{dd}	μ_{Vth}	σ_{Vth}	μ_{fmax}	σ_{fmax}
Intel μP [3]	14 gates	0.9 V	0.15 V	0.025 V	1.2 GHz	0.06 GHz
Node chip	42 gates	1.2 V	0.3 V	0.025 V	394 MHz	16 MHz