A 10T Non-Precharge Two-Port SRAM for 74% Power Reduction in Video Processing

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Abstract

We propose a low-power non-precharge-type two-port SRAM for video processing. The proposed memory cell (MC) has ten transistors (10T), comprised of the conventional 6T MC, a readout inverter and a transmission gate for a read port. Since the readout inverter fully charges/discharges a read bitline, there is no precharge circuit on the read bitline. Thus, power is not consumed by precharging, but is consumed only when a readout datum is changed. This feature is suitable to video processing since image data have special correlation and similar data are read out in consecutive cycles. As well as the power reduction, the precharge-less structure shortens a cycle time by 38% compared with the conventional SRAM, because it does not require a precharge period. This, in turn, demonstrates that the proposed SRAM operates at a lower voltage, which achieves further power reduction. Compared to the conventional 8T SRAM, the proposed SRAM reduces a charge/discharge possibility to 19% (81% reduction) on the bitlines, and saves 74% of a readout power when considered as an H.264 reconstructed-image memory. The area overhead is 14.4% in a 90-nm process technology.

Keywords

Low-power SRAM, non-precharge SRAM, two-port SRAM, video processing, H.264.

1. Introduction

As the ITRS Roadmap predicts, a memory area is becoming larger, and will occupy 90% of an SoC's area in 2013 [1]. Even on a real-time video SoC, this trend is going on. An H.264 encoder for a high-definition television requires, at least, a 500-kb memory as a search-window buffer, which consumes 40% of a total power [2]. As a process technology is scaled down, a large-capacity SRAM will be adopted as a frame buffer and/or a restructured-image memory on a video chip, and may potentially dissipate a larger portion of power. To save the power in the real-time video application, we report a low-power two-port SRAM in this paper.

A two-port SRAM is suitable for real-time video processing since it can make one read and one write at the same time in a clock cycle [2-5]. In the conventional eight-transistor (8T) two-port memory cell (MC) shown in Fig. 1, two nMOS transistors (N5 and N6) for a read wordline (RWL) and a local read bitline (LRBL) are added to a single-port 6T MC, which frees a static noise margin (SNM) in a read operation [6]. Meanwhile, a precharge circuit must be implemented on the LRBL so that the two nMOS transistors can sink a bitline charge to the ground.

In addition to the precharge circuit, we have to prepare a bitline keeper on the LRBL in the conventional two-port SRAM. Many MCs connecting to the LRBL draw bitline leakage even if they are not selected as a readout bit. Even when a selected MC did not discharge the LRBL ("1" readout), the LRBL voltage would be decreased by the bitline leakage in such case if there was no bitline keeper. The bitline keeper compensates this bitline leakage, and maintains the voltage level on the LRBL during "1" readout [7]. Otherwise, we cannot distinguish a readout current from the bitline leakage, which turns out to readout malfunction.

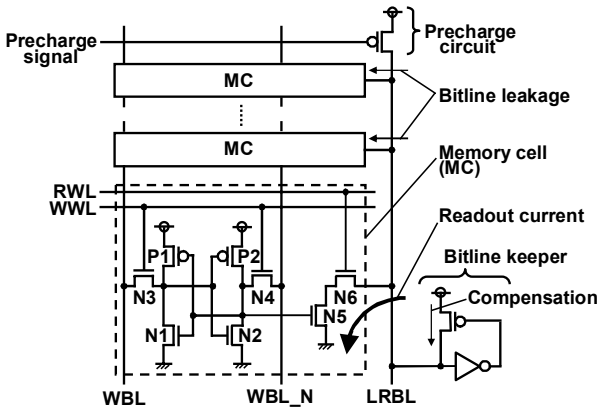


Fig. 1. A schematic of the conventional 8T precharge-type two-port memory cell.

As a process technology is advanced, a supply voltage and a threshold voltage of transistors go down. Since the low threshold voltage increases the bitline leakage, we have to upsize the bitline keeper, and then have to pay area overhead. The large bitline keeper gives negative influence to a readout time as well. To make the matters worse, the delay overhead becomes larger as a supply voltage is decreased.

Fig. 2 illustrates simplified operation waveforms in read cycles in the conventional 8T precharge-type SRAM. Since a precharge scheme is adopted and an LRBL needs to be precharged to a supply voltage by the start time of a clock cycle, a charge/discharge power is consumed on the LRBL when "0" is read out. In contrast, no power is consumed when "1" is read out because the LRBL keeps the supply-voltage level and we do not have to precharge the LRBL.

In our prior study that saves the charge/discharge power on a read bitline, a majority logic circuit and data-bit reordering are accommodated to write "1"s in as many as possible [8] (hereafter, we call the prior SRAM "MJ SRAM" in this paper). The MC structure in the MJ SRAM is same as the conventional 8T SRAM although the read and write circuits are different. Input data comprised of eight pixels are reordered into digit groups (from the most-significant-bit group to the least-significant-bit group), and

then a flag bit is appended to each group. If the number of "0"s in a group is more than that of "1"s, the "0" data are inverted to "1"s by the majority logic circuit. Thereby, we can maximize the number of "1"s in the input data. The inversion information ("1" means inversion) is stored in the additional flag bit. In a read cycle, the group data are inverted if a flag bit is true, and then they are put back in the original order so that we can read out the original data. This mechanism reduces the power of the read bitline because we can statistically increase the possibility that "1" is read where no power is dissipated.

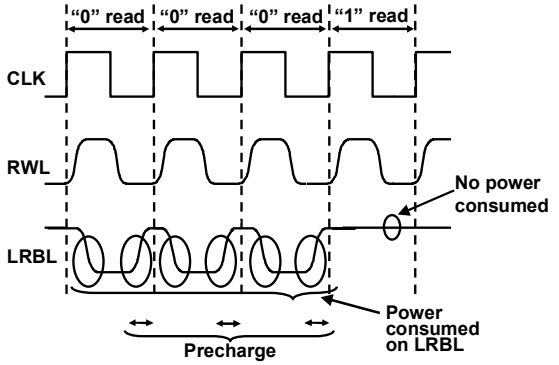


Fig. 2. Waveforms in the conventional 8T precharge-type two-port SRAM in read cycles.

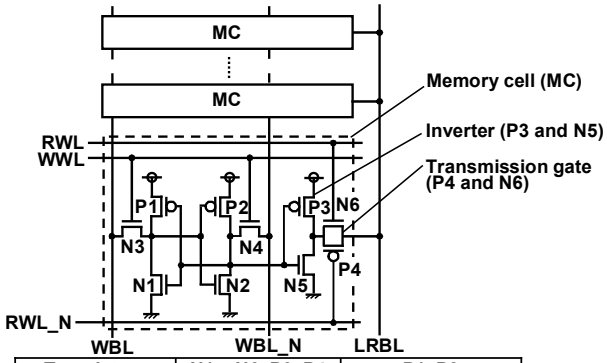
For further power reduction, we will propose a novel non-precharge-type SRAM in this paper. The proposed SRAM reduces bitline power in both cases that consecutive "0"s are read out and consecutive "1" are read out, since there is no precharge circuit on bitlines. The charge/discharge power is consumed only when a readout datum is changed. On the contrary, in the conventional SRAM, consecutive-"0" readout leads to a large bitline power. In addition to the power reduction with the consecutive readout, the proposed SRAM operates in a shorter cycle time since a precharge period is not required. Besides, we can get rid of the bitline keeper, which improves an operation in a low-voltage region. In comparison with the MJ SRAM, our proposed SRAM eliminates the flag bit that causes a power overhead.

The rest of this paper is organized as follows. Section 2 introduces the proposed 10T non-precharge SRAM, and exhibits the reduction of the number of charge/discharge times in simulation. In Section 3, we will describe design and evaluation of a 64-kb SRAM test chip in a 90-nm process technology. Section 4 summarizes this paper.

2. 10T Non-Precharge SRAM

2.1 Circuit

Fig. 3 shows a schematic of the proposed 10T non-precharge two-port MC. Two pMOS transistors are added to the conventional 8T two-port MC, which results in the combination of the conventional 6T single-port MC, an inverter, and a transmission gate. The additional signal (RWL_N) is an inversion signal of RWL, and controls the appended pMOS transistor at the transmission gate. The additional pMOS transistor (P4) increases an LRBL capacitance by 5.5%, compared to the conventional 8T two-port SRAM. While the RWL and RWL_N are asserted and the transmission gate is on, a stored node is connected to an LRBL through the inverter. It is not necessary to prepare a precharge circuit since the inverter can fully charge/discharge the LRBL by itself. Please make sure that there is no precharge circuit either on differential write bitlines (WBL and WBL_N) since they are dedicated for a write port.



Transistors	N1 – N6, P3, P4	P1, P2
Width / Length	0.2μm / 0.1μm	0.2μm / 0.13μm

Fig. 3. A schematic of the proposed 10T non-precharge-type two-port memory cell. Transistor sizes are also denoted.

Fig. 4 illustrates operation waveforms in the proposed 10T non-precharge SRAM. Since the non-precharge scheme is employed, the charge/discharge power on the LRBL is consumed only when the LRBL is changed. Thus, no power is dissipated on the LRBL if an upcoming datum is same as the previous state.

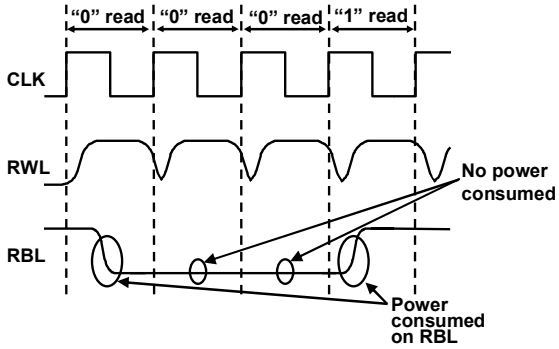


Fig. 4. Waveforms in the proposed 10T non-precharge-type two-port SRAM in read cycles.

The proposed SRAM theoretically reduces a power on the LRBL to a half of the MJ SRAM in a read operation, if readout data are random and the bitline capacitance is same. The transient probability in a sequence of random data is 50% in the proposed non-precharge SRAM while in the MJ SRAM, the number of charge/discharge times becomes one as an expected value. In the MJ SRAM, a pair of a charge and a discharge takes place when "0" is readout. The LRBL power is thus reduced to about 50% in our proposed SRAM in the read operation.

2.2 Application to Video Image

In the proposed SRAM, the charge/discharge power consumed on the LRBLs is proportional to the number of times that a datum flips (the number of transitions: "0" to "1" and "1" to "0") along the time axis. Therefore, we can exploit the proposed SRAM for video processing as well as the MJ SRAM, because adjacent pixels have strong correlation one another in a video image.

In H.264 codec, the YUV format is adopted as a pixel datum. An example is in Fig. 5. One pixel is comprised of an 8-bit luma (Y signal) and 4-bit chroma (U and V signals). In this paper, only luma data are considered. The most significant bits (MSBs) in

consecutive data tend to be lopsided to either "0" or "1" with high probability, while in the least significant bits (LSBs), the values of the bits are random. In other words, the correlation becomes stronger in a more significant bit, which was well exploited in the MJ SRAM.

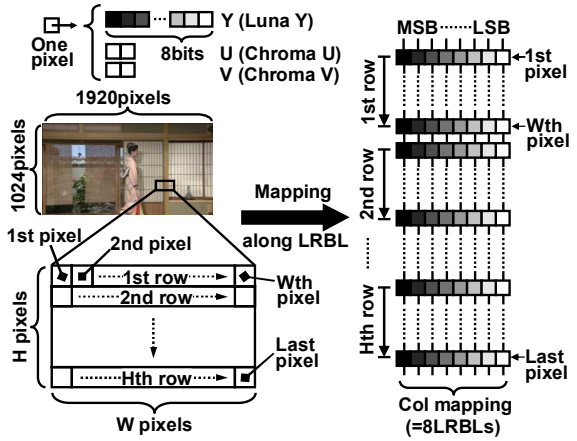


Fig. 5. An example of H.264 image data and its mapping onto eight LRBLs.

Table 1. Simulation conditions in H.264 encoder.

Profile	Main profile
Frame rate	30 fps
Bit rate	7.5 Mbps
Search range	±128 × ±128
Symbol mode	CABAC
JM version	9.8

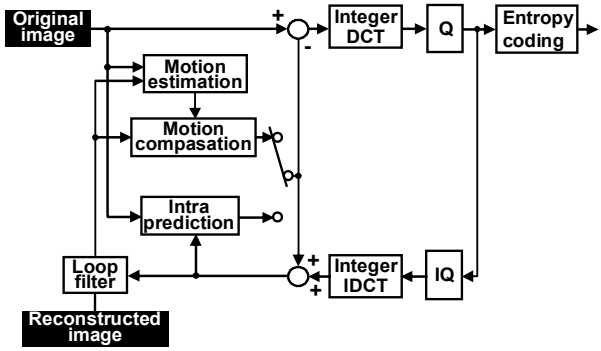


Fig. 6. H.264 encoding process.

As discussed in the previous subsection, the power reduction on the LRBLs is theoretically expected thanks to the non-precharge scheme even if input data are random. Besides, further power reduction is promising since image data are lopsided to "0"s or "1"s with higher possibility in a more significant digit. We exploit these characteristics in the proposed SRAM to reduce the LRBL power as well as the MJ SRAM.

2.3 Optimization of Block Size

In this subsection, we discuss the optimum data mapping that utilizes the spatial correlation in an image. In a video image, the correlations among local pixels are supposed to be different in the vertical and lateral directions. It is important to determine the block size mapped onto an LRBL since a scan path affects effective use of the spatial correlation and power. Assuming an H.264 encoder, we made a simulation under the condition shown in Table 1 to fix the block size. In the simulation, statistic analysis was carried out with the original images and reconstructed images, extracted from ten high-definition test sequences: "Bronze with Credit", "Building along the Canal", "Church", "Intersections", "Japanese Room", "European Market", "Yachting", "Street Car", "Whale Show", and "Yacht Harbor". The original image is encoded, and then its reconstructed image is generated in a local decoding loop, and utilized for motion estimation and motion compensation. The encoding process is depicted in Fig. 6.

Fig. 5 illustrates an example of the block size and its scan path. We set the number of pixels in a block to 256, because the search range is ±128 × ±128 in the H.264 encoder and a burst access over 256 pixels is possible if a full-search algorithm is considered. Hence, in the simulation, a pixel block (W × H pixels) has 256 pixels. The scan path from the 1st pixel to the Wth pixel is mapped onto eight LRBLs.

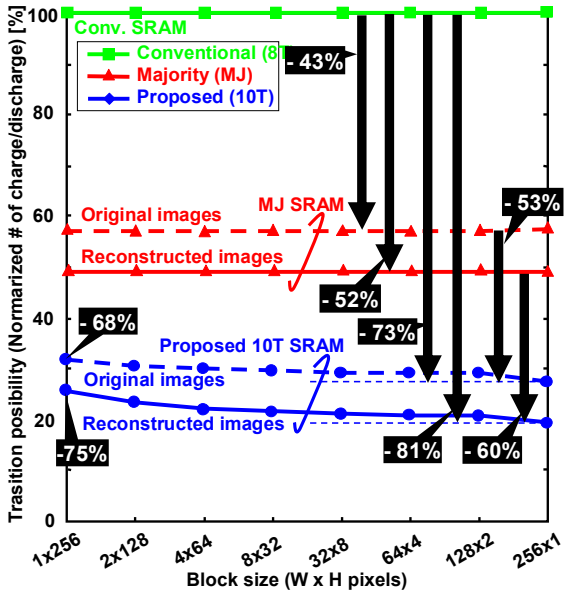


Fig. 7. Transition possibilities (the normalized numbers of charge/discharge times) on an LRBL between the conventional 8T, MJ, and proposed 10T SRAMs when a block size is changed.

Fig. 7 compares the transition possibilities (the normalized numbers of charge/discharge times) on an LRBL between the conventional 8T SRAM, MJ SRAM, and proposed 10T SRAM when the block size is changed. The values are average ones in the ten sequences. In the both cases of the original image and reconstructed image, the block size of 256 × 1 pixels is optimum in terms of power reduction. The graph indicates that the proposed 10T SRAM saves 73% of a dynamic power on an LRBL compared to the conventional 8T SRAM when the original image is read out.

The maximum power saving is achieved when a reconstructed image that has a stronger correlation than the original image is considered. The saving factor is extended to 81% compared to the conventional 8T SRAM, which indicates that the statistical characteristic of the reconstructed image is well exploited. It can

be said that the proposed non-precharge SRAM is suitable for real-time video codec such as MPEG2, MPEG4, and H.264 that require a large-capacity reconstructed-image memory.

3. Design in 90-nm Process Technology

3.1 Overview

Fig. 8 is a chip layout of the proposed non-precharge 64-kb SRAM in a 90-nm process technology. The chip is currently under fabrication. The MC area comprised of ten transistors is 3.96 × 0.76 μm^2. The schematic and the transistor sizes have been already shown in Fig. 3. An MC block is 64 words by 64 bits, in which two 256-pixel blocks can be put.

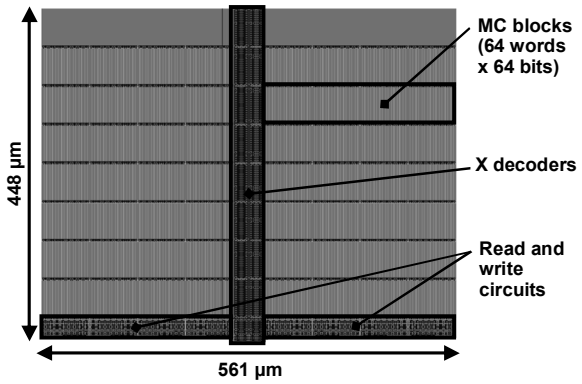


Fig. 8. A layout of the proposed non-precharge 64-kb SRAM in 90-nm CMOS process technology.

Fig. 9 is a block diagram of the proposed SRAM. A hierarchical read-bitline structure (double-bitline structure: LRBLs and global read bitlines (GRBLs)) is applied to avoid a speed overhead of a single-bitline scheme [6]. A GRBL driver drives a GRBL with a block selector signal from the X decoders.

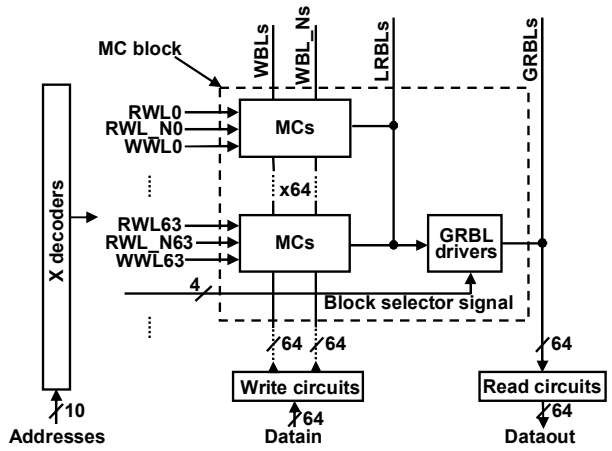


Fig. 9. A block diagram of an memory cell block in the proposed SRAM.

Fig. 10 (a) and (b) show operation waveforms of the proposed non-precharge SRAM when "0" and "1" are read out, respectively. After a block selector signal is asserted, a GRBL is discharged/charged as Dataout. The access times at the "0" and "1" readouts are 0.93 ns and 1.16 ns, respectively. The "0" readout is faster than the "1" readout because nMOS transistors in the GRBL driver and read circuit are stronger than pMOS ones. The figure demonstrates that the proposed SRAM shortens a cycle time to 1.16 ns, thanks to the precharge-less structure. This access time corresponds to a 862-MHz (= 1 / 1.16 ns) operation since the proposed SRAM does not requires a precharge period.

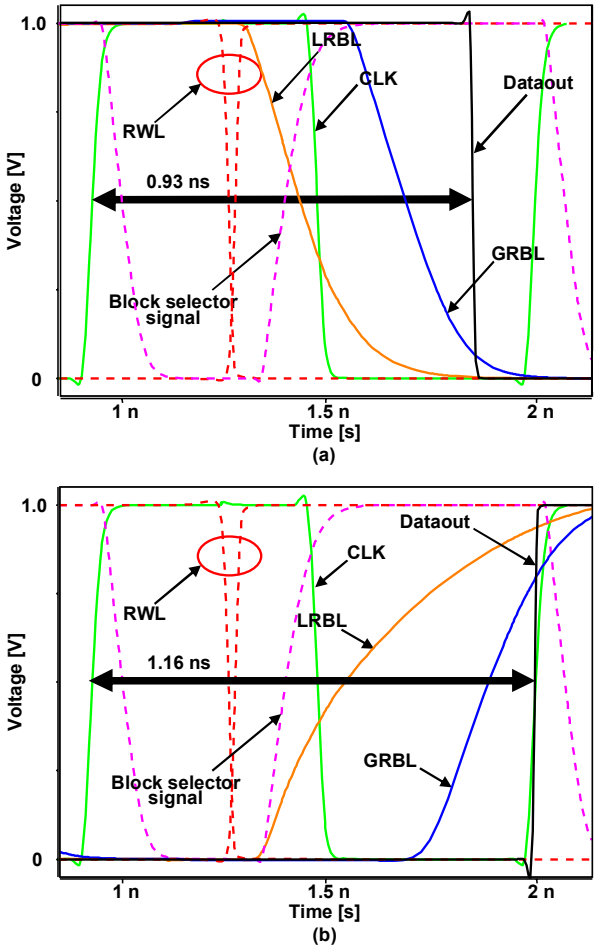


Fig. 10. Operation waveforms of the proposed non-precharge SRAM when (a) "0" and (b) "1" are read out.

We make an area comparison between the conventional SRAM, MJ SRAM, and proposed SRAM in Fig. 11. The area overhead in the proposed SRAM is 14.4% because there are two pMOS transistors added to the conventional 8T MC. However, the read and write circuits are smaller than the conventional SRAM by 1% because of the elimination of precharge and bitline keeper circuits. Besides, we can get rid of flip-flops at data output since a GRBL voltage is not changed up by precharging and it is needless to latch the data output at the beginning of the precharge phase.

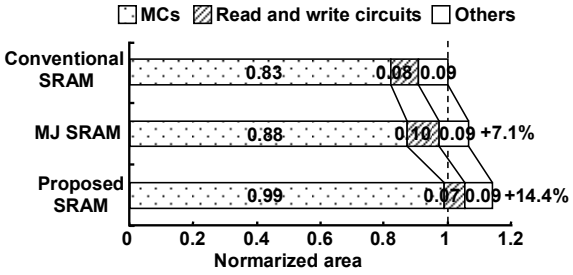


Fig. 11. An area comparison between 64-kb SRAMs in a 90-nm process technology.

3.2 Operating Frequency and Supply Voltage

As described above, there is no precharge period in the proposed SRAM, which can shorten a cycle time compared with other precharge-type SRAMs. This means higher performance in operating frequency. Fig. 12 shows frequency dependences on supply voltage in simulation. At a supply voltage of 1 V, the proposed non-precharge SRAM improves the operating frequency by 315 MHz (65% faster) compared with the conventional precharge SRAM. In other words, the proposed SRAM can run at a lower supply voltage when an operating frequency is same as others. In the conventional SRAM and MJ SRAM, bitline keepers hinder low-voltage operation as mentioned in Section 1. In contrast, the proposed SRAM works at a lower voltage, which achieves much lower power since a dynamic power is proportional to the square of a supply voltage. At an operating frequency of 300 MHz, the proposed SRAM properly operates at 0.69 V while the MJ SRAM does not below 0.85 V.

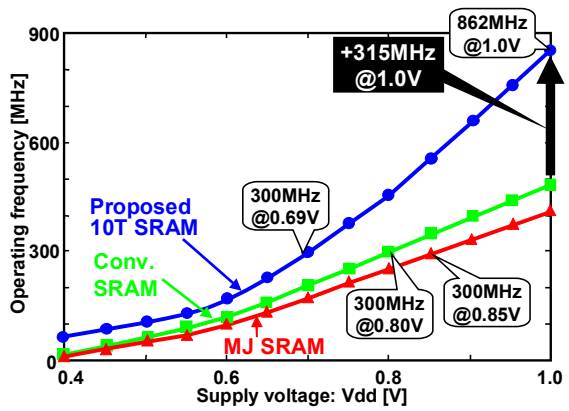


Fig. 12. Operating frequencies versus supply voltage in a 90-nm process technology.

3.3 Power

In the proposed SRAM, we do not have to pay any power overhead in a write operation because the 6T structure at the write port is same as the conventional one. On the other hand, in a read operation, the additional pMOS transistor, P4 in Fig. 3, increases an LRBL capacitance by 5.5% as mentioned in Subsection 2.1. However, please note that the number of charge/discharge times is a half of the conventional case. Thereby, the readout power is theoretically reduced in the proposed SRAM even if data are random.

Fig. 13 makes power comparisons when we vary content stored in the SRAMs. As a video memory, power reduction in a read operation is technically important since readout is made more frequently than write-in. In the conventional 64-kb SRAM, the readout power is estimated at 3.98 mW at a supply voltage of 1.0 V and a frequency of 300 MHz. The readout power on the LRBLs and GRBLs occupies 81% of the total power in the conventional SRAM, and hence the proposed SRAM reduces this part.

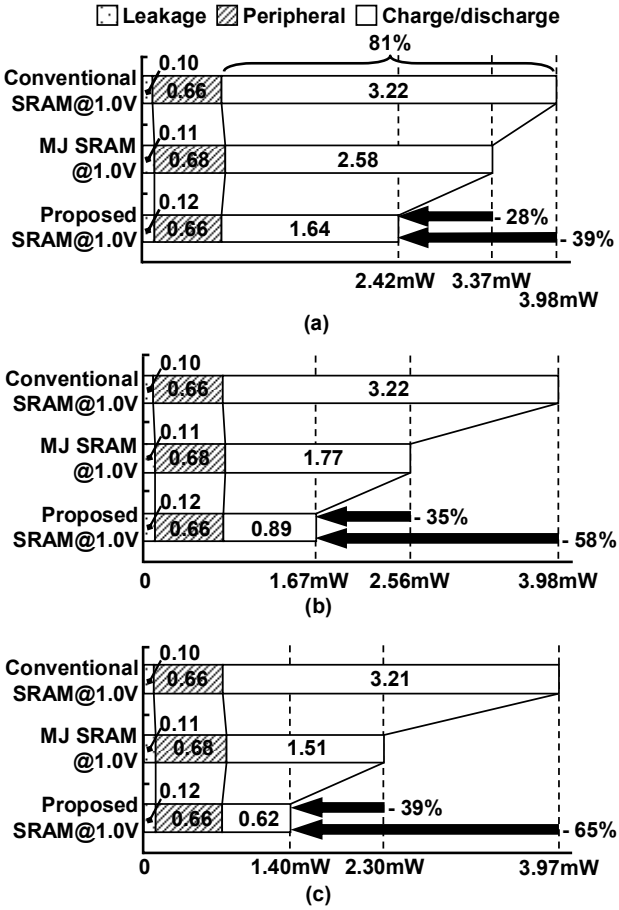


Fig. 13. Readout power comparisons between 64-kb SRAMs in a 90-nm process technology at 1.0 V and 300 MHz (temperature: 25°C). (a) Random data, (b) original image data, and (c) reconstructed image data.

When random data are considered, the proposed SRAM reduces the readout power by 39% and 28% compared with the conventional SRAM and our previous work, MJ SRAM, respectively. If the memory content is an H.264 original image (average of ten video sequences mentioned in Subsection 2.3), the saving factor gets larger to 58% compared with the conventional SRAM. In a reconstructed image, we can maximize the power improvement, where we can save 65% of the readout power.

Fig. 14 compares the readout power in the conventional SRAM, MJ SRAM, and proposed SRAM when a supply voltage is changed, while the operating-frequency condition is still 300 MHz that is the same condition Fig. 13. The supply voltage is the minimum one where an SRAM properly functions at the 300 MHz. The supply voltages are set to 0.8 V, 0.85 V, and 0.69 V in the conventional SRAM, MJ SRAM, and proposed SRAM, respectively, according to Fig. 12. Our proposed SRAM with a 64-kb capacity saves 74% of a total power at the lower supply voltage when it is utilizes as a reconstructed image buffer. Its power

dissipation is 0.67 mW.

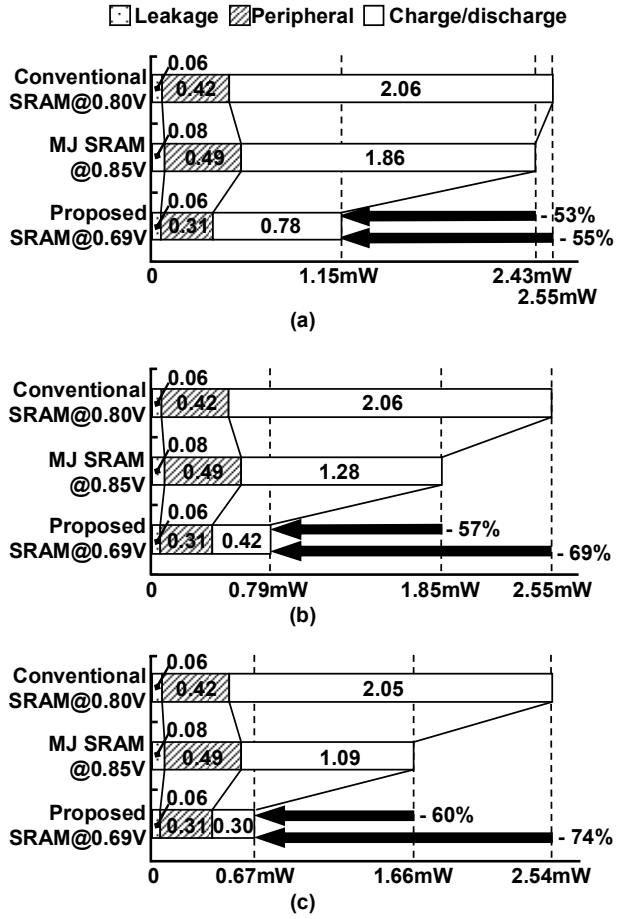


Fig. 14. Readout power comparisons between 64-kb SRAMs in a 90-nm process technology at 300 MHz (temperature: 25°C). (a) Random data, (b) original image data, and (c) reconstructed image data. Please note that supply voltages are different although the operating frequency is fixed to the 300 MHz.

4. Summary

We have proposed a two-port non-precharge SRAM comprised of ten transistors. This SRAM is suitable for a real-time video image that has statistical similarity. The proposed SRAM can operate at a 65% higher frequency than the conventional 8T SRAM since it has no precharge period. The area overhead is 14.4% in a 90-nm process technology. The proposed SRAM saves 74% of a readout power when it is used as an H.264 reconstructed-image memory.

5. Acknowledgments

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