Which is the Best Dual-Port SRAM in 45-nm Process Technology? – 8T, 10T Single End, and 10T Differential –

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Abstract— **This paper compares readout powers and operating frequencies among dual-port SRAMs: an 8T SRAM, 10T single-end SRAM, and 10T differential SRAM. The conventional 8T SRAM has the least transistor count, and is the most area efficient. However, the readout power becomes large and the cycle time increases due to peripheral circuits. The 10T single-end SRAM is our proposed SRAM, in which a dedicated inverter and transmission gate are appended as a single-end read port. The readout power of the 10T single-end SRAM is reduced by 75% and the operating frequency is increased by 95%, over the 8T SRAM. On the other hand the 10T differential SRAM can operate fastest, because its small differential voltage of 50 mV achieves the high-speed operation. In terms of the power efficiency, however, the sense amplifier and precharge circuits lead to the power overhead. As a result, the 10T single-end SRAM always consumes lowest readout power compared to the 8T and the 10T differential SRAM.**

Index Terms—**SRAM, low power, non-precharge-type SRAM, two-port SRAM, differential port, video processing**

I. Introduction

As the ITRS Roadmap predicts, a memory area is becoming larger, and will occupy 90% of a system on a chip by 2013 [1]. For example, an H.264 encoder for a high-definition television requires, at least, a 500-kb memory as a search-window buffer, which consumes 40% of its total power [2]. As process technology is scaled down, a large-capacity SRAM will be adopted as a frame buffer and/or a restructured-image memory on a video chip. The large-capacity SRAM potentially dissipates a larger portion of a total power, and dominates a circuit speed. Therefore, low-power and high-speed dual-port SRAM is strongly required for video processing. In particular, the power and operating frequency in a read operation is crucial since the readout takes place more frequently than write-in in a video codec. For instance in a motion estimation, once picture data are written in memory, full-search algorithms or other motion compensation algorithms read out the data many times.

This paper compares three kinds of dual-port SRAMs in a 45-nm process technology. A dual-port SRAM is well utilized for video processing because a read and write accesses are possible at the same time. As the three kinds of dual-port SRAMs, we handle the conventional 8T SRAM, 10T SRAM with a single-end read port, and 10T SRAM with differential read ports. The next section describes their cell topologies.

II. Cell Topologies

A. 8T SRAM

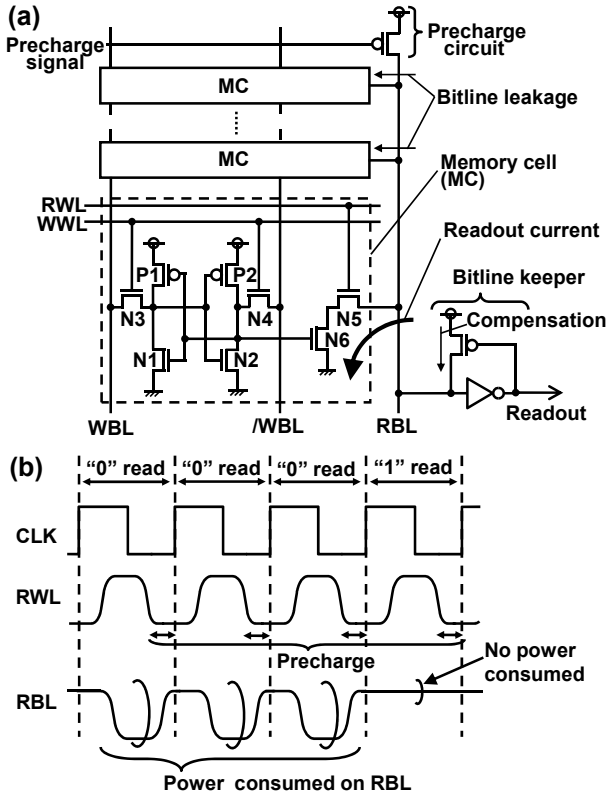

Fig. 1. The conventional 8T dual-port SRAM. (a) A schematic and (b) waveforms in read operation.

The conventional dual-port SRAM cell comprised of eight transistors (8T SRAM) [3] is shown in Fig. 1 (a). The 8T SRAM frees a static noise margin (SNM) in a read operation because it has a separated read port. Meanwhile, a precharge circuit must be implemented on a read bitline (RBL) so that the two nMOS transistors at the read port can sink a bitline charge to the ground. Thus, a certain power is dissipated by precharging (see Fig. 1 (b)). In addition to the precharge circuit, we have to prepare a bitline keeper on the RBL [4], which imparts negative influence on a readout time. To make the matters worse, the delay overhead becomes larger as a

supply voltage (VDD) decreases because of the bitline keeper.

B. 10T Single End SRAM (10T-S SRAM)

To improve the 8T SRAM, we have proposed a 10T non-precharge SRAM with a single-end read bitline [5], as depicted in Fig. 2 (hereafter, we call "10T-S SRAM"). Two pMOS transistors are appended to the 8T SRAM cell, which results in the combination of the 6T conventional cell, an inverter and transmission gate. The additional signal (/RWL) is an inversion signal of a read wordline (RWL); it controls the additional pMOS transistor (P4) at the transmission gate. While the RWL and /RWL are asserted and the transmission gate is on, a stored node is connected to an RBL through the inverter. It is not necessary to prepare a precharge circuit because the inverter fully charges/discharges the RBL.

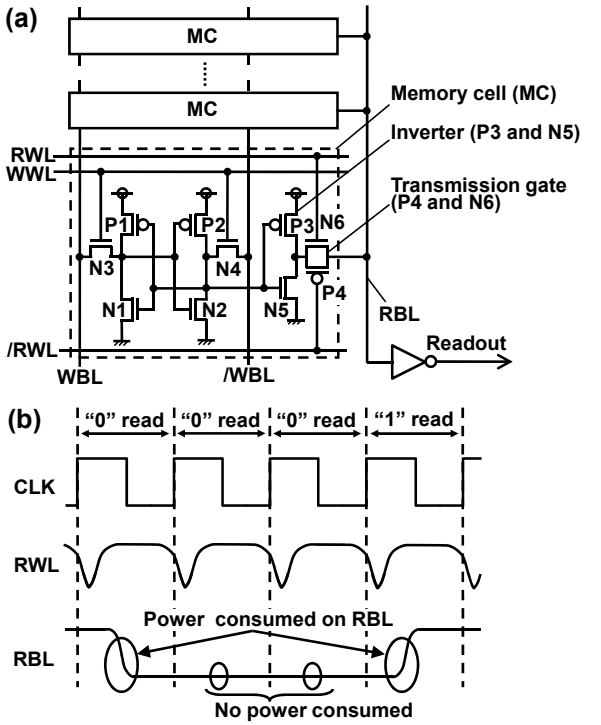

Fig. 2. The proposed 10T SRAM with a single-end read bitline (10T-S SRAM). (a) A schematic and (b) waveforms in read operation.

Fig. 2 (b) illustrates operation waveforms in the 10T-S SRAM in read cycles. A charge/discharge power on the RBL is consumed only when the RBL is changed. Consequently, no power is dissipated on the RBL if an upcoming datum is the same as the previous state. The 10T-S SRAM is suitable for a real-time video image that has statistical similarity [5].

The 10T-S SRAM reduces a bitline power in both cases that the consecutive "0"s and consecutive "1"s are read out. The charge and discharge power are consumed, only when a readout datum is changed. In the 10T-S SRAM, the transient probability on the RBL is 50% in a sequence of random data. In contrast, in an image, adjacent pixels have strong correlation to one-another, so the transient probability is more decreased than random data [5].

C. 10T Differential SRAM (10T-D SRAM)

Fig. 3 (a) shows a schematic of a 10T SRAM with differential read bitlines (RBL and /RBL) [6]. Two nMOS transistors (N5 and N7) for the RBL and the other additional nMOS transistors (N6 and N8) for /RBL are appended to the conventional 6T SRAM. As well as the 8T SRAM, precharge circuits must be implemented on the RBL and /RBL.

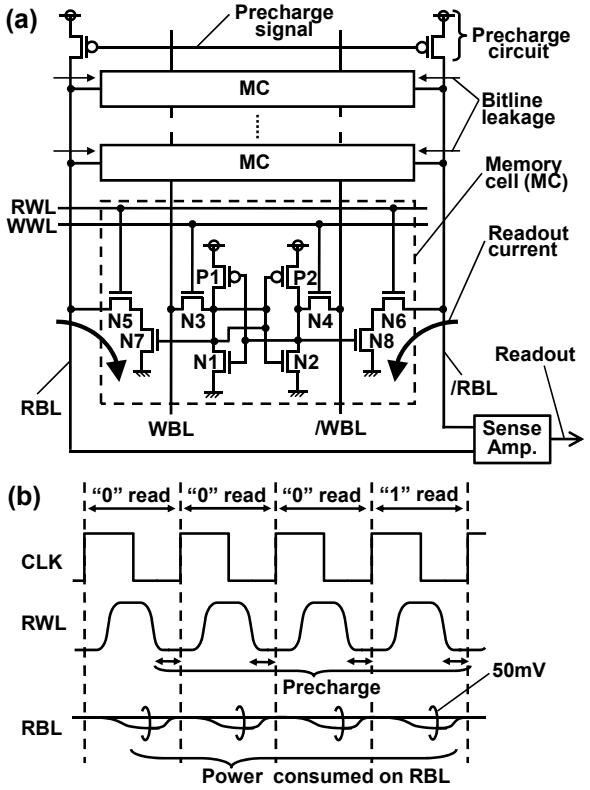

Fig. 3. 10T SRAM with differential read bitlines (10T-D SRAM). (a) A schematic and (b) waveforms in read operation.

Fig. 3 (b) depicts operation waveforms in the 10T-D SRAM in read cycles. The differential bitlines must be precharged to VDD by the start time of a clock cycle. To correctly sense a difference voltage between the RBL and /RBL, the difference voltage must be, at least, more than 50 mV [7-9].

III. Simulation Results

A. Cell and Macro Layouts

Fig. 4 portrays the layouts of the three kinds of dual-port SRAMs in a 45-nm process technology. The schematics were already shown in the previous figures. The areas of the 8T, 10T-S, and 10T-D SRAM cells are $1.55 \times 0.41\ \mu m^2$, $1.97 \times 0.41\ \mu m^2$, and $1.95 \times 0.41\ \mu m^2$, respectively.

We also designed 64-kb SRAM macros in the 45-nm process technology, for gate-level simulations. Fig. 5 shows the macro layouts. The core sizes of the 8T, 10T-S, and 10T-D SRAM macros are $260 \times 443\ \mu m^2$, $255 \times 550\ \mu m^2$, and $261 \times 547\ \mu m^2$, respectively. The 8T SRAM macro is the most area efficient because of the least transistor count. The 10T-D SRAM macro has, compared to the 10T-S SRAM, a 2% area overhead due to differential sense amplifiers and precharge circuits.

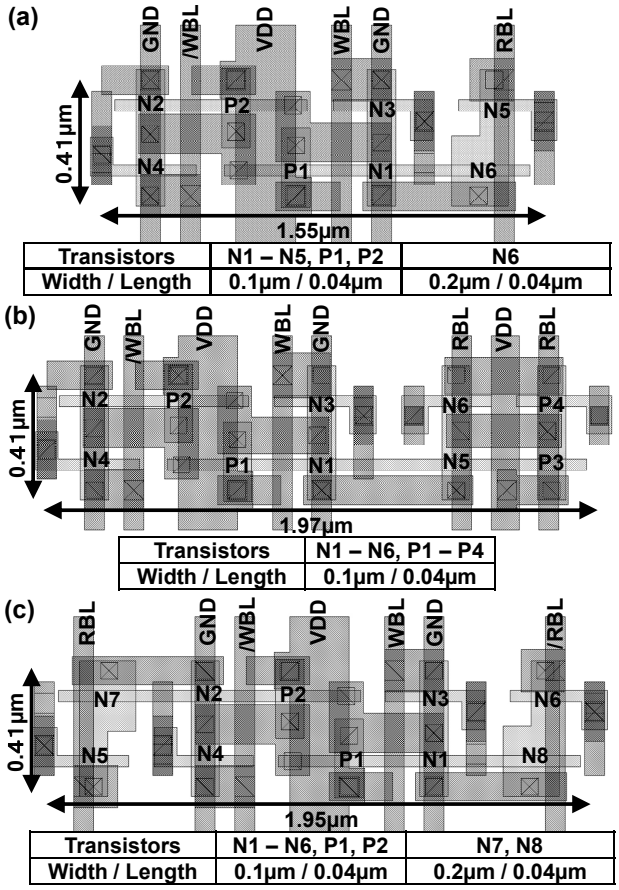

Fig. 4. Cell layouts of (a) 8T, (b) 10T-S, and (c) 10T-D SRAMs, in a 45-nm process technology.

B. Operating Frequency versus Supply Voltage

To obtain an operating frequency, we carried out Monte Carlo simulations, considering threshold voltage variation of each transistor. The number of Monte Carlo samples is 20,000.

Fig. 6 shows operating waveforms in the three kinds of SRAMs. In the figure, we adopt the SS corner model to simulate the worst-case delay. The followings are the criteria to calculate the access times:

- In the 8T SRAM, an access time is a period from a time at which an RWL rises to VDD/2 to a time at which an output of the sense amplifier is charged up to VDD/2.
- In the 10T-S SRAM, an access time is a longer one: a periods from a time at which an RWL rises to VDD/2 to a time at which an output of the sense amplifier is charged up to VDD/2, or a period from a time at which an RWL rises up to VDD/2 to a time that an output of the sense amplifier is discharged down to VDD/2.
- In the 10T-D SRAM, an access time is a period from a time at which an RWL rises to VDD/2 to a time at which a differential voltage between an RBL and /RBL is expanded to 50 mV, 100 mV or 200 mV.

In all the SRAMs, the worst cell with the worst threshold-voltage variation determines the delay. In particular, in the 10T-D SRAM, even if the sense point is set to 50 mV, most cells sink the bitline more than 50 mV.

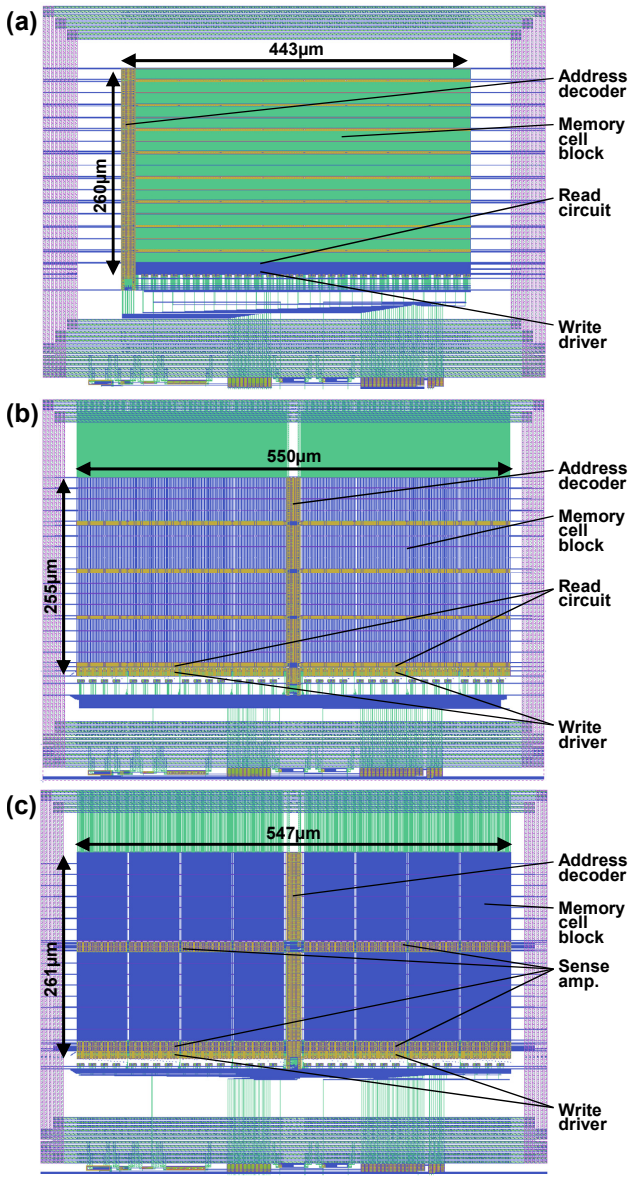

Fig. 5. Macro layouts of (a) 8T, (b) 10T-S, and (c) 10T-D SRAMs, in a 45-nm process technology. The total memory capacity of each macro is 64 kb.

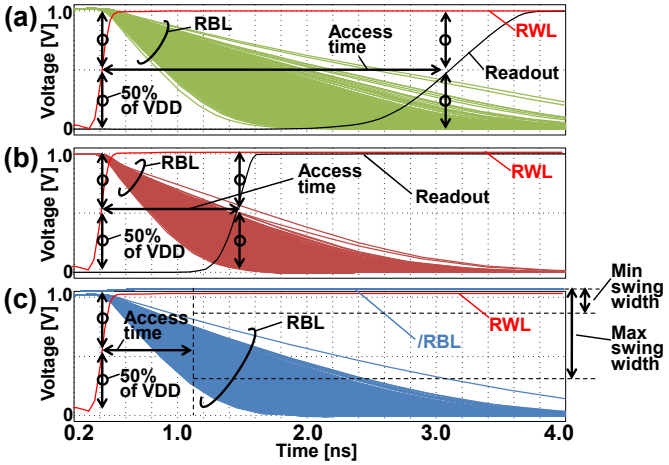

Fig. 6. Operation waveforms of (a) 8T, (b) 10T-S, and (c) 10T-D SRAMs at the SS corner (temperature = 25C°).

Fig. 7 shows the characteristics of the operating frequency when VDD is changed. The operating frequency is calculated as an inverse of a cycle time, which is a sum of a bitline charge/discharge time plus propagation delays in decoder circuits and a wordline. In this simulation of the operating frequency, the precharge periods in the 8T and 10T-D SRAMs are not taken into account because it can be completely overlapped with the decoder operation.

At a supply voltage of 1.0 V, the 8T, 10T-S and 10T-D SRAMs can run at 294 MHz, 572 MHz and 755 MHz, respectively. The 10T-D SRAM can operate fastest. The small differential voltage of 50 mV achieves the high-speed operation. The second fastest is the 10T-S SRAM. Although the additional transistor (P4) is appended in the 10T-S SRAM (see Fig. 2 (a)) and increases an RBL capacitance, the 10T-S SRAM is faster than the 8T SRAM because neither precharge circuit nor keeper circuit is needed.

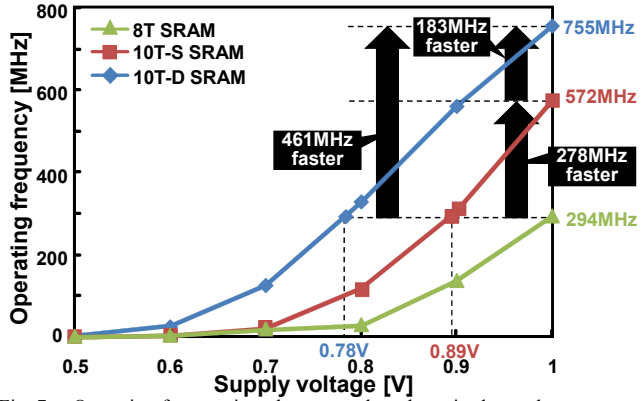

Fig. 7. Operating frequencies when a supply voltage is changed.

C. Power

Fig. 8 compares the readout powers in the 8T, 10T-S, and 10T-D SRAMs. Note that VDD is changed in the lines, according to Fig. 7. The 10T-S SRAM is not the fastest but the lowest power. This is because the transition possibility of the RBL is 50% when a sequence of random data is considered. On the other hand, in the 10T-D SRAM, the average voltage difference between the RBL and /RBL is 80% of VDD (= 0.8 V) as mentioned in the previous subsection, even if the sense point in the worst-case is set to 50 mV.

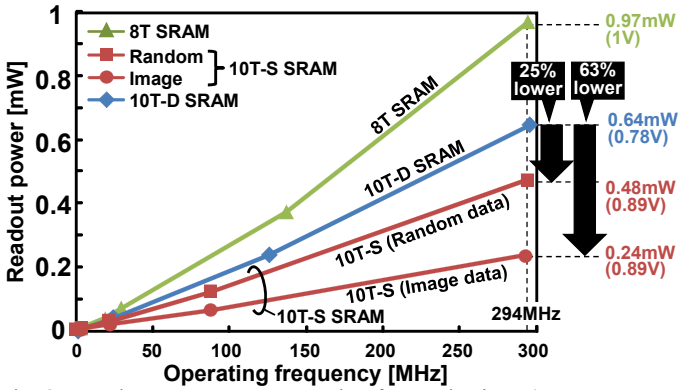

Fig. 8. Readout power versus operating frequencies in a 45-nm process technology.

The readout power in the 10T-S SRAM is 25 % lower than the 10T-D SRAM at the operating frequency of 294 MHz, when random data is considered. The saving factor is maximized to 63% if readout data has statistical similarly like H.264 reconstructed image data [5].

IV. Summary

In this paper, we clarified that the 10T SRAM with a single-end read port is the best as a dual-port SRAM in a 45-nm process technology. Although the conventional 8T SRAM has the least transistor count, and is the most area efficient, the readout power becomes large and the cycle time increases due to the keeper circuits on the read bitlines. The 10T differential-port SRAM can operate fastest. In terms of the power efficiency, however, even if the sense point is set to 50 mV, most cells sink the bitline more than 50 mV, which leads to the power overhead. As a result, the 10T single-end SRAM always consumes the lowest readout power of the three.

Acknowledgment

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