A 58-μW Single-Chip Sensor Node Processor Using Synchronous MAC Protocol

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Abstract

We propose a single-chip ultralow-power sensor node processor with a synchronous media access control (MAC). It is comprised of a transceiver, i8051 micro processor, and dedicated MAC processor. The test chip occupies 3 x 3 mm^2 in a 180-nm CMOS process, including 1.38 M transistors. The power is 58.0 μW under a network environment.

Keywords: Wireless sensor network, single-chip sensor node, synchronous MAC, low power

Introduction

A wireless sensor network (WSN) consists of many wireless sensor nodes, each of which is driven by a small battery. The sensor nodes obtain environmental information and send it to a base station with a multi-hopping scheme, under the severe energy constraint. For the power of the sensor node and its cost, it is necessary to be implemented on an LSI, so that we can extend the lifetime and achieve low cost in the entire system.

A low-power transceiver and a wireless SoC for a WSN have been reported [1-2]; [2] implements TICER [3] as a MAC, in which a sender node periodically repeats wakeups and sleeps in a preamble operation when establishing communication with receiver nodes (Fig. 1). In the figure, T is a receiver's wakeup period, and T_{on} is a carrier sense time; as T becomes larger, the power of TICER becomes larger, since a number of preambles must be tried.

I-MAC processor

To shorten the preamble time and save the needless energy, we propose the isochronous media access control (I-MAC), and implement it on a sensor node system LSI with a power management mechanism. The I-MAC is a synchronized MAC; it has a periodic wakeup time synchronized with the actual time [4]. The I-MAC in Fig. 1 synchronizes the wakeup times on the sender and receiver nodes. An internal timer keeps the time. To compensate time lag among sensor nodes, the flooding time synchronization protocol (FTSP) algorithm [5] is implemented by software, which suppresses the time lag within 250 μs. When the wake-up period is 100 ms, the I-MAC reduces 84.7% of communication over TICER.

Fig. 2 shows the block diagram of the proposed sensor node that includes a transceiver (TX/RX), microcontroller, and power management module (PMM). Fig. 3 is the state transition diagram of the I-MAC; it can be simplified because all nodes are synchronized and predict their operations. Hence, a simple processor for the I-MAC (MAC processor in Fig. 2) can be implemented as dedicated hardware. As well, the PMM controls the power supplies of the components, based on the state transition diagram. In our system, i8051 deals with only upper layers than the MAC layer (e.g. network layer and sensor input). Note that [2] implements TICER as a dedicated processor, but the chip is not integrated with an RF transceiver. We implement the I-MAC with a transceiver and PMM with it to reduce total power. The PMM is operated at 32.768 kHz and counts up the internal time. In a sleep state, only the PMM is activated.

Fully-integrated transceiver

The TX is comprised of a PLL and power amplifier (PA). Generally, it is difficult to increase output efficiency of a PA because transmitting power is small in a WSN. In [1], the output power efficiency is 16.5 % at 1.46 dBm using MEMS. We propose a higher-efficiency PA using an oscillator with multi-phase outputs. Fig. 4 shows the schematics of the proposed oscillator and combination with the PA. The multi-phase oscillator has four five-stage ring oscillators, connected by interpolators; 20-phase square waves are output at every 18 degrees. The PA has ten phase-modulated class-D amplifiers in parallel. Each class-D amplifier is controlled by other phases, which reduces short current through the PA in an active mode. Fig. 5 shows the relationship between the conduction angle and power efficiency. The maximum power efficiency achieves 17.9 % at 1.45 dBm without any MEMS or inductors.

In the RX part, we adopted a low-IF architecture. The I/Q mixer also exploits the multi phases for I/Q separation. A complex band-pass delta-sigma ADC converts the I/Q signals to quantized signals. Then, a digital image rejection filter selects a desired bandwidth. The image signal rejection is digitally-assisted without analog circuits. Fig. 6 shows the basis of the digital image rejection. $F_s/4$ frequency shifting is carried out by multiplying the 1, −1, j, −j by the I/Q signals; considering the I/Q signals in a discrete time domain, it equals multiplying by $e^{j(\pi/2)n}$ when n = 1/4. The manipulation can be achieved only by forwarding, inverting or changing the I/Q signals. This frequency shifting technique does not incur additional image signals in principle. Once the desired bandwidth is shifted, it can be filtered out by a low-pass filter (decimation filter); the decimation filter is concurrently used for decimation and image rejection. The image rejection ratio is 60 dB when the frequency shifting is set to 1 MHz. The digital image rejection filters can remove conventional SAW filters. As the final stage of the RX, the baseband DSP demodulates FSK. The RX achieves a bit error rate below 10^{-5} at a data rate of 60 kbps and at an SNR of 7.8 dB.

Verification on network

The power of each component is shown in Fig. 3. We verified the average energy in data-gathering operation on a network level using network simulator: QualNet [6]. Network simulation is very important to estimate power because nodes' powers are not uniform; a node near a base station consumes more power to process gathered data whereas a peripheral node that merely sends small data results in lower power. In the network simulation, the wake-up period is 100 ms, and the data rate is 20 kbps. Randomly-deployed 100 nodes in the area of 100 x 100 m^2 collect data to a base station at the center. The average operation time of each component in collecting the data is shown in Table 1. The wake-up ratio is 0.28%, and the proposed sensor node processor achieves a power of 58.0 μW on average. Table 2 shows the specifications of the sensor nodes. Fig. 7 depicts the chip micrograph. The test chip was fabricated in a 180-nm CMOS process and the area is 3 x 3 mm^2.

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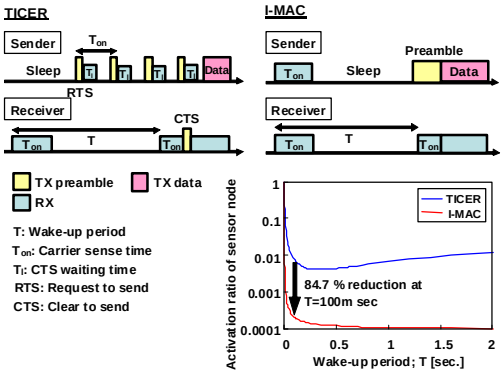


Fig. 1. Timing charts of TICER and I-MAC protocols.

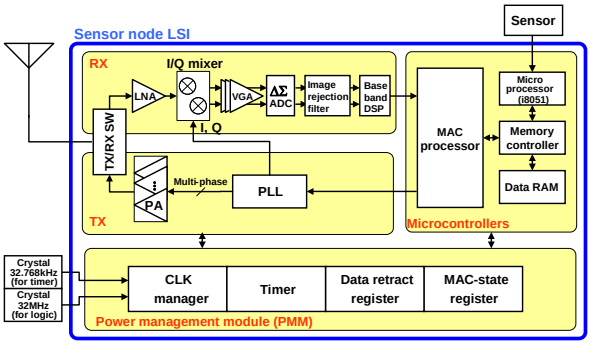
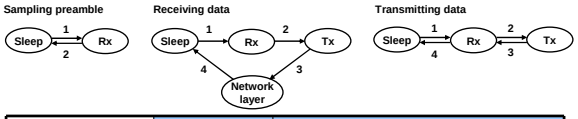


Fig. 2. Block diagram of proposed sensor node VLSI.



		Block power	State of a sensor node			
		Dynamic/Leak	Sleep	Tx	Rx	Network layer
LNA		1.17mW/-	OFF	OFF	ON	OFF
PA		4.26mW/-	OFF	ON	OFF	OFF
PLL		3.28mW/-	OFF	ON	ON	OFF
VGA		955μW/-	OFF	OFF	ON	OFF
ADC		999μW/-	OFF	OFF	ON	OFF
Image rejection filter		2.75mW/1.02μW	OFF	OFF	ON	OFF
Baseband		1.34mW/1.4μW	OFF	OFF	ON	OFF
MAC processor		11.7μW/135nW	OFF	ON	ON	ON
Memory controller		14.4μW/88.3nW	clk gating	ON	ON	ON
Data RAM		710μW/11μW	clk gating	read	write	read/write
i8051		787μW/8.2μW	OFF	OFF	OFF	ON
PMM		3.97μW/156nW	ON	ON	ON	ON
Crystal oscillator	32.768kHz	3.6μW/-	ON	ON	ON	ON
	32MHz	2.88mW/-	OFF	ON	ON	ON
Total power			7.73μW	11.16mW	14.12mW	4.41mW

Fig. 3. Power control by power management module.

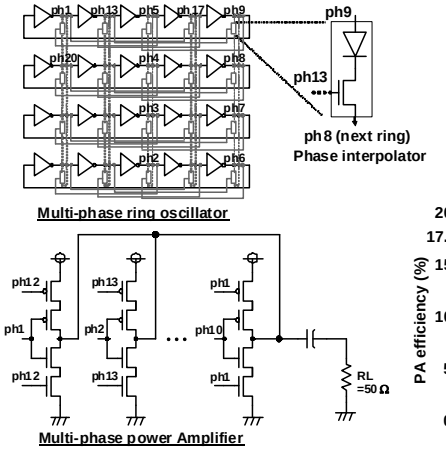


Fig 4. Multi-phase oscillator and power amplifier.

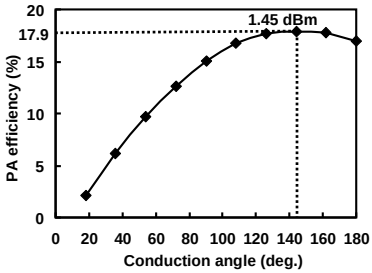


Fig 5. PA efficiency.

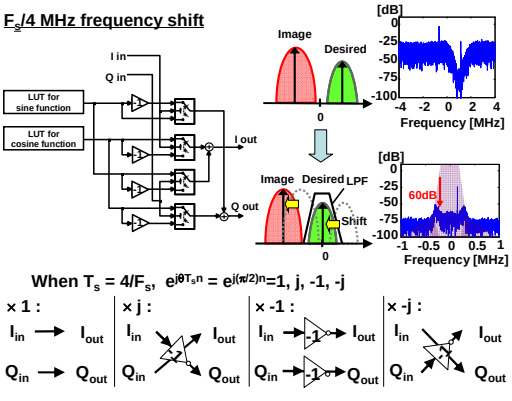


Fig. 6. Digital image rejection scheme using frequency shift.

Table1. Average operation time of sensor node.

Total time [ms]	84767.8
TX active time [ms]	22.5
RX active time[ms]	218
Sleep time [ms]	84527.0
wake-up ratio [%]	0.284

Table2. Performance parameters.

System		
Process	CMOS	180nm
Supply voltage	single supply	1.8V
Communication		0.1-20m
Carrier frequency		433.67-434.17MHz
Bitrate	variable per 10kbps	10-60kbps
Channel bandwidth		150kHz
Clock	Outer crystal oscillator	32.768kHz, 32MHz
Frequency tolerance	32.768kHz crystal osc.	+/- 20ppm
Modulation		FSK
Transceiver		
Transceiver	with Image rejection	Low-IF
Transmitter power		9.00mW
Receiver power		12.05mW
Output power		-4dBm
RX sensibility	For 1E-5 BER	-72.8dBm

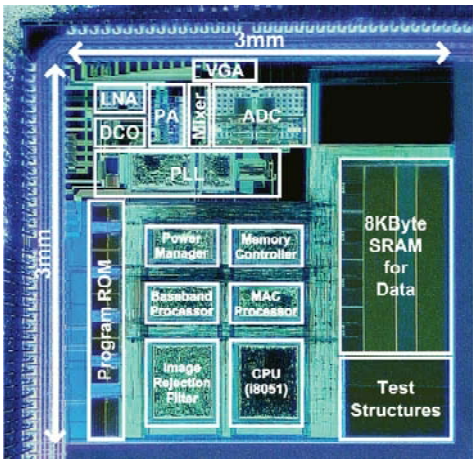


Fig 7. Chip micrograph.