A 58-μW Sensor Node LSI with Synchronous MAC Protocol

S. Izumi, T. Takeuchi, T. Matsuda, H. Lee, T. Konishi, K. Tsuruda, Y. Sakai,
C. Ohta, H. Kawaguchi, and M. Yoshimoto
Department of Computer and Systems Engineering, Kobe University
1-1, Rokkodai, Nada, Kobe, 657-8501 Japan
E-mail: shin@cs28.cs.kobe-u.ac.jp

Abstract

To shorten the preamble time and save the needless energy, we propose the isochronous media access control (I-MAC) [1], and implement it on a sensor node system LSI with a power management mechanism. Fig. 1 shows the block diagram of the proposed sensor node that includes a transceiver (TX/RX), microcontroller, and power management module (PMM). The state transition of the I-MAC can be simplified because all nodes are synchronized and predict their operations. Hence, a simple processor for the I-MAC can be implemented as dedicated hardware. As well, the PMM controls the power supplies of the components, based on the state transition of the I-MAC. The PMM is operated at 32.768 kHz and counts up the internal time. In a sleep state, only the PMM is activated. In our system, i8051 deals with only upper layers than the MAC layer.

The TX is comprised of a PLL and power amplifier (PA). We propose a higher-efficiency PA using an oscillator with multi-phase outputs. The multi-phase oscillator has four five-stage ring oscillators, connected by interpolators; 20-phase square waves are output at every 18 degrees. The PA has ten phase-modulated class-D amplifiers in parallel. Each class-D amplifier is controlled by other phases, which reduces short current through the PA in an active mode. The maximum power efficiency achieves 17.9 % at 1.45 dBm without any MEMS or inductors.

In the RX part, we adopted a low-IF architecture. The I/Q mixer also exploits the multi phases for I/Q separation. A complex band-pass delta-sigma ADC converts the I/Q signals to quantized signals. Then, a digital image rejection filter selects a desired bandwidth. The image signal rejection is digitally-assisted without analog circuits. The image rejection ratio is 60 dB. As the final stage of the RX, the baseband DSP demodulates FSK. The RX achieves a bit error rate below 10^{-5} at a data rate of 60 kbps and at an SNR of 7.8 dB.

The test chip was fabricated in a 180-nm CMOS process and the area is 3 x 3 mm^2. The power of each component is shown in Fig. 3. We verified the average energy in data-gathering operation on a network level using network simulator. In the network simulation, the wake-up period is 100 ms, and the data rate is 20 kbps. Randomly-deployed 100 nodes in the area of 100 x 100 m^2 collect data to a base station at the center. The wake-up ratio is 0.28%, and the proposed sensor node processor achieves a power of 58.0 μW on average.

References

[1] M. Ichien, et al., "Isochronous MAC using long-wave standard time code for wireless sensor networks," in Proc. of IEEE HUT-ICCE 2006, pp.172-177, Oct. 2006.
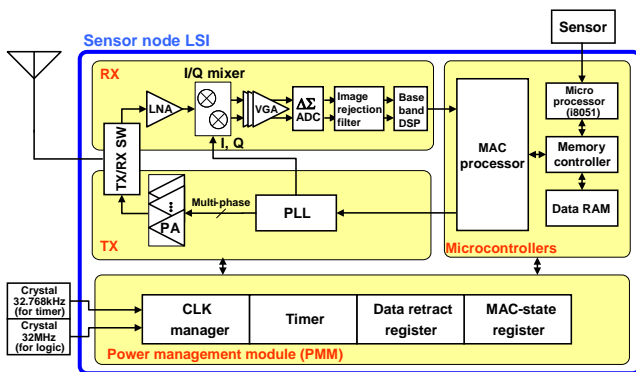
Figure 1: Block diagram of sensor node VLSI.

	Block power	State of a sensor node			
	Dynamic/Leak	Sleep	Tx	Rx	Network layer
LNA	1.17mW/-	OFF	OFF	ON	OFF
PA	4.26mW/-	OFF	ON	OFF	OFF
PLL	3.28mW/-	OFF	ON	ON	OFF
VGA	955µW/-	OFF	OFF	ON	OFF
ADC	999µW/-	OFF	OFF	ON	OFF
Image rejection filter	2.75mW/1.02µW	OFF	OFF	ON	OFF
Baseband	1.34mW/1.4µW	OFF	OFF	ON	OFF
MAC processor	11.7µW/135nW	ON	ON	ON	ON
Memory controller	14.4µW/88.3nW	clk gating	ON	ON	ON
Data RAM	710µW/11µW	clk gating	read	write	read/write
i8051	787µW/8.2µW	OFF	OFF	OFF	ON
PMM	3.97µW/156nW	ON	ON	ON	ON
Crystal oscillator 32.768kHz	3.6µW/-	ON	ON	ON	ON
Crystal oscillator 32MHz	2.88mW/-	OFF	ON	ON	ON
Total power		7.73µW	11.16mW	14.12mW	4.41mW

Figure 2: Chip micrograph.