A Process-Variation-Adaptive Network-on-Chip with Variable-Cycle Routers

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***Abstract*— As process technology is scaled down, a typical system on a chip (SoC) becomes denser. In scaled process technology, process variation becomes greater and increasingly affects the SoC circuits. Process variation strongly affects Network-on-Chips (NoCs), which have a synchronous network across the chip: its network frequency is degraded.**

As described herein, we propose a process-variation-adaptive NoC with a variation-adaptive variable-cycle router (VAVCR). The proposed VAVCR can configure its cycle latency adaptively, corresponding to process variation. It can increase the network frequency, which is limited by the slowest network component in a conventional router. The total execution time reduction of the proposed VAVCR is 14.9%, on average, for five task graphs.

***Index Terms*— Network-on-Chip, process variation, adaptive circuits**

I. Introduction

The minimum feature size of a CMOS process technology is scaled down, which enables higher density and lower chip cost. However, process variation is increasingly expanded by technology scaling. The expanded process variation strongly affects the SoC circuit characteristics. Network-on-Chip (NoC), which is emerging as a highly efficient network fabric for many-core processors [1], commonly adopts a synchronous design for a network overall across the chip. The NoC in a many-core processor has many network components, each of which is affected by process variation. The network component delays are varied considerably as the number of network components increases. Therefore, the frequency of the large-scale chip-wide synchronous network is degraded to the level of the slowest network component. Many studies have sought means to mitigate the variations of many-core processors using dynamic voltage and frequency scaling (DVFS), fine-grain body biasing (FGBB) [2], and dynamic voltage frequency-core scaling (DVFCS) [3]. However, they did not specifically address variation in a large-scale chip-wide synchronous network.

The contribution of this paper is a proposal for a process-variation-adaptive NoC using a variation-adaptive variable-cycle router (VAVCR). The proposed VAVCR can configure the cycle latency of the router in adaptation to the spatial process variation. Thereby, the NoC with the proposed VAVCR can increase the network frequency and the overall throughput.

II. Background

A. Process Variation

Technology scaling increases the threshold-voltage (V_{th}) variation of MOS transistors composed of die-to-die (D2D) and within-die (WID) variation, of which the WID variation is divided into systematic and random variations. This paper presents consideration of the WID variations because they affect characteristics of individual cores within a die, which turn out to be core-to-core (C2C) variations. Systematic variation is caused mainly by lens aberration and has a spatial correlation. Therefore, neighboring transistors have similar characteristics. In contrast, random variation is caused mainly by random dopant fluctuation (RDF) and line edge roughness (LER). Random variations show no spatial correlation. For that reason, individual transistors have different characteristics from their neighboring transistors.

B. Process Variation in NoC

Process variation in NoC shows up as variations in the operating frequencies of individual cores in NoC. Considering that synchronous designs for entire NoC processors in situations where the operating frequencies of each core vary, each core in the NoC must synchronize with the slowest core. Therefore, the throughput of the entire NoC processor degrades with increasing impact of process variation. Therefore, GALS designs in which the individual core and network fabric operate at their own maximum frequencies are widely adopted in NoC design. The network portion composed of routers, wires, and buffers is designed frequently with a single frequency and voltage domain [3] because the design of the network portion in NoC must be complicated and too costly when adopting the multi-frequency and multi-voltage design. However, when the network portion is with the single frequency and voltage domain, the network portion frequency is determined by the slowest components such as routers and buffers because operating frequencies of routers and buffers distributed across the entire chip are varied according to process variation. This issue is very important in a large-size NoC fabricated using a scaled process technology.

III. Impact of Variation on NoC circuits

A. Variation in the Processor Core

This section shows the impacts of process variation in the processor core. Assuming a 20 FO4 inverter delay as a single pipeline stage in the processor core to obtain the impacts of V_{th} variation in the operating frequency of processor core, we conducted Monte Carlo simulations using a SPICE circuit simulator at 65-nm process technology. Systematic variation of V_{th} arises as C2C variation. We use the standard deviation of systematic variation σ_{system}/μ = 6.3% from [4]. Random variation is apparent at individual transistors. Consequently, it affects all circuits in the core. We use standard deviations of random variation from actual measurement [5]. The standard deviations of random variation of PMOS and NMOS are, respectively, σ_{rnd_PMOS} = 43 mV and σ_{rnd_NMOS} = 28 mV (at L = 60 nm, W = 140 nm). Parameters used for the estimation of operating frequency are presented in Table I.

Fig. 2 shows the distribution of operating frequency obtained

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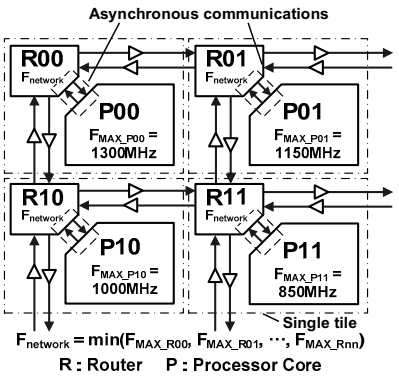

Figure 1. Operation frequency variations in NoC.

by simulations of 20 FO4 inverters. We set four frequency bins used at the evaluations in Sect. IV.C. The frequency bin details are presented in Table IV. Table II presents summary statistics of operating frequency of 20 FO4 inverters. From Fig. 2, the variation in operating frequency derived from V_{th} variation can be approximated as a normal distribution. Operating frequencies of 20 FO4 inverters show variation in 145.4 MHz/σ. Accordingly, it is apparent that individual processor cores in NoC under the V_{th} variation represent mutually different operating frequency characteristics.

B. Variations in On-Chip Networks

As described in Sec. II.C, to produce a single frequency domain for the entire network portion, the $F_{network}$ is degraded because all components of the network portion must be synchronized with the slowest one. In this section, delay variations of each pipeline stage of the router are evaluated. We used an open-source RTL of a router [6]. The router was synthesized using 65-nm process technology with Synopsys Design Compiler. The configurations of the router synthesis are shown in Table III. Then, the synthesized netlist was evaluated using a SPICE circuit simulator and the delay variations were obtained. As parameters for the variation, the Table I parameters are used as described in Sec. III.A. We assumed the link length between the nodes as 1 mm for the delay evaluation.

The evaluated result for the delays of each pipeline stage is depicted in Fig. 3. The upper bound (i.e. the worst delay) of each graph is assuming 99.7% of the whole. The longest delay of each pipeline stage is the virtual channel allocation (VA) stage. The delay of VA stage varies between 627 ps to 1319 ps.

IV. Proposed Variation-Adaptive Variable-Cycle Router

A. Process-Variation-Adaptive Variable-Cycle Router

In this section, a process-variation-adaptive variable-cycle router (VAVCR) is proposed. The proposed VAVCR can configure the cycle latency of the router corresponding to the spatial process variation. The VAVCR can realize a variation-adaptive NoC configuration. Fig. 4 presents timing diagrams of the conventional and proposed router pipeline. The values of the delays are brought from Fig. 3. Figs. 4(a) and 4(c) show the worst delay of each stage (i.e. the upper bound of the delay in Fig. 3). Figs. 4(b) and 4(d) show the best delay of each stage (i.e. the lower bound of the delay in Fig. 3).

TABLE I. Parameters for Operating Frequency Estimation

Technology	65-nm CMOS	σ_{system}	0.063 / μ_{Vth}
Process corner	TT	σ_{rnd_NMOS}	43 mV
Temperature	25℃	σ_{rnd_PMOS}	28 mV
# of Monte Carlo	10000		

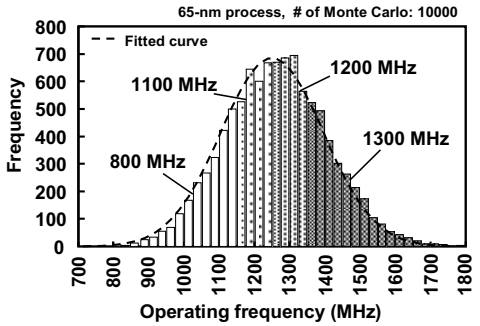

Figure 2. Distribution of operating frequency of 20 FO4 inverters. The dashed line signifies the fitted normal distribution curve.

TABLE II. Operating Frequency Statistics of 20 FO4 Inverters

$\mu_{frequency}$	1237.7 MHz	$\mu_{frequency} + 3\sigma_{frequency}$	1653.6 MHz
$\sigma_{frequency}$	145.4 MHz	$\mu_{frequency} - 3\sigma_{frequency}$	801.5 MHz
Maximum	1802.1 MHz	minimum	775.3 MHz

TABLE III. Parameters for Estimation of Router Pipeline Delay

Topology	4x4 mesh	# of VC	4
Flit size	64 bits	VC buffer size	4 flits
Routing	X-Y DOR	# of port	5 (NEWS and its node)
Router type	Speculative, look ahead		

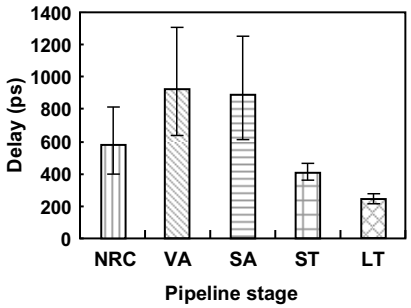

Figure 3. Delay of each pipeline stage: NRC, next routing computation; VA, virtual channel allocation; SA, switch allocation; ST, switch traversal; LT, link traversal. The upper bound (i.e. the worst delay) of each graph is assuming 99.7% of the whole.

Figs. 4(a) and 4(b) portray timing diagrams of the conventional router pipeline. The router frequency is determined by the worst delay (Fig. 4(a)). Accordingly, great amounts of slack emerge at router pipelines, which can operate on the best delay (Fig. 4(b)). This large amount of slack occur because of process variation. Consequently, the stronger the process variation, the greater is the slack which occurs at the router pipeline.

Figs. 4(c) and 4(d) portray timing diagrams of the proposed VAVCR pipeline. The VAVCR pipeline applies multi-cycle

paths to NRC, VA, and SA stages (Fig. 4(c)) when whichever delay of the pipeline stage exceeds the predefined cycle time. The cycle time is set to 1/1050 MHz in this example. At the case in which any delay of the pipeline stage does not exceed the predefined cycle time, the VAVCR pipeline does not apply the multi-cycle paths; it operates in the same way as a conventional pipeline, but at the higher frequency (Fig. 4(d)) compared with Fig. 4(b). Therefore, the proposed VAVACR pipeline can reduce the large slack at the conventional router pipeline, and can realize greater network throughput.

Fig. 5 portrays a distribution of the router cycle latency for 4×4 mesh network. The number in the circle represents the latency of the router. Figs. 5(a) and 5(b) respectively show the networks of the conventional router and proposed VAVCR. In the proposed VAVCR, the routers are configured as a three-cycle latency router or a four-cycle latency router corresponding to the spatial process variation in the chip. The pipeline delays of each router are measured in the burn-in test, and configured the cycle latencies at the fabricating lab. The network frequency (F_{network}) can be increased to 1050 MHz from 700 MHz by application of the proposed VAVCR.

B. Evaluation Methodology

We used BookSim simulator [7] to evaluate the entire NoC implemented with the proposed VAVCR. BookSim was modified to evaluate the proposed VAVCR. The router configuration is identical to that shown in Table III.

The spatial process variation is modeled using a simplified VARIUS model [4]. The spatial correlation parameter is assumed as $\Phi = 0.5$. We used a simple spatial process variation model that has the same V_{th} value within a single tile, which includes a processor core, router, and repeater buffers as shown in Fig. 1. Variation parameters of Table I are used as explained in Sec. III. In this evaluation, 100 different variation maps (chips) are assessed. The network frequency for the conventional router and proposed VAVCR are 700 MHz and 1050 MHz, respectively. The processor core frequencies are determined by the V_{th} variation map and the frequency bins in Table IV. Frequency bins are obtained using the evaluation in Sec. III.A. The router latencies of the proposed VAVCR are 4 cycles for frequency 0 and 1 bins, and 4 cycles for frequency 2 and 3 bins.

As the traffic pattern used in this evaluation, we used the standard task graph set (STG) [8] and TGFF [9]. For the STG, we used random (500 tasks, the task graph number is 0000), robot, sparse, and fpppp. We set the packet size of each edge as 16±8. For TGFF, we set parameters as follows: number of tasks; processing cycles of tasks; and packet sizes of 500, 3000±1500, and 32±16, respectively [10]. Each task in the task graph is assigned to the processor core based on the critical path method.

C. Evaluation

Figs. 6–10 present evaluation results of the conventional router and the proposed VAVCR. They signify the total execution times of a task graph. Each result contains the evaluation of 100 variation maps (chips). The execution times are normalized by the average of the evaluation result of the conventional router. The dashed and chained lines respectively indicate the average of the conventional router and the proposed VAVCR.

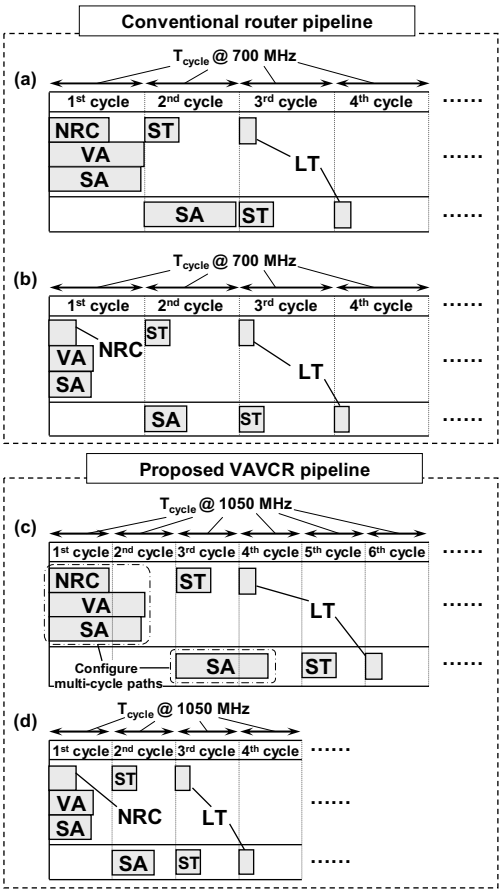

Figure 4. Timing diagrams of the conventional and proposed router pipeline. (a) and (c) show the worst delay of each stage. (b) and (d) show the best delay of each stage. (a) (b): Conventional router pipeline. The cycle time (T_{cycle}) of the entire NoC is determined by the worst delay. The frequency is 700 MHz in this example. (c) (d): Proposed VAVCR pipeline. (c): VAVCR applies multi-cycle paths to NRC, VA, and SA stage. The frequency is 1050 MHz in this example. (d): VAVCR can operate at a higher frequency than the conventional pipeline can ((b)).

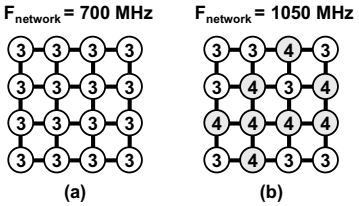

Figure 5. Distribution of the router latency for 4×4 mesh network: (a) conventional router and the (b) proposed VAVCR. The proposed VAVCR configures the latency of the routers corresponding to the spatial process variation.

TABLE IV. RATIOS AND FREQUENCIES OF THE FREQUENCY BIN AND ROUTER LATENCIES IN THE PROPOSED VAVCR

Frequency bin	Frequency 0	Frequency 1	Frequency 2	Frequency 3
Frequency	800 MHz	1100 MHz	1200 MHz	1300 MHz
Ratio	27.6%	25.8%	24.7%	23.2%
Router latency of the proposed VAVCR	4 cycles	4 cycles	3 cycles	3 cycles

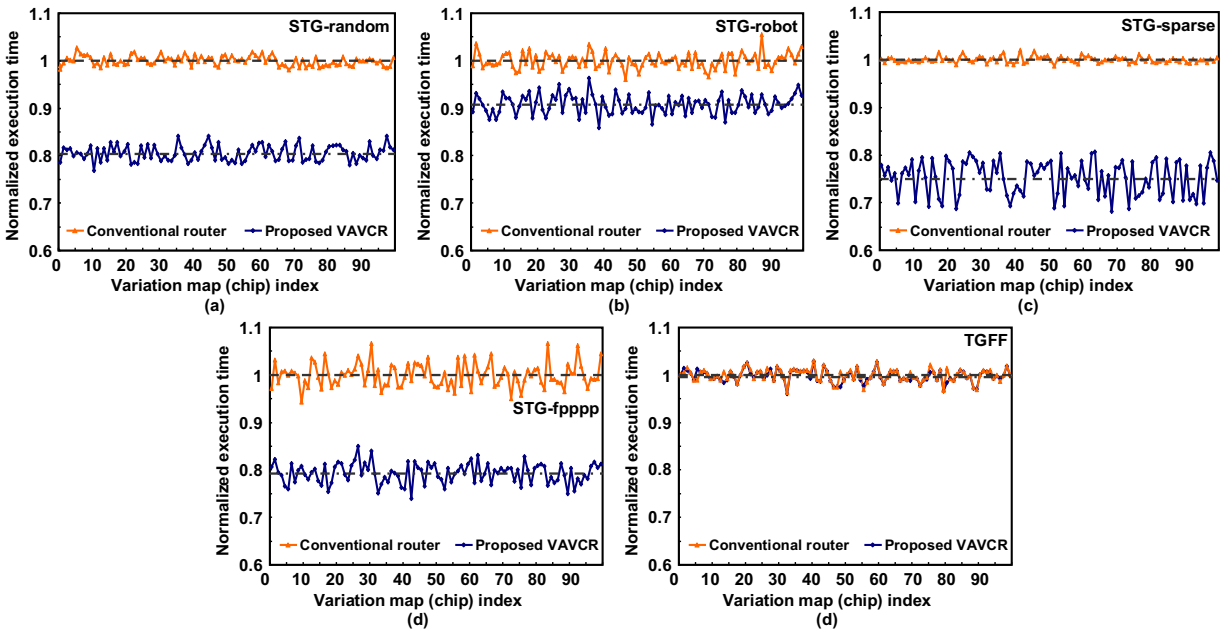

Figure 6. Normalized execution time: (a) STG-random, (b) STG-robot, (c) STG-sparse, (d) STG-fpppp, and (e) TGFF.

In Fig. 6, the proposed VAVCR is shown to reduce the total execution time of the STG-random by 19.5% on average. The packet latency of the STG-random was increased by 23.4% on average. The execution time was reduced mainly because of the increase in the network frequency. The packet latency of the STG-random was increased because of the existence of the four-cycle routers. Irrespective of the amount of the increase in the packet latency, the proposed VAVCR reduced the total execution time. Similarly, the proposed VAVCR reduced the total execution times of the STG-robot (Fig. 7), STG-sparse (Fig. 8), STG-fpppp (Fig. 9), and TGFF (Fig. 10) by 9.19%, 24.8%, 20.7%, and 0.201% on average, respectively. The packet latencies of the STG-robot, STG-sparse, STG-fpppp, and TGFF were increased by 20.3%, 16.3%, 12.6%, and 38.5% on average, respectively.

The proposed VAVCR can efficiently reduce the total execution time in executing the network-bound task such as the STG-random, STG-sparse, and STG-fpppp. In contrast, the proposed VAVCR reduces it inefficiently when executing the computation-bound task such as TGFF.

Table V presents a summary the reductions of the total execution time, the increases in the packet latency, the standard deviations of the total execution time of the conventional router, and the proposed VAVCR. They are 14.9%, 22.2%, 1.42%, and 2.14% on average of the five task graphs, respectively.

TABLE V. EVALUATION RESULTS OF 100 VARIATION MAPS (CHIPS)

	Reduction of the total execution time	Increase in the packet latency	σ_{exec_time} of conv.	σ_{exec_time} of prop.
STG-random	19.5%	23.3%	1.01%	1.63%
STG-robot	9.19%	20.3%	1.65%	2.03%
STG-sparse	24.8%	16.3%	0.63%	3.62%
STG-fpppp	20.7%	12.6%	2.53%	2.13%
TGFF [17]	0.201%	38.5%	1.33%	1.3%
Avg. of 5 TGs	14.9%	22.2%	1.42%	2.14%

V. CONCLUSION

As described in this paper, we proposed a process-variation adaptive NoC with a variation-adaptive variable-cycle router, VAVCR. The proposed VAVCR can adaptively configure its cycle latency corresponding to a spatial process variation, and increases the network frequency that is limited by the slowest network component in the conventional router. The proposed VAVCR can reduce the total execution time 14.9%, based on an average of the five task graphs.

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