Bit Error Rate Estimation in SRAM Considering Temperature Fluctuation

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Abstract

SRAM performance varies depending on the operating environment. This study specifically examines the bit error rate (BER) when considering temperature fluctuation. The SRAM performance is generally determined using a read margin because a half-select issue must be considered even in a write operation. As a metric of the SRAM's performance, we also adopt a static noise margin (SNM) with which we evaluate three methods to estimate the BER considering temperature fluctuation. Method 1 iterates calculations for the SNM many times with Monte Carlo simulation. BER is defined as the number of cells that have no margin. Method 2 includes the assumption that SNM forms a normal distribution. Its BER is defined as a probability distribution function. Method 3 includes the assumption that SNM is determined as either square but not the smaller one of the two squares. The BER estimations are compared with a test chip result implemented in a 65-nm CMOS technology: Method 2 has 11.10% and Method 3 has 4.09% difference (unfortunately, Method 1 has no data missing because of a lack of simulations). The shift of the minimum operating voltage between the low and high temperatures is 0.04 V at a 128-Kb capacity when the temperature fluctuates from 25°C to 100°C.

Keywords

SRAM, bit error rate, static noise margin, temperature fluctuation

1. Introduction

Recently, LSIs have been widely used in various environments. The LSI performance varies depending on the operating environment. The SRAM characteristics are also affected by the environment. Herein, we specifically examine the bit error rate (BER) of the SRAM when considering temperature fluctuation. The BER can be a metric determining a minimum operating voltage (V_{min}) of the SRAM if the SRAM capacity is known. It is necessary to estimate the BER during a design phase for maintaining SRAM reliability. In the SRAM, the read margin decreases at high temperature, although a write margin has the opposite characteristics [1]. We estimate the read performance using a static noise margin (SNM) because the operating margin of the SRAM is determined by the read margin [2]. A half-select issue must be considered even for the write operation.

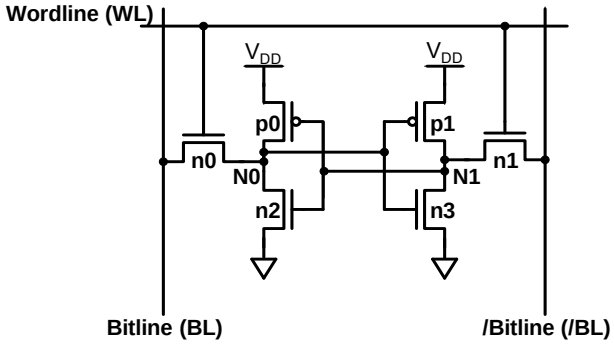

Figure 1: Schematic of a 6T bitcell.

Figure 1 depicts a schematic of a commonly used six-transistor (6T) bitcell. The 6T bitcell consists of load transistors (p1 and p0), access transistors (n0 and n1), and drive transistors (n2 and n3). The SNM is obtainable from *butterfly curves*, which physically represent a metric of the read operation stability [3]. The butterfly curves reflect the two inverters' and access transistors' characteristics [4]. The SNM is described in the next section.

As explained herein, we verify three BER estimation methods and compare measured BER with results of these estimation methods considering temperature fluctuation.

2. Temperature Dependences in SRAM

2.1. Transistor characteristics

First, we must understand the temperature characteristics of a transistor to consider their impacts on the SNM. The main temperature-dependent parameters are a threshold voltage (V_{th}) and mobility (μ) [5]. The temperature dependence can be expressed as

$$V_{th}(T) = V_{th}(T_0) - \alpha(T - T_0) \text{ and} \quad (1)$$

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m}, \quad (2)$$

where T signifies a temperature, T_0 stands for a reference temperature, α denotes a temperature coefficient, and m represents a process-dependent parameter (ca. 2). Both V_{th} and μ decrease with T. Furthermore, the drain current (I_{ds}) changes along with the temperature fluctuation. In a saturated region, I_{ds} is

$$I_{ds}(T) = \frac{\beta}{2}\mu(T)(V_{gs} - V_{th}(T))^2, \quad (3)$$

where β is a transistor coefficient [6]. I_{ds} is affected differently by either V_{th} or μ. A lower V_{th} increases I_{ds}, but a lower μ decreases it. I_{ds} decreases with T because μ gives

more impact on I_{ds} if V_{gs} (voltage between the gate and source) is high (although I_{ds} increases with T if V_{gs} is low).

2.2. Static noise margin and bit error rate

The temperature dependence of the SNM can be described based on the transistor characteristics (particularly V_{th} and I_{ds}). To estimate SNM, two bitlines (BLs) and a wordline (WL) are connected to a supply voltage (V_{DD}). In this state, the voltage of the other node (N1) is rapidly decreased from a certain point if a voltage of an internal node (N0) is forced to be increased to V_{DD} from the ground. Figure 2 presents this drop voltage (V_{drop}), which depends on V_{th} of n3. Similarly, the other curve of V_{N0} (N0's voltage) is obtainable by changing V_{N1} (N1's voltage). These two curves form butterfly curves with two eyes. The smaller square inscribed in the eyes is generally defined as an SNM. The SNM depends on V_{DD} and I_{ds} [7]. If a bitcell has no SNM, then it is an unreadable cell. The ratio of unreadable cells to overall SRAM capacity is the BER, which is an important metric for estimating the minimum operating voltage (V_{min}). In fact, the temperature fluctuation and BER affect V_{min}.

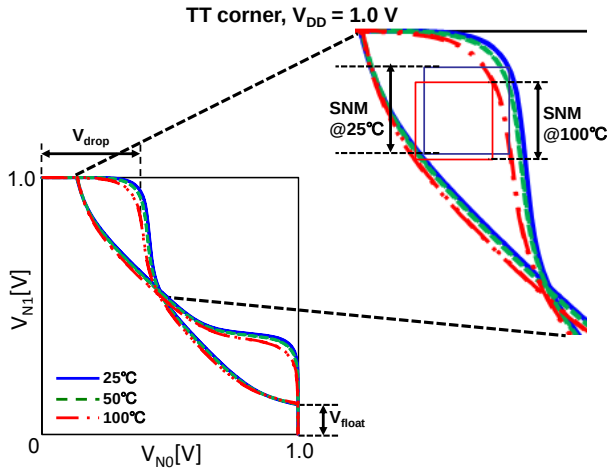

Figure 2: SNM at each temperature at V_{DD} = 1.0 V.

In Figure 2, at V_{drop}, V_{N1} is pulled down by n3 in a saturated region. As the temperature increases, V_{N1} decreases considerably. When V_{N0} is V_{DD}, V_{N1} is not turned off completely. Therefore, it floats a little (= V_{float}). As V_{drop} does, V_{float} also depends on I_{ds} of n3, and increases with T at a high V_{DD}. Actually, V_{float} decreases with T at a low V_{DD}. Consequently, SNM has temperature characteristics. The figure presents an example of SNM when V_{DD} = 1.0 V.

3. Voltage dependence of SNM

In an earlier section, it was explained that SNM has temperature dependence. In addition, SNM has voltage dependence [7]. To estimate BER, we obtain the trends of μSNM and σSNM (average and standard deviation of the SNM) at each temperature (25°C, 50°C, 75°C, and 100°C). The voltage characteristics of the SNM were investigated using Monte Carlo (MC) simulation at those temperatures. The MC trials were 1000; V_{DD} was 0.6–0.8 V, varying at intervals of 0.02 V. Figure 3 presents simulation results.

μSNM degrades linearly according to the operating voltage. Its slope shows similar dependence. This trend exhibits the models of V_{th}, μ, and I_{ds} respectively in (1), (2), and (3). In contrast, σSNM is constant irrespective of the voltage and temperature [8]. The σSNM dependence of the voltage and temperature is negligible. Based on the discussion presented above, μSNM and σSNM corresponding to a voltage and temperature can be estimated easily by sampling a few simulations.

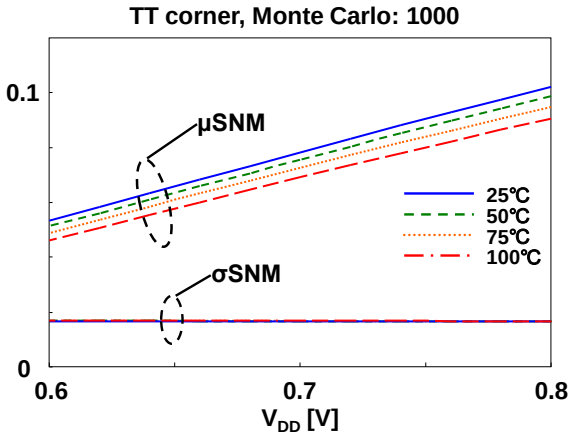

Figure 3: μSNM and σSNM at respective temperatures.

4. BER Estimation Methods

We verify three BER estimation methods. Method 1 calculates the SNMs many times with the MC simulation. Its BER is defined as a percentage of cells that have no SNM. Method 2 assumes that the SNM forms a normal distribution. Its BER is defined as a probability that the SNMs are less than zero. Method 3 is almost identical to Method 2 except for the SNM definition. For Method 3 SNM is determined as another side of the two squares but not a smaller one.

Method 1 is accurate if the SRAM capacity is less than the number of MC trials, but this means that a 10-Kb SRAM requires tens of thousands of MC trials to estimate its BER at a condition set of a voltage and temperature. More simulation time is needed for more SRAM capacity, which is increasing with a process technology trend. Figure 4 presents the distribution of the SNMs in Methods 2 and 3. "Worst" corresponds to Method 2, and "Left" (or "Right") signifies Method 3. Table 1 presents average, standard deviation, and skewness of the distributions.

Method 2 can save simulation time because this does not require many iterations of the MC trials. It is sufficient to obtain the average and standard deviation of the SNM by running simulations a thousand times; the computation cost is less than a tenth of that for Method 1. However, the SNM distribution does not follow a normal distribution strictly (Figure 4; Table 1). The definition of the "Worst" SNM in Figure 4 and Table 1 takes a smaller square in both, but the "Worst" case spreads lower than the "Left" and "Right" cases. This can be recognized as skewness in the table, which signifies a large negative value: the "Worst" case distribution is asymmetry. Consequently, estimating the

SNM distribution is difficult when using the standard deviation model.

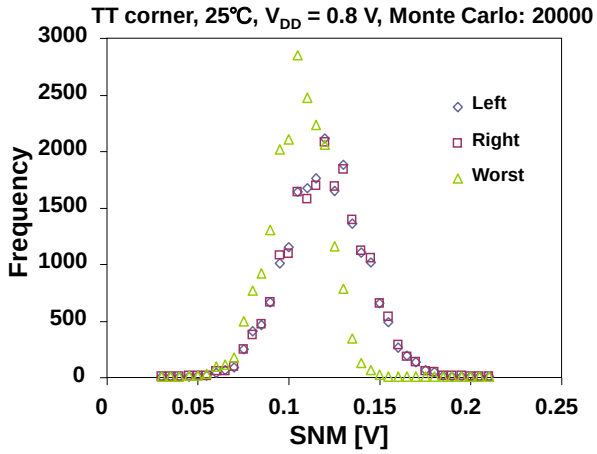

Figure 4: SNM distributions. "Left" and "Right" evaluate only either square. "Worst" evaluates both squares.

Table 1: Average, standard deviation, and skewness of the three distributions

	Left	Right	Worst
Average [V]	0.1176	0.1179	0.1034
S.D. [V]	0.0209	0.0212	0.0157
Skewness	0.0032	0.0034	–0.3320

Method 3 uses only either square. The SNM distribution is assumed as a normal distribution, although this method does not represent an adequate margin of a cell. However, at a very low SNM, the "Worst" case can be estimated as twice of "Left" or "Right" (or a sum of "Left" and "Right") because the event of the very low SNM is rare.

Figure 5 presents probability density distributions of the three methods. The MC trials are conducted 20000, 1000, and 1000 times, respectively, in Methods 1, 2, and 3. The distribution in Method 2 does not follow that of Method 1 because its distribution is skewed. However, Method 3 fits with Method 1.

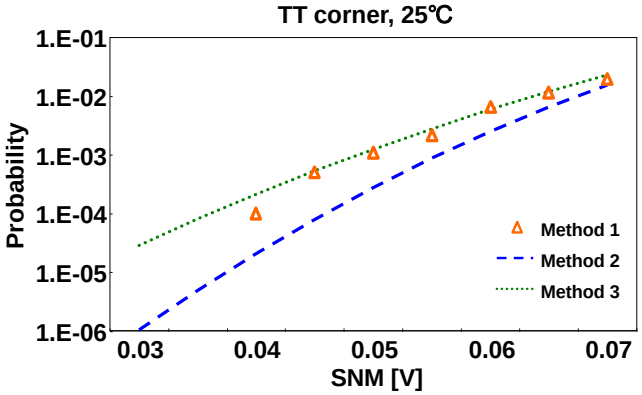

Figure 5: Probability density distributions of three methods.

5. Measurement Results

5.1. Implementation

We implemented a 1-Mb SRAM in a 65-nm CMOS process to measure a BER. Figure 6 displays a chip layout. The SRAM configuration is 16-Kb block × 64 blocks, which equals 1-M bits. The bitcell has a standard 6T topology. Transistor sizing is $\beta = 2$ and $\gamma = 1$, where β denotes the ratio of a drive transistor to an access transistor, and γ represents the ratio of an access transistor to a load transistor.

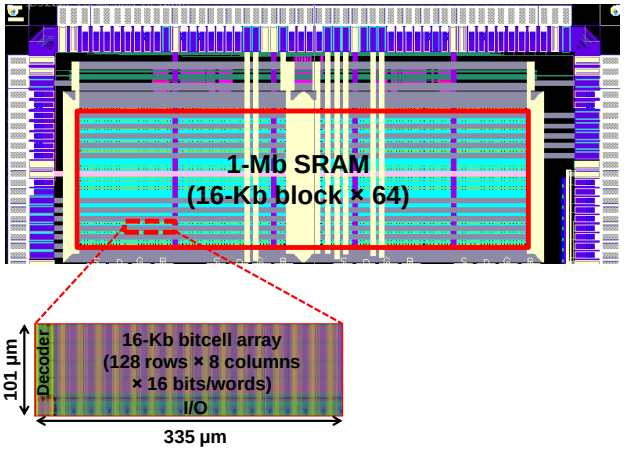

Figure 6: Layout of a 1-Mb SRAM.

5.2. Bit Error Rates

We compare the BERs of estimation using the three methods with the measured BER. Figure 7 presents the results of comparison. In both the simulations and measurements, the temperature condition is 25°C. The other conditions are the same as those described in Section 4. Assuming that the SNM is a normal distribution, μSNM and σSNM are calculable in Methods 2 and 3. The SNM probability density function becomes the following.

$$f(SNM) = \frac{1}{\sqrt{2\pi}\sigma SNM} \exp\left\{-\frac{(SNM - \mu SNM)^2}{2\sigma SNM^2}\right\} \quad (4)$$

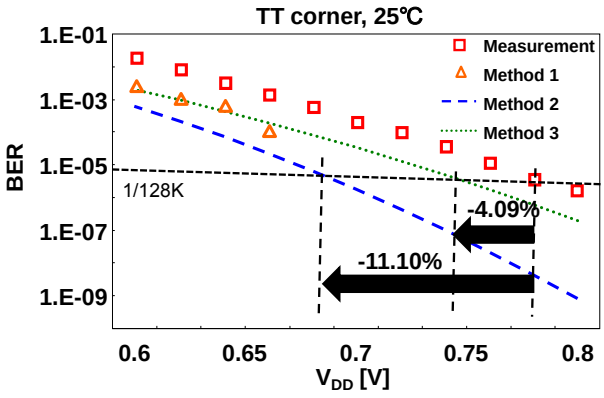

Figure 7: BER Comparison.

The simulated BER is the probability at which the calculated SNM is less than zero. Data in Method 1 cannot be shown at a lower BER region because of the iteration of the MC simulation. The BER slope in Method 2 does not fit to the measurement because its SNM distribution is skewed and not a normal distribution. The BER in Method 3 is the closest to the measurement. The simulated BER still has an error compared with the measurement, which is regarded as a mismatch of the simulation model.

In addition, the simulated V_{min} has an error between the measurement and each method. At a capacity of 128 Kb, the respective errors of Methods 2 and 3 to the measurement are 11.10% and 4.09%. In Method 2, the error will increase more with the SRAM capacity.

Temperature characteristics of the BER were measured using a thermograph streamer. Figure 8 portrays the measured BERs and estimated ones in Method 3. These results show that Method 3 is useful to estimate the BER dependence on the temperature and voltage. The read operation margin is degraded at high temperature. Furthermore, V_{min} becomes higher. The measured V_{min} shift (ΔV_{min}) is 0.04 V at a BER of 1/128K when the temperature changes from 25°C to 100°C. The estimated ΔV_{min} using Method 3 is as much as 0.04 V, which demonstrates that the BER slope in Method 3 matches that of the measurement.

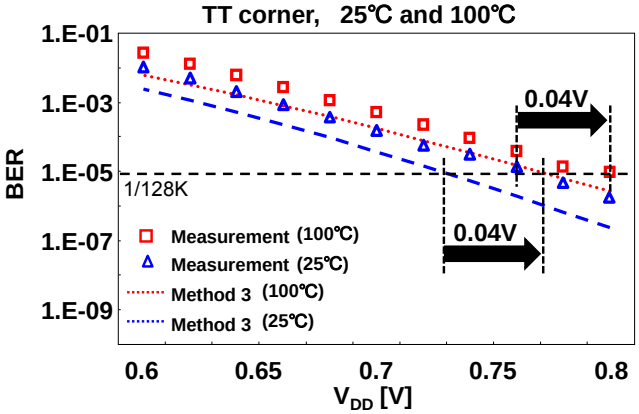

Figure 8: BERs with temperature fluctuation.

6. Conclusion

Recently, advanced technology enables increasingly large capacity SRAM. The verification and simulation of SRAM performance are require enormous time as increased the memory capacity. .This study also verify about the SRAM performance depending on the temperature. We estimate characteristics corresponding temperature fluctuation. To obtain tendencies of average and standard deviation of SNM enabled to get BER without enormous time simulation. We implemented a 1-Mb SRAM chip in 65-nm CMOS technology and confirmed the accuracy of three methods. About Method 2 and Method 3, the difference value of V_{min} is 11.10 % and 4.09 % respectively. Compared BER of Method 3 with measurement result, ΔV_{min} is same values, and is both 0.04 V at 128-Kb capacity when temperature fluctuates from 25°C to 100°C. Furthermore, it is confirmed that BER slope corresponding temperature fluctuation is estimated exactly. Furthermore, ΔV_{min} is predictable with increasingly memory capacity using Method 3. We confirmed most suitable method which can estimate BER shift depending on the temperature, and the method does not need enormous time simulation.

Acknowledgments

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