A 40-nm 256-Kb 0.6-V Operation Half-Select Resilient 8T SRAM with Sequential Writing Technique Enabling 367-mV VDDmin Reduction

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Abstract

This paper introduces a novel half-select resilient dual write wordline 8T (DW8T) SRAM with a sequential writing technique. The process scaling increases random variation that degrades SRAM operating margins, for which the proposed DW8T cell presents two features: half-VDD precharging write bitlines and dual write wordlines. The dual write wordlines are sequentially activated in a write cycle, and its combination with the half-VDD precharge suppresses the half-select problem. The DW8T SRAM with the sequential writing technique improve a half-select bit error rate by 71% at the disturb worst corner (FS, 125°C) and by 79% at a typical corner (CC, 25°C) over the conventional 8T, respectively. We implemented a 256-Kb DW8T SRAM and a half-VDD generator on a single chip in a 40-nm CMOS process. The measurement results of the seven samples show that the proposed DW8T SRAM achieves a VDD_{min} of 600 mV and improves the average VDD_{min} by 367 mV compared to the conventional 8T SRAM. The measured leakage power can be reduced by 25%.

Keywords

SRAM, 8T, disturb, half-select

1. Introduction

CMOS technology scaling increases random and systematic variation [1]. To date, the SRAM is the most sensitive device to the variation because of its large capacity and minimum sizing [2]. The high-yield requirement for the classic 6T SRAM makes the cell size larger because the 6T cell has a tradeoff between the static noise margin (SNM) and the write noise margin (WNM) in nature [3]. Dual port 8T cells have been proposed to free the SNM/WNM tradeoff with its dedicated read port, which enables lower-voltage operation than 6T SRAMs [4]. The 8T cells, however, have a half-select problem, which is a disturbance to unselected cells in a write cycle [5] as illustrated in Fig. 1. The half-selected cell in the unselected column is disturbed because the 8T cell is usually comprised of minimum sizing transistors and the β ratio is one; the cell content might be flipped when the write wordline (WWL) is activated for turning on all the access gates in the horizontal direction. In this paper, a novel sequential writing technique is proposed: dual write wordlines mitigate the half-select disturbance in an 8T SRAM.

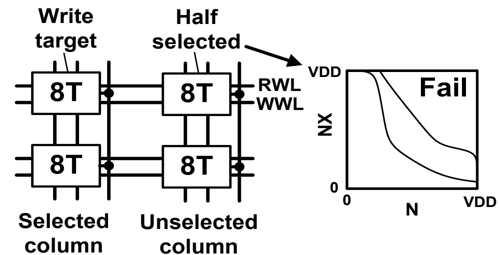

Figure 1: Half-select problem in a write cycle in a 8T SRAM.

A dual wordline 6T cell has been proposed for a stable read operation [6]. The 6T cell in this literature is asymmetrically designed to enlarge its SNM with a single-ended readout. The single-ended 6T cell, however, has disadvantages in the half-select margin and the write margin because of the asymmetrical nature.

This paper is organized as follows. Section 2 provides the sequential writing technique for the proposed dual write wordline 8T (DW8T) SRAM. In Section 3, measurement results about VDD_{min} (minimum operating voltage) and operating power will be shown by using 256-Kb test chips in a 40-nm CMOS process. Section 4 summarizes this paper.

2. Sequential Writing Technique for Dual Write Wordline 8T SRAM

Figure 2 presents a schematic of the proposed DW8T cell and the concept of the sequential writing technique. In the proposed DW8T cell, the write bitlines (WBLs) are precharged to a half of the supply voltage (a half VDD), which decreases the disturbing currents through the WBLs. The proposed 8T cell has two WWLs: they are called "dual write wordlines" in this paper and are sequentially activated in a write cycle. The sequential writing technique eliminates one of the two disturbing currents flowing from a high-state node to WBL and from WBLN to a low-state node. Utilizing the half-VDD precharging WBLs and the dual write wordlines, the proposed scheme mitigates the half-select problem.

Figure 3 shows waveforms of the conventional and proposed 8T cells in the half-selected situation. In a write operation, the conventional 8T cell is disturbed by the noise current from a write bitline to a low-state node. On the other hand, the proposed DW8T cell is disturbed by either of the two disturbing currents mentioned above: one is from a high-state node and the other is to a low-state node.

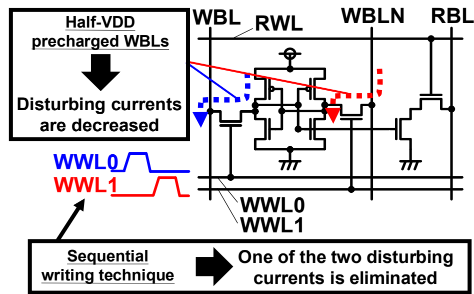

Figure 2: The proposed dual write wordline 8T (DW8T) cell and novel sequential writing technique.

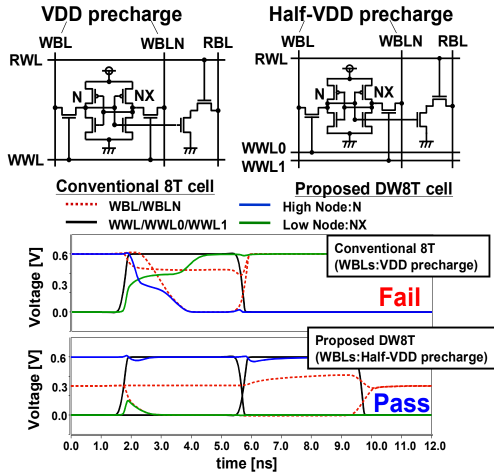

Figure 3: Waveforms of the conventional 8T cell and the proposed DW8T cell when half-selected in a write cycle.

The proposed sequential writing technique can separate the two disturbing currents because the dual write wordlines are sequentially activated in the proposed DW8T cell. The disturbing current in the DW8T is suppressed lower than the conventional 8T and its SNM is improved because the WBLs are precharged to a half VDD.

Figure 4 presents a comparison of the SNMs in the conventional and proposed 8T cells when no variation is considered. The butterfly curves for the proposed DW8T, however, become asymmetric because either of the access gates is merely asserted. The proposed scheme improves the SNM to 86 mV from 68 mV (18 mV = 26.5% improvement).

Figure 5 shows the simulated bit error rates (BERs) of the conventional 8T, DW8T and DW8T with a negative WBL scheme. The both DW8Ts use the proposed sequential writing technique. The DW8T (without the negative WBL) has disadvantages in the write margin due to the proposed sequential write technique; in the write worst corner (SF, -40°C), the write BER of the DW8T is degraded by 1.5 orders of magnitude, compare with the conventional 8T. Therefore, we adopt negative WBL scheme [7] to improve the write margin. The negative bitline level is -0.1 V (20% of VDD). The BERs of the DW8T with the negative WBLs are limited by the half-select margin at the disturb worst corner (FS, 125°C) and a typical corner (CC, 25°C),

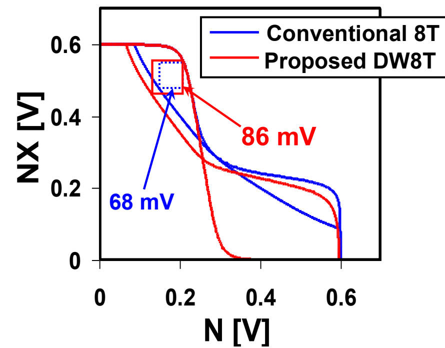

Figure 4: SNM comparison between the conventional 8T cell and the proposed DW8T cell (CC corner, 25°C).

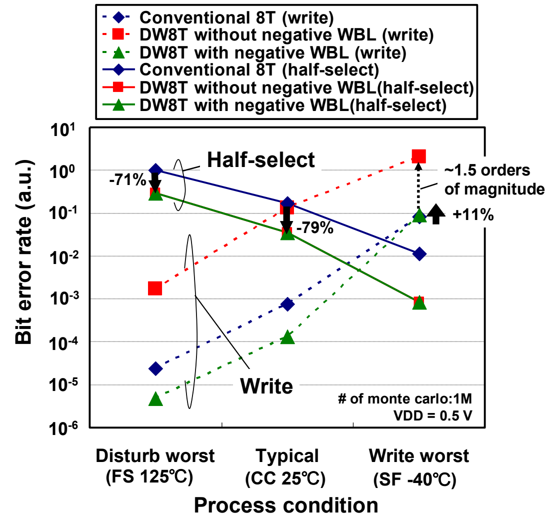

Figure 5: Simulated BERs of the conventional 8T SRAM, DW8T SRAM, and DW8T SRAM with negative WBLs.

whereas at the write worst corner, its BER is indeed limited by the write margin. The DW8T improves the half-select BER by 71% at the disturb worst corner and by 79% at the typical corner over the conventional 8T, respectively. Its write BER is degraded by 11% at the write worst corner; however it is not the global worst point. The performance in terms of BER is restricted by the disturb worst corner in our design.

3. Experimental Results

We designed a 256-Kb DW8T SRAM test chip in a 40-nm CMOS process. We also implemented half-VDD generators on the chip [8]. Each 8-Kb SRAM block has a half-VDD generator. Figs. 6(a) and 6(b) portray the schematic and the layout of the half-VDD generator. The layout size is 35 × 5 μm^2. The area overhead is less than 0.5% in the 256-Kb SRAM macro.

Figure 7 shows the measured output voltages of the half-VDD generators in three test chips implemented in the CC corner. In the output range of 0.2 V to 1.1 V, the output voltage follows the half VDD within an error of -45 mV to +35 mV at room temperature (RT).

Figure 8 portrays the measured half-select BERs of the conventional 8T SRAM and the proposed DW8T SRAM

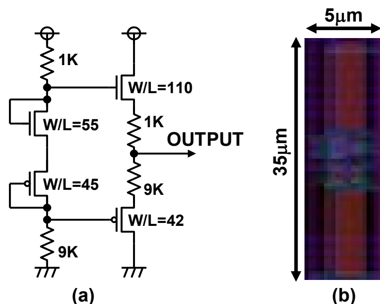

Figure 6: (a) Schematic and (b) layout of the half-VDD generator [8].

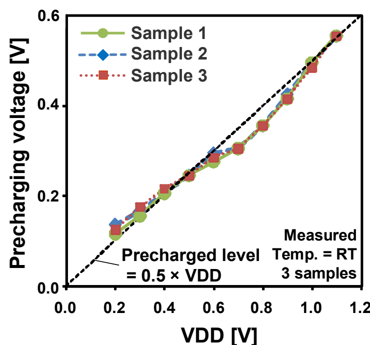

Figure 7: Measured output voltages of the half-VDD generators in three test chips. The nominal VDD is 1.1 V.

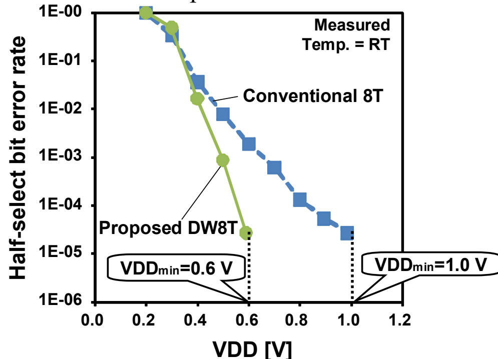

Figure 8: Measured half-select BERs of the conventional 8T SRAM and the proposed DW8T SRAM (best chip). The operating frequency is 10 MHz.

with the sequential writing technique on the best chip. The measurement result of the conventional 8T SRAM was obtained by reusing the proposed DW8T SRAM; the dual write wordlines are simultaneously controlled in a similar manner and the WBLs are precharged to VDD in this case. The precharge level can be changed to an arbitrary value on the test chip. The measurement results show that the proposed DW8T SRAM with the sequential writing technique can operate at a VDD_{min} of 0.6 V and can improve the VDD_{min} by 0.4 V on the best chip.

By using seven test chips, we also measured the VDD_{min}'s of the conventional 8T SRAM and the proposed DW8T SRAM. Figure 9 shows the data from the seven samples. The number six is the best chip mentioned above. The VDD_{min} is improved by 367 mV (from 1.019 V to 0.652 V) on average in the proposed DW8T SRAM.

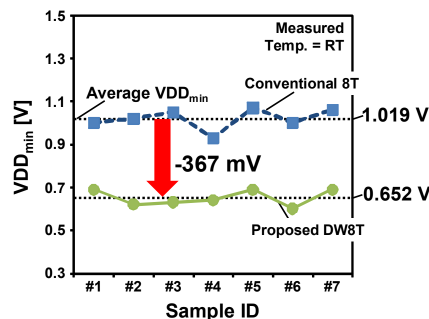

Figure 9: Measured VDD_{min}'s of the coventional 8T SRAM and the proposed DW8T SRAMs. #6 is the best chip.

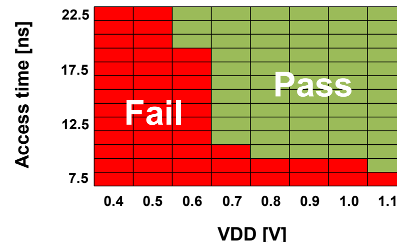

Figure 10: Shmoo plot of the proposed 256-Kb DW8T SRAM.

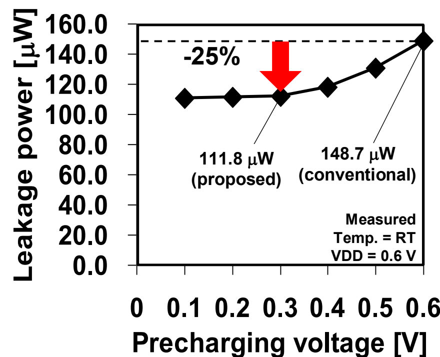

Figure 11: Measured leakage power in the proposed DW8T SRAM when a precharging voltage is changed.

Figure 10 portrays a Shmoo plot of the access time and VDD. The operation is restricted by a read operation rather than the write operation. So, we confirmed that the proposed scheme does not affect its access time although the proposed DW8T has the dual write wordlines to be sequentially activated. The best chip can operate at an access time of 20.0 ns even when the VDD is 0.6 V. The access time at the nominal VDD of 1.1 V is 8.5 ns.

The leakage power was measured in the standby mode as shown in Fig. 11. The VDD and the operating frequency were set to 0.6 V and 10 MHz, respectively. In the figure, the precharging voltage on the WBLs are changed to a half VDD (= 0.3 V) in the proposed scheme. The leakage power is decreased by 25%, compared with the conventional 8T SRAM. The leakage power is decreased with a precharging voltage because bitline leakage is accordingly reduced.

We also investigated area overheads; the proposed 8T SRAM requires an additional WWL and an extra driver for it to implement the sequential writing technique. The additional WWL can be laid out without any area overhead

Table 1: Configurations of the implemented test chip.

Technology	40-nm CMOS Process
Chip size	2.5 mm × 2.5 mm
SRAM macro size	900 μm × 1420 μm
Capacity	256 Kbit
SRAM organization	16 bits/word × 512 words × 32 blocks
Cell area	0.6679 μm^2 (logic rule)
# of cells / bitline	64
Performance (Access time @ VDD)	8.75 ns @ 1.1 V, 20.0 ns @ 0.6 V (=VDD_{min})

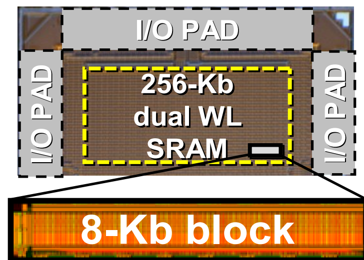

Figure 12: Die photograph of the test chip.

in the given process, whereas the extra WWL driver occupied some area. The area overhead for the extra WWL driver is, however, small because it merely drives either of the access gates in the proposed DW8T cell and the capacitance is small (usually, the conventional SRAM drives the two access gates, which has to be designed twice larger). Consequently, the area overhead for the dual write wordline drivers is only 2.3% in the SRAM macro. The area overhead derived from the negative WBL scheme is 2%. The proposed DW8T cell area is 0.6679 μm^2 on a logic rule basis, which is 21% larger than the classic 6T cell (the same size as that of the conventional 8T cell).

The configurations of the test chip are summarized in Table II. The chip size is 2.5 × 2.5 mm^2, and the 256-Kb SRAM macro is 900 × 1420 μm^2. The SRAM macro is comprised of 16 bits per word × 512 words × 32 blocks. A die photograph is presented in Fig. 12.

4. Summary

In this paper, we proposed a novel DW8T SRAM with the sequential writing technique that can mitigate the half-select problem. A half-VDD generator was designed to precharge WBLs for decreasing disturbing currents. The proposed sequential writing technique further eliminates one of the two disturb currents, which improves the half-select margin better. DW8T with sequential writing technique improves the half-select BERs by 71% at the disturb worst corner and 79% at the typical corner compared with the conventional 8T, respectively. We implemented the 256-Kb DW8T SRAM macro and the half-VDD generator on a single chip in a 40-nm CMOS process. The measured output voltage of the half-VDD generator shows good dependence on the VDD from 0.2 V to 1.1 V within an error of -45 mV to +35 mV. The VDD_{min} of the proposed 256-Kb DW8T SRAM is improved by 367 mV on average among seven sample chips. The best chip operates at a VDD_{min} of 600 mV. The proposed half-VDD precharging WBLs improves the leakage power by 25%, compared with the conventional 8T SRAM.

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