NMOS-Inside 6T SRAM Layout Reducing Neutron-Induced Multiple Cell Upsets

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***Abstract*—This paper presents a novel NMOS-inside 6T SRAM cell layout that reduces a neutron-induced MCU SER on a same wordline. We implemented a 1-Mb SRAM macro in a 65-nm CMOS process and irradiated neutrons as a neutron-accelerated test to evaluate the MCU SER. The proposed 6T SRAM macro improves the horizontal MCU SER by 67–98% compared with a general macro that has PMOS-inside 6T SRAM cells.**

Keywords; SRAM; soft error rate (SER); multiple cell upset (MCU); neutron particle; twin well; triple well;

I. INTRODUCTION

Nanoscaled integrated circuits are susceptible to particle-induced soft error effect (SEE) because of their low signal charge and noise margin [1–3]. Particularly multiple cell upsets (MCUs), which are defined as simultaneous errors in more than one memory cell induced by a single event, have been closely scrutinized. The MCUs are caused by a collection of charges produced by secondary ions in neutron-induced nuclear reaction. The ratio of the MCUs to single-event upsets (SEUs) is increasing drastically in nanoscaled SRAMs [4–6]. Process-scaling reportedly causes multiple MCU modes: charge sharing among memory storage nodes, bipolar effect in a P-well, and multi-coupled bipolar interaction (MCBI) [7]. In the literature, fail bits are spread over about a 1000 × 1000 bit area in 22-nm SRAM design; it is apparently impossible to correct multiple bit upsets (MBUs = MCUs in the same word) merely by error correction coding (ECC) [8].

Respective Figs. 1 and 2(a) show a schematic and layout of a general 6T SRAM cell with a 65-nm CMOS logic rule. In the design, the sizes of the transistors are relaxed to suppress threshold voltage variation so that the cell area is about twice as large as a commercial 65-nm 6T cell [9]. The 6T cell consists of PMOS load transistors (PL0, PL1), NMOS driver transistors (ND0, ND1) and access transistors (NA0, NA1). A wordline (WL) and two bitlines (BL, BLN) are horizontally and vertically connected among cells, respectively. In the layout of the general 6T cell, the PMOS transistors are sandwiched by the NMOS transistors; this structure is called an NMOS-PMOS-NMOS (NPN) layout in this paper. On the other hand, the proposed 6T cell is designed as a PMOS-NMOS-PMOS (PNP) layout in Fig. 2(b). The PNP 6T cell can lower a horizontal MCU rate because we have observed that an NMOS has a four-times larger SEU cross section than a PMOS for a wide range of supply voltages (see Fig. 3) [10–11]. Furthermore, in the PNP layout, the NMOSes are horizontally separated from adjacent ones.

In this paper, we present horizontal MCU improvement of the PNP 6T layout with 65-nm 1-Mb SRAM test chips. The SRAMs are designed in both of twin-well and triple-well structures because well engineering drastically affects the MCU SER [12-13]. We will show experimental results that the proposed layout improves the horizontally MCU SER by 67–98% in the both of the twin- and triple-well structures. The novel layout enhances effectiveness of single error correcting - double error detecting ECC (SEC-DED ECC).

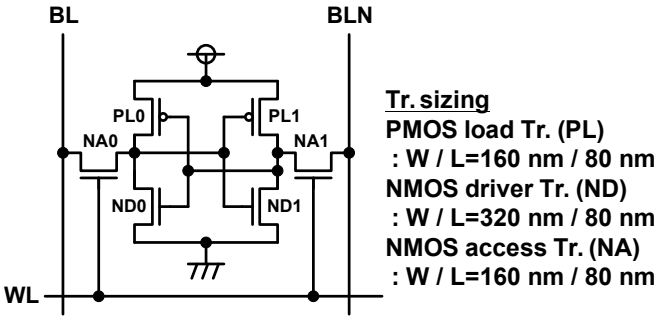

Figure 1. Schematic of 6T SRAM cell.

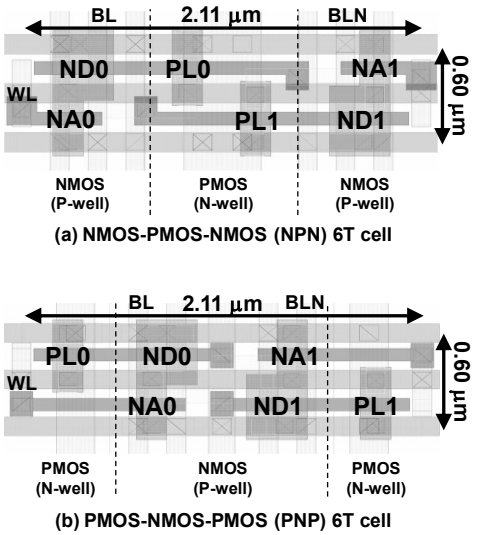

Figure 2. Layouts of (a) general NMOS-PMOS-NMOS (NPN) 6T cell and (b) novel PMOS-NMOS-PMOS (PNP) 6T cell designed with a 65-nm logic rule.

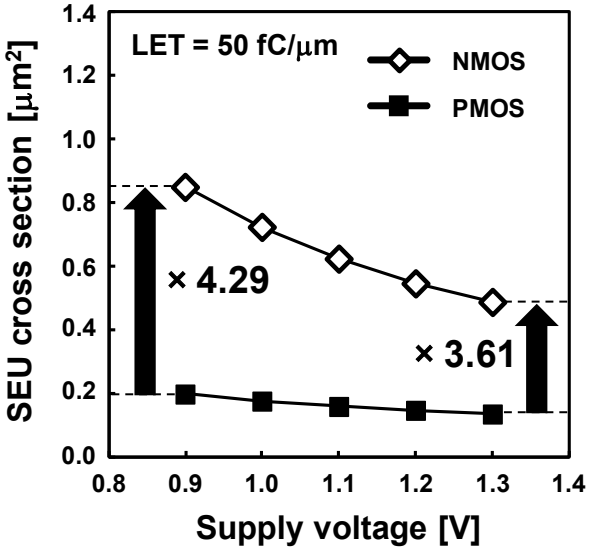

Figure 3. SEU cross sections of NMOS and PMOS with a twin-well 65-nm process calculated using the iRoC TFIT simulator [10].

II. SRAM DESIGN

We designed and fabricated a 1-Mb SRAM test chip consisting of 256-Kb macros of four types (NPN layout with twin well, PNP layout with twin well, NPN layout with triple well (Fig. 4), and PNP layout with triple well), as presented in Fig. 5(a). Additionally, Fig. 5(b) illustrates the block diagram of a 16-Kb block (128 columns × 128 rows). The SRAM macros using the four-type 6T cells occupy same areas so that the SRAM macros share same peripheral circuits. In the two macros with the triple-well structures, the memory cells are merely allocated in the triple well; the peripheral circuits are on the twin well. In the memory cells on the triple-well structure, the deep N-well narrows the area of the P-well; thereby the parasitic bipolar effect increases the MCU SER.

Fig. 6 presents a layout of the implemented SRAM cell arrays and well taps. The NPN and PNP 6T cells designed by the 65-nm logic rule have 2.11 × 0.60 μm^2 area (see Figs. 1 and 2; the gate length is relaxed to 80 nm to suppress variation). The well taps are inserted every 32 cells (= 19.2 μm) in the vertical direction. Since the memory cell incorporates the Metal-1 layer as internal connections, the vertical Metal-2 and horizontal Metal-3 layers are assigned as BLs and WLs.

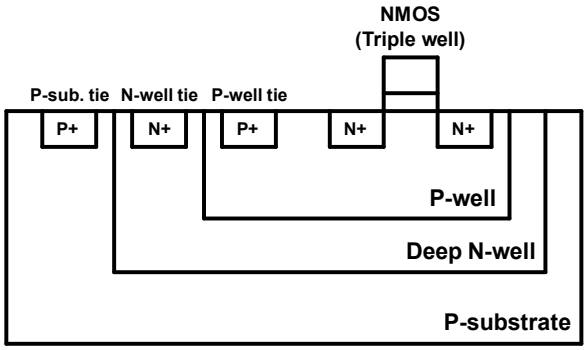

Figure 4. Cross section of NMOS when using triple well.

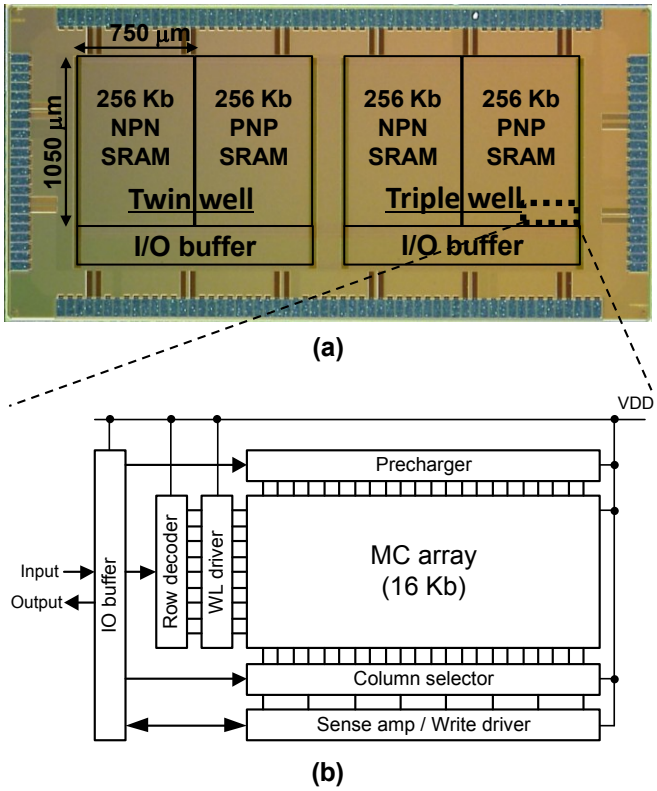

Figure 5. (a) Micrograph of a 1-Mb SRAM test chip including NPN and PNP SRAMs with twin and triple wells. (b) Block diagram of a 16-Kb block.

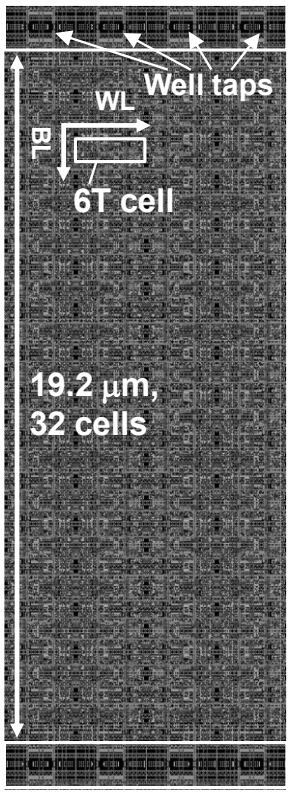

Figure 6. Layout of memory cell array and well taps.

III. Experimental Results

Fig. 7 presents an experimental setup for a neutron-accelerated test. The neutron irradiation experiment is conducted at The Research Center for Nuclear Physics (RCNP), Osaka University. Spallation neutron beam generated by a 400-MeV proton beam irradiates a measurement board 7892-mm far from a tungsten target, on which three sample chips are placed in a measurement board, for 30 hrs. The neutron flux is normalized to 13 cph / cm^2 above 10 MeV at ground level in New York City [14]. Fig. 8 shows a timeline of an FPGA on the measurement board. The FPGA automatically generates input data pattern to the SRAM macro before the irradiation and finally outputs addresses of the fail bits.

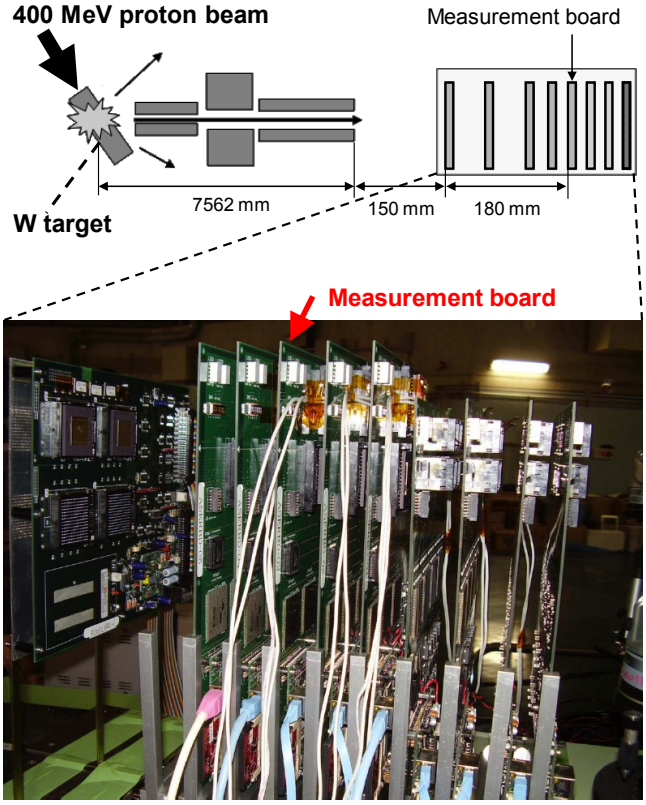

Figure 7. Setup for neutron-accelerated test.

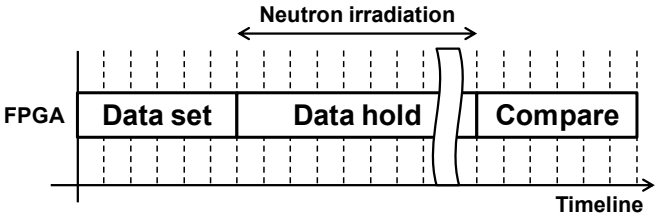

Figure 8. Timeline of the FPGA on the measurement board.

Fig. 9 portrays measurement results of single-bit-upset (SBU) SERs when a checkerboard (CKB) pattern is used. The supply voltage is varied from 0.6 V to 1.2 V to assess the dependence of the SERs on the supply voltage. Results show that the SBU SERs were ranging from 500 FIT / Mb to 1400 FIT / Mb depending on the supply voltage, but no apparent difference on the SBU SER is observed among the four layouts.

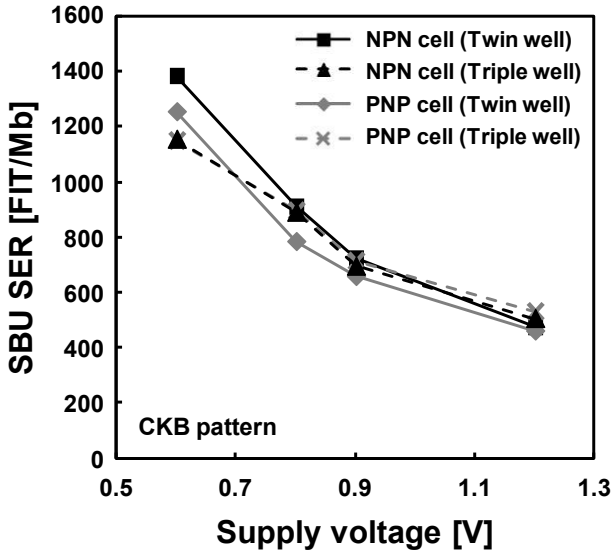

Figure 9. Measured neutron-induced SBU SERs in the CKB pattern at 0.6-1.2 V (four layouts).

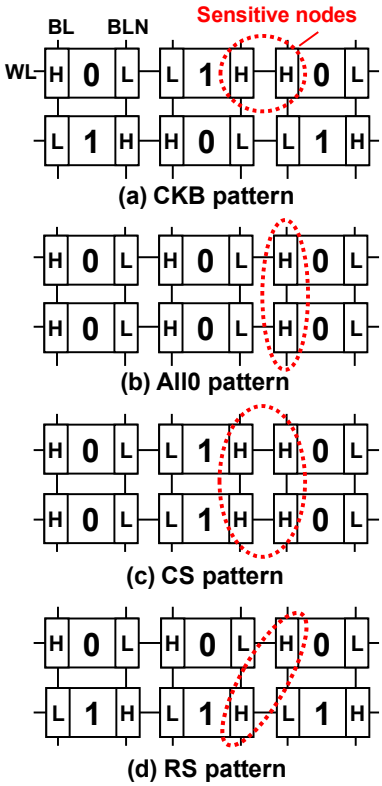

Figure 10. Data patterns: (a) checker-board (CKB), (b) all zero (All0), (c) column stripe (CS), and (d) row stripe (RS).

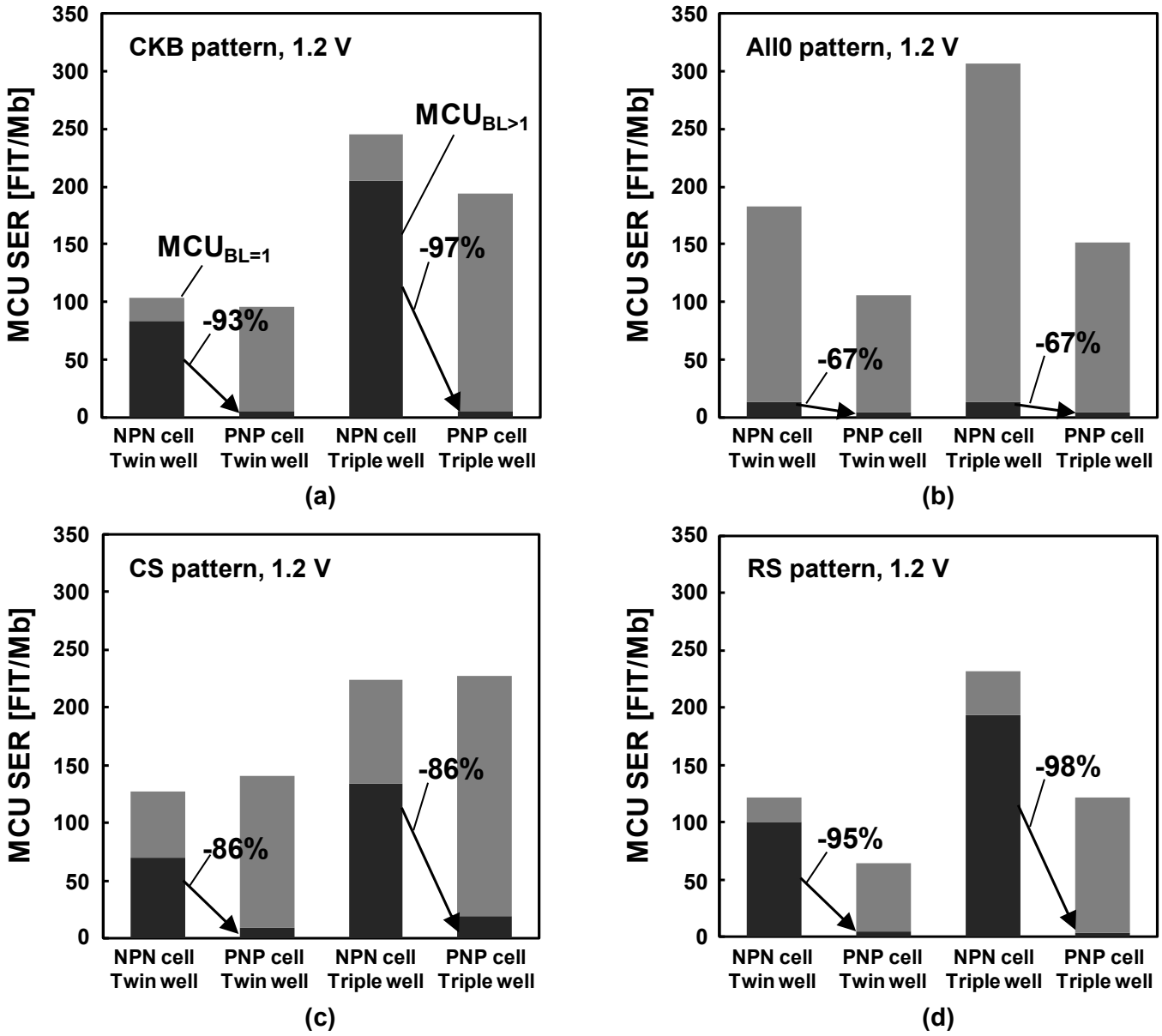

Figure 11. MCU SER improvements at 1.2 V when using (a) CKB, (b) All0, (c) CS, and (d) RS patterns. A gray bar shows $MCU_{BL=1}$ and a black bar shows $MCU_{BL>1}$.

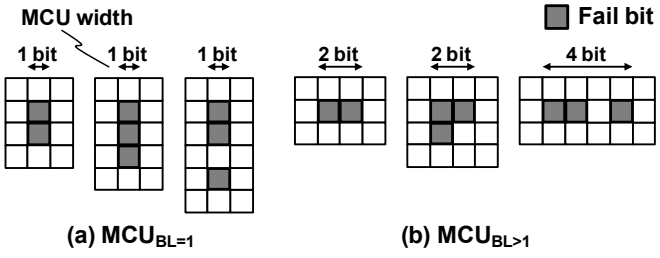

Figure 12. Multiple-cell-upset patterns: (a) $MCU_{BL=1}$ and (b) $MCU_{BL>1}$ are defined respectively by vertical fail bits in a same column and by horizontal fail bits in two or more columns.

In addition to the SBU SER, we measured MCU SER using four data patterns presented in Fig. 10: (a) CKB, (b) all zero (All0), (c) column stripe (CS), and (d) row stripe (RS), in which sensitive node patterns differ.

Figs. 11(a)–(d) portray measured MCU SER in the four data patterns at the supply voltage of 1.2 V. Hereinafter, as presented in Fig. 12, an MCU SER in the vertical direction is called $MCU_{BL=1}$, and an MCU SER in the horizontal direction is called $MCU_{BL>1}$. The $MCU_{BL>1}$ is more important for designers to adopt the interleaving and/or ECC strategy. When using the CKB, CS, and RS patterns, the $MCU_{BL>1}$ in the PNP 6T SRAM can be suppressed by 86–98% compared to the general NPN layout. The novel PNP layout separates NMOSes

from adjacent ones in the horizontal direction, which reduces the $MCU_{BL>1}$ SER. However, only 67% improvement is observed in the All0 pattern because no horizontally adjacent sensitive node exists even in the NPN layout in this pattern. The novel PNP layout with the twin-well structure achieves $MCU_{BL>1}$ SERs of 6, 5, 9, and 5 FIT/Mb in the CKB, All0, CS and RS patterns and the PNP layout with the triple-well structure achieves $MCU_{BL>1}$ SERs of 6, 5,19 and 3 FIT/Mb.

IV. Conclusion

Reducing the horizontal $MCU_{BL>1}$ SER is more crucial than the vertical one, which can be suppressed by SEC-DEC ECC. This paper presented a novel PNP (NMOS-inside) 6T SRAM that makes a neutron-induced $MCU_{BL>1}$ SER lower than the general NPN 6T SRAM in the horizontal direction. We designed a 65-nm 1-Mb SRAM test chips including the NPN and PNP SRAM macros. The measurement results demonstrate that the PNP layout suppresses the horizontal $MCU_{BL>1}$ SER by 67–98% in the CKB, All0, CS and RS patterns with the twin-well and triple-well structure in which the tap density is 1/32 of memory cells.

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