A 51-dB SNDR DCO-Based TDC Using Two-Stage Second-Order Noise Shaping

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***Abstract*—This paper presents a two-stage second-order noise shaping time-to-digital converter (TDC) using a one-bit digitally-controlled oscillator (DCO). The clocks output from DCOs are counted and digitized as in a conventional gated ring oscillator (GRO) TDC. A time error is propagated to the second DCO, which provides second-order noise shaping. In the conventional GROTDC, internal oscillators must maintain their phase state. However, because of the leak current, the stored phase states are degraded or even lost. In our proposed architecture, the DCOs always oscillate and need not maintain their phase state. Therefore, our proposed TDC is more suitable in leaky recent process than a GROTDC is. Because no switched capacitor or opamp is used, the proposed TDC can be implemented in a small area and with low power. Mismatches in the oscillation frequency between the DCOs might occur. However, error detection and correction can be performed using a first-order least mean square (LMS) filter. In a standard 65-nm CMOS process, an SNDR of 51 dB is achievable at an input bandwidth of 3 MHz and a sampling rate of 65 MHz, where the power is 271 μW.**

I. Introduction and Previous Studies

Designing high-performance and low-power-consumption chips at low-cost is necessary to produce competitive information and communications equipment. Scaling in process technology has enabled the miniaturization of transistors. Consequently, the number of transistors in a device can be increased. Low-cost functionality of digital systems has developed rapidly. Low-power features have also been achieved by reducing the supply voltage.

For analog circuits, however, deriving benefits from scaling is difficult. Low-supply-voltage operation reduces the dynamic range. Linearity becomes degraded, and gain in an opamp is lessened. To compensate for these disadvantages, transistor sizing and the area of passive components are ever-increasing. Consequently, a mixed-signal chip comprising digital and analog circuitry can achieve neither low cost nor low power in recent advanced process. An analog-to-digital converter (ADC) is a critical component of mixed-signal circuits, in which opamps and capacitors prevent merits derived from scaling, particularly in a ΔΣ ADC.

Several ADCs operating in a time domain have been examined recently. One ADC uses two-ring oscillators comprising inverters and voltage-controlled delay units (VCDUs) [1], which are put in the inverter chains, where an analog input voltage is fed to a VCDU. Depending on the value of the analog input voltage, the pulse in this ring oscillator is delayed as a function of the VCDU. The delay time appears behind another ring oscillator with no input voltage. In other words, a phase delay between the ring oscillators is sampled as a datum in each period. Then, a one-bit time-to-digital converter (TDC) with a data flip-flop (DFF) digitizes the phase delay. This ADC architecture inherently has a first-order noise shaping characteristic because the output from the TDC is fed back to the ring oscillator via the VCDU, where it acts as an integrator. However, it is extremely difficult, virtually impossible, to match the frequencies in the two-ring oscillator, which creates a timing error, although a signal is handled in the time domain. Another issue is nonlinearity in the VCDU. To make matters worse, the mismatch between the two VCDUs produces adverse effects. Consequently, implementing a higher-order ADC with the VCDUs or even first-order ADC implies a difficult design.

Instead of the VCDU, a voltage-controlled oscillator (VCO) is used as an ADC [2]–[4], in which a VCO frequency varies depending on the analog input voltage. This type of ADC is called a VCO-Based ADC. A multi-bit quantizer counts the rising edges of the oscillation. This mechanism also has a first-order noise shaping characteristic. A higher-order ΔΣ ADC can be achieved using active filters with opamps and other analog elements. This type of ADC, however, presents disadvantages: the VCO has nonlinearity like that of a VCDU-type ADC in terms of a voltage-to-frequency conversion. Designing higher-order ADC requires opamps and other analog elements that are unsuitable for advanced processes.

To convert the analog voltage data into the time domain data, some studies have been done. Methods such as voltage-controlled delay line (VCDL) and asynchronous delta sigma modulator (ADSM) [5] have been reported. The TDC has been developed and assessed as an internal circuit of a phase lock loop (PLL). On the other hand, the gated ring oscillator TDC (GROTDC) has been studied as a TDC that uses a ring oscillator comprising gated inverters [6]. Figure 1 portrays a GROTDC circuit diagram. A pulse width (T_{in}) is input to a

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GROTDC as a time-varying analog datum. During T_{in}, the GROTDC quantizes it with the counter by counting up the clock, GRO_{out}. Then the datum is shown as a discrete value. It is noteworthy that this GROTDC also has a first-order noise shaping characteristic, but in the literature, its function as the first-order modulator is merely exhibited.

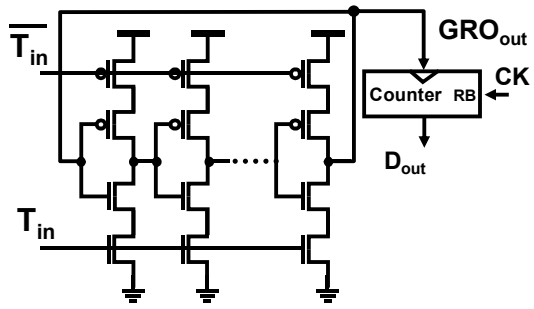

Figure 1 Gated ring oscillator time-to-digital converter (GROTDC).

High-order noise shaping GROTDC architecture has been reported as presenting the possibility of propagating the quantization error noise using a DFF and of realizing higher performance using a GROTDC [7]. Figure 2 portrays a second-order multi-stage noise shaping (MASH) GROTDC architecture, which employs GROTDCs as ΔΣ modulators. The counters are quantizers. The DFF propagates the quantization error to the next stage. Therefore, this architecture realizes second-order noise shaping. However, GRO's gating behavior is affected by switching noise and transistor leakage. Therefore, the stored phase states are degraded or even lost. This architecture is not perfect in leaky recent process.

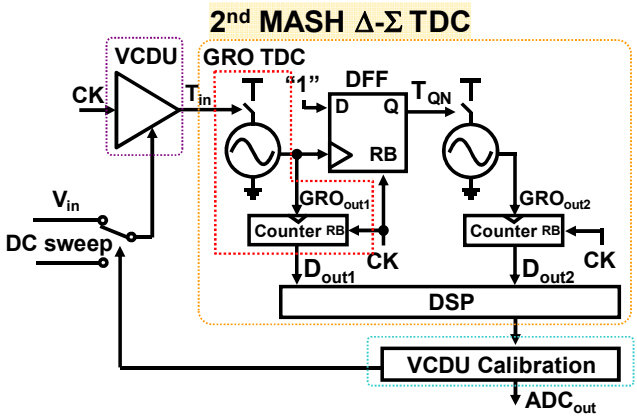

Figure 2 Second-order MASH GROTDC architecture with VCDU.

II. Proposed One-Bit DCO-Based TDC

Our proposed architecture is depicted in Figure 3. The one-bit digitally controlled oscillator (DCO) presents several advantages over a GRO by alleviating problems related to leak current and power supply noise. Our proposed TDC architecture uses a DCO instead of a GRO. Actually, a DCO has two modes: a high-frequency mode and a low-frequency mode. During T_{in}, the output frequency of the DCO becomes high. Unlike a GRO, the DCO does not stop its oscillation or does not maintain its output phase state.

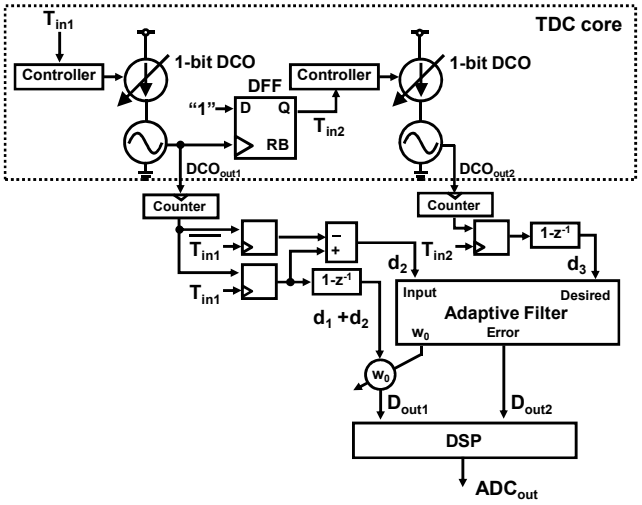

Figure 3 Proposed two-stage second-order noise shaping one-bit DCO-based TDC architecture.

Regarding the conventional GROTDC, when the Enable signal is off, the GRO ceases oscillation and maintains the output phase state. However, leakage current or switching noise will prevent maintenance of its internal state. Use of the proposed DCO eliminates these problems because the DCO continues oscillating and the leakage effects are negligible.

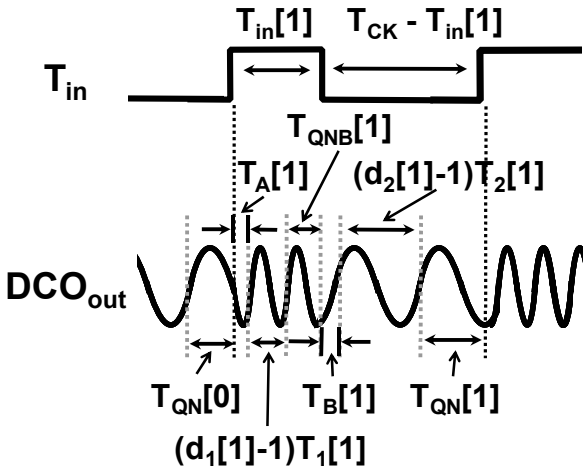

Figure 4 Timing diagram of the one-bit DCO-based TDC

Figure 4 depicts a timing diagram of the one-bit DCO-based TDC. Therein, T_{in} signifies the input pulse width into TDC, DCO_{out} stands for the output of the oscillation, T_1 denotes the period of the fast mode waveform, and T_2 represents that of the slow mode waveform, d_1 and d_2 denote the number of clocks, and T_{QN} and T_{QNB} represents the periods of the DCO oscillation, which are the quantization errors. T_{in} and $T_{CK}-T_{in}$ can be estimated as shown below:

$$T_{in}[k] = T_A[k] + (d_1[k]-1)T_1 + T_{QNB}[k], \quad (1)$$

$$T_{CK} - T_{in}[k] = T_B[k] + (d_2[k]-1)T_2 + T_{QN}[k]. \quad (2)$$

Because the total phase of T_A and T_{QN} equals 2π, T_A is given as

$$T_A[k] = \frac{2\pi - 2\pi T_{QN}[k-1]/T_2}{2\pi} T_1. \quad (3)$$

Similarly, T_B is given as

$$T_B[k] = \frac{2\pi - 2\pi T_{QNB}[k]/T_1}{2\pi} T_2. \quad (4)$$

As T_{QNB} can be canceled with using the four equations presented above, the total oscillation counts of $d_1 + d_2$ are

$$\begin{aligned} d_1[k] + d_2[k] &= \{T_{CK} - w_1 T_{in}[k] - (T_{QN}[k] - T_{QN}[k-1])\}/T_2 \\ w_1 &= 1 - T_2/T_1 \end{aligned} \quad .(5)$$

Then, during T_{in} off, a DFF detects the first rising edge of DCO and outputs the following.

$$T_{in2}[k] = (d_2[k]-1)T_2 + T_{QN}[k]. \quad (6)$$

By inputting T_{in2} to the next DCO controller, quantization error propagation can be realized. Similarly, the total oscillation counts of the second DCO d_3 are represented as the expressions shown below:

$$\begin{aligned} d_3[k] &= \{T_{CK} - w_2 T_{in2}[k] - (T_{QN2}[k] - T_{QN2}[k-1])\}/T_4 \\ &= \{T_{CK} - w_2(d_2[k]-1)T_2 - w_2 T_{QN}[k] \\ &\quad - (T_{QN2}[k] - T_{QN2}[k-1])\}/T_4 \\ w_2 &= 1 - T_4/T_3 \end{aligned} \quad . \quad (7)$$

In the equations shown above, T_3 denotes the period of the fast mode, and T_4 represents that of the slow mode. To realize second-order noise shaping, the mismatches in the oscillation frequency between DCOs must be estimated. Our architecture adaptively estimates the ratio of the oscillation frequency between the DCOs. Because T_{in} is included in d_3 and d_2, its ratio can be estimated. Using T_{in}, d_2 is represented as

$$d_2[k] - 1 = \{T_{CK} - T_{in}[k] - T_B + T_{QN}[k]\}/T_2 \quad (8)$$

The mismatch between d_2 and d_3 can be resolved using the following coefficient $w_E = w_2 T_2/T_4$. Furthermore, w_0 can solve the mismatch of T_{QN} between eq. 5 and eq. 7. Therefore, this architecture requires only a one-order adaptive filter. We can reduce the area overhead of the digital circuits. Consequently, by using the Z-function, final digital output of the TDC is given by

$$\begin{aligned} TDC_{out} &= (1-z^{-1})(w_E d_2 + d_3) - w_E(d_1 + d_2) \\ &= \frac{w_1 w_2}{T_4} T_{in} - \frac{(1-z^{-1})^2}{T_4} T_{QN2} + C_{offset} \end{aligned} \quad . \quad (9)$$

In the above equation, C_{offset} is the total of all constant numbers. Therefore, our proposed TDC digitizes T_{in} with second-order noise shaping.

III. Implementation Results

We examined the waveform data obtained from a SPICE simulation using the LMS filter modeled using software (Matlab Simulink; The MathWorks Inc.). Figure 5 presents results of the estimated coefficients when the sampling rate is 65 MHz, the filter length is one, and the step size is 0.001. The coefficient converges in about 10 μs. Furthermore, it shows that the expected coefficient can be estimated using the LMS filter. The convergence time can be adjusted by changing the LMS filter step size. Figure 6 shows the output spectrum of the proposed TDC. It is apparent that the effect of second noise shaping is realized. The input signal frequency is 1 MHz, the signal amplitude is 1.9 ns, and the sampling rate is 65 MHz. The output SNDR of the first-order noise shaping is 44.9 dB in this case. The output SNDR of the second-order noise shaping is 51.2 dB, which achieves about a 6-dB improvement in the SNDR. The TDC core consumes 179.9 μW in the DCOs including the controllers, and 91.1μW in the DFF.

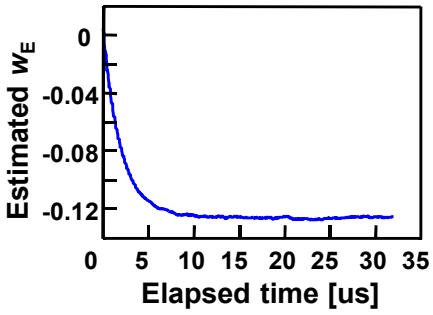

Figure 5 Learning curve of the LMS filter for coefficient estimation.

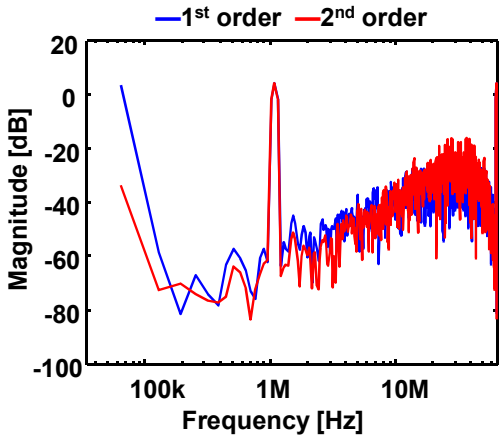

Figure 6 Output spectra of the first- and second-order noise shaping TDCs.

Assuming that the power line of the oscillator has a decoupling capacitance of 1 pF, the noise waveforms appear at the side of the circuit as shown in Figure 7. In this case, the frequency of the conventional GRO is 4.58 GHz, the slower frequency of the DCO is 4.48 GHz, and the faster one is 6.82 GHz. When using a DCO, the voltage drop during startup and shutdown is less than that of the GRO. In addition, the undershoot and overshoot during the DCO's switching are less than those of the GRO. Therefore, reduction of the noise from the oscillator itself can be expected.

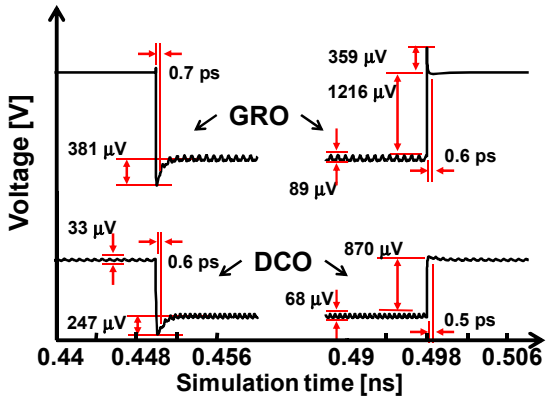

Figure 7 Noise waveforms on the power line of the oscillators.

Figure 8 portrays simulation results with consideration of leakage current in a 65-nm process. Both results show the characteristics of second-order noise shaping. For the GROTDC, the noise floor turns out higher. Under the identical conditions, the noise shaping effect of the DCO is more evident than that of the GRO, and the side effect of the leakage current is smaller in the DCO.

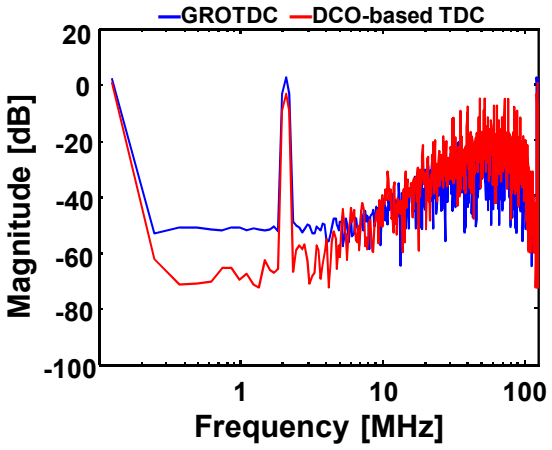

Figure 8 Output spectra of the conventional GROTDC and our proposed TDC both with second-order noise shaping.

IV. Summary

Herein, we described a 51-dB one-bit DCO-based TDC with second-order noise shaping. The TDC core circuit consumes 271µW. The proposed architecture obviates analog circuits such as opamps and switched capacitors. The control and calibration of the TDC are implemented with digital circuits, which can support production of low-power TDCs at low cost. The proposed TDC thereby maintains scalability with future leaky advanced processes. As process technology advances, the ring oscillator frequency is expected to increase, which will be beneficial for the proposed TDC. Process scaling will support our proposed TDC architecture in the future. The design cost and turn around time (TAT) can be reduced as well.

If we adopt a voltage-to-time converter for our architecture, this analog-to-digital converter (ADC) can be adapted to various applications such as ubiquitous sensors, in which many ADCs must be implemented on a chip. One node collects information through the ADCs. It then forwards it to a base station. A low-power ADC with a small footprint and without opamps or capacitors is expected to be useful for future ubiquitous applications.

Acknowledgments

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