A 62-dB SNDR Second-Order Gated Ring Oscillator TDC with Two-Stage Dynamic D-Type Flipflops as A Quantization Noise Propagator

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Abstract—**This paper presents a second-order noise shaping time-to-digital converter (TDC) with two gated ring oscillators (GROs). The oscillating outputs from the GROs are counted and digitized. As a quantization noise propagator (QNP) between the two GROs, two-stage dynamic d-type flipflops (DDFFs) a NOR gate are adopted. The proposed QNP does not propagate a time error caused by flipflop's metastability to the next GRO, and thus improves its linearity over the conventional master-slave d-type flipflop. In a standard 65-nm CMOS process, an SNDR of 62-dB is achievable at a sampling rate of 65MS/s.**

I. INTRODUCTION

Designing high-performance and low-power chips at low-cost is necessary to produce competitive information and communications equipment. Scaling in process technology has enabled the miniaturization of transistors. Consequently, the number of transistors in a device is increasing; low-cost functionality of digital systems can be developed. Low-power features are achieved by reducing supply voltage.

For analog circuits, however, deriving benefits from scaling is difficult. Low-voltage operation reduces a dynamic range. Linearity becomes degraded, and gain in an opamp is lessened. To compensate for these disadvantages, transistor sizing and the area of passive components are ever-increasing; a mixed-signal chip comprising digital and analog circuitry can achieve neither low cost nor low power in a recent advanced process. An analog-to-digital converter (ADC) is a critical component of mixed-signal circuits, in which opamps and capacitors prevent merits derived from scaling, particularly in a $\Delta\Sigma$ ADC.

Several ADCs operating in a time domain have been examined recently. A voltage-controlled oscillator (VCO) is used [1]–[3], in which a VCO frequency varies depending on an analog input voltage. A multi-bit quantizer counts the rising edges of the oscillation. This type of ADC is called a VCO-based ADC.

Another type of ADC uses a time-to-digital converter (TDC) that converts an analog time into a digital datum. Combining a TDC with a voltage-controlled delay line (VCDL) and an asynchronous delta sigma modulator (ADSM) has been reported as an ADC [4]. The TDC has been also developed and assessed as an internal circuit of a phase lock loop (PLL).

As a TDC, the gated ring oscillator TDC (GROTDC) has been studied that uses a ring oscillator comprising gated inverters [5]. Figure 1 portrays a GROTDC circuit diagram. A pulse width (T_{IN}) is input to a GROTDC as a time-varying analog datum. During T_{IN}, the GROTDC quantizes it with a counter by counting up the oscillation, GRO_{OUT}. Then, the count datum is shown as a discrete value. It is noteworthy that this GROTDC has a first-order noise shaping characteristic, but in the literature, its function as the first-order modulator is merely exhibited.
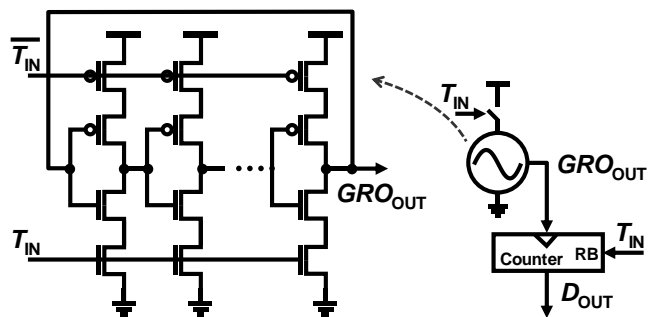

Figure 1   Gated ring oscillator time-to-digital converter (GROTDC).

II. HIGH-ORDER GROTDC

High-order noise shaping GROTDC architecture has been reported as presenting the possibility of propagating the quantization noise using a d-type flipflop (DFF) and of realizing higher performance using a GROTDC [6]-[7]. Figure 2 portrays a second-order multi-stage noise shaping (MASH) GROTDC architecture, which employs GROTDCs as $\Delta\Sigma$ modulators. The counters are quantizers. The quantization noise propagator (QNP) consists of a conventional master-slave d-type flipflop (MSDFF) propagates the quantization noise to the next stage.
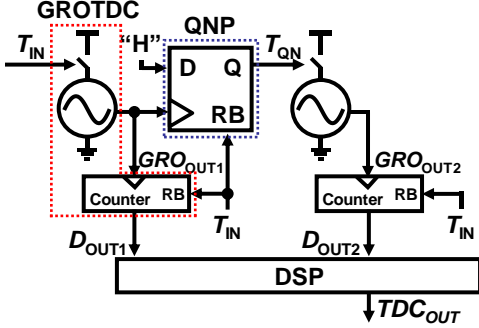

Figure 2   Second-order MASH GROTDC architecture.

Figure 3 shows a timing diagram of the conventional second-order GROTDC. When T_{IN} is high, the first-stage GRO oscillates. When is low, it ceases the oscillation and maintains the output phase state. The QNP is reset by a low state of T_{IN}, and detects the first rising of GRO_{OUT1}. Thus, the QNP propagates T_{QN} that contains a quantization noise to the next GRO. D_{OUT1} (D_{OUT2}) denotes the number of GRO_{OUT1} (GRO_{OUT2}) oscillations in the sampling period. D_{OUT1} (D_{OUT2}) includes QN_1 (QN_2) representing a quantization noise of GRO_{OUT1} (GRO_{OUT2}). By correctly propagating QN_1 to the second-stage GRO and cancelling it using D_{OUT1} and D_{OUT2}, the GROTDC achieves a second-order noise shaping characteristic. That is, the performance of the QNP as a propagator is crucial for the high-order GROTDC.
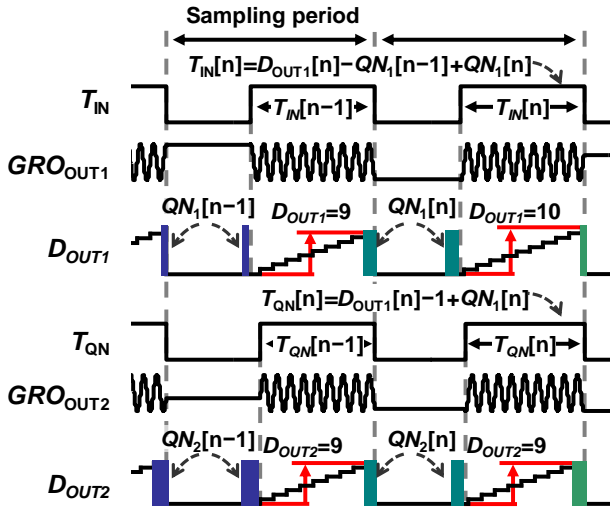

Figure 3   Timing diagram of GROTDC

The MSDFF QNP, however, produces a large jitter in a time domain because of its metastability. When a rising edge of GRO_{OUT1} and a rising edge of T_{IN} are close, the metastability occurs. The MSDFF QNP cannot propagate a correct quantization noise because it takes a long time to stabilize its output in the metastable state. As a result, the MSDFF QNP worsens the second-order noise shaping characteristic.

III. PROPOSED LOW-JITTER DYNAMIC D-TYPE FLIPFLOP

As shown in Figure 4, we propose a dynamic d-type flipflop (DDFF) to minimize the metastability; the DDFF can be comprised of only six transistors because a data input is fixed to "high". The simple DDFF operates faster than the conventional MSDFF, and thus is resilient to the metastability. As well, its linearity and operating frequency are better than the MSDFF.
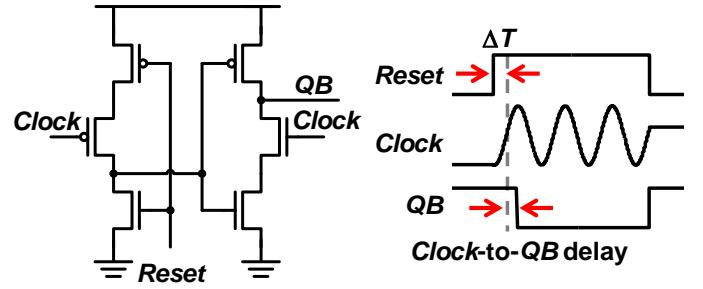

Figure 4   Schematic and timing diagram of the proposed DDFF.

Figure 5 compares "*Clock*-to-*QB*" delay characteristics in the conventional MSDFF and proposed DDFF. In the figure, ΔT is defined as a time interval from the rising edge of "*Reset*" to the first rising edge of "*Clock*". If they are close each other, the metastability occurs.
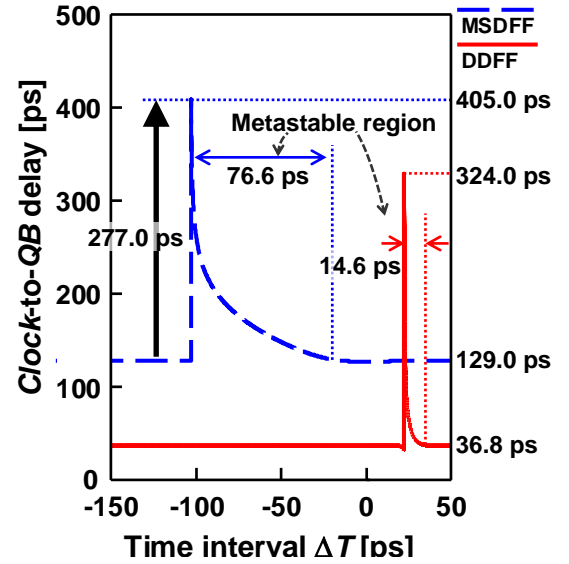

Figure 5   "Clock-to-QB" delay characterictics.

Normally, the respective delays are 129.0 ps and 36.8 ps in the MSDFF and the DDFF; the proposed DDFF is four times faster. The delays are deteriorated in the metastable regions.

The widths of the metastable regions are 76.6 ps and 14.6 ps, respectively in the MSDFF and DDFF; the metastable region, which is a sensitive timing, is five times narrower in the proposed DDFF.

IV. PROPOSED QNP WITH TWO-STAGE DDFFS

To mask the metastable region and achieves the faster operation, we propose a novel QNP using the DDFFs. As shown in Figure 6, the proposed QNP has two DDFFs and a NOR gate. Figure 7 shows a timing diagram of the proposed QNP.
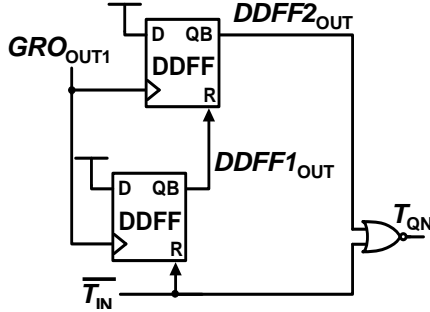

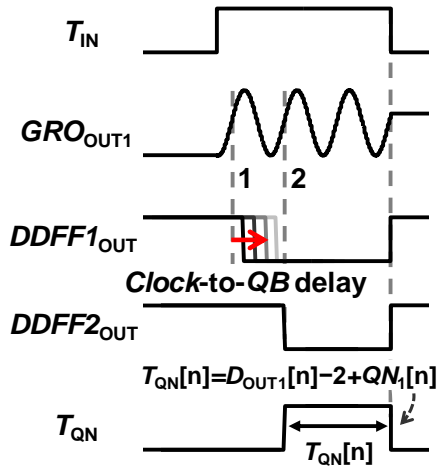Figure 6   Proposed QNP comprising two-stage DDFFs..

Figure 7   Timing diagram of the proposed QNP.

$DDFF1_{OUT}$ denotes the output of the first-stage DDFF. $DDFF1_{OUT}$ is delayed if metastability occurs. At the second-stage DDFF, however, metastability never occurs unless the oscillation period of GRO_{OUT1} is shorter than 324.0 ps (see Figure 5 for a metastable delay of 324.0 ps in the DDFF). This is the reason why we prepare the two-stage DDFF, with which a correct quantization noise can be fed to the next GRO.

Figure 8 shows propagation characteristics of the MSDFF and the proposed QNP; the linearity of QN_1 is evaluated. The oscillating frequency of GRO_{OUT1} is set to 900 MHz. In the MSDFF, the mismatch is as much as 277.0 ps (see Figure 5).
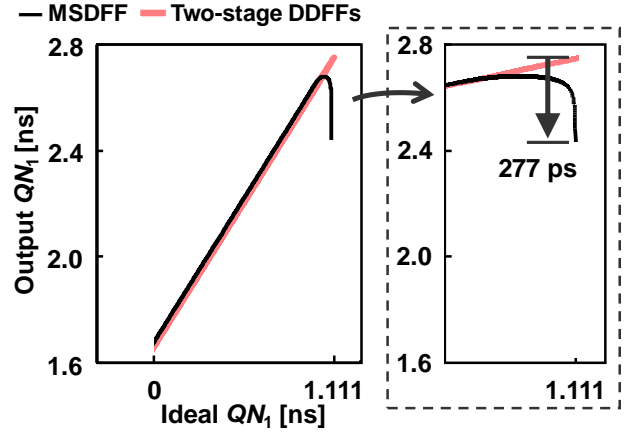

Figure 8   Transfer characteristics of MSDFF and two-stage DDFF

V. IMPLEMENTATION RESULTS

Figure 9 shows the negative impact of the metastability in the second-order MASH GROTDC with the conventional MSDFF in a 65-nm process. In this simulation, the GRO oscillates at 2.17 GHz (the oscillating period is 460 ps). The sampling rate is 65MS/s. In every sampling period, an incorrect quantization noise is injected at a possibility of 20%, which causes metastability. The second-order noise shaping characteristic is not achievable if the metastability exists.

Figure 10 compares simulation results between the MSDFF and the proposed QNP. The GROTDC with the proposed QNP, which can accurately propagate a quantization noise, exhibits the second-order noise shaping characteristic. Its SNDR is 62 dB, whereas that in the GROTDC with the MSDFF is lowered to 52 dB.
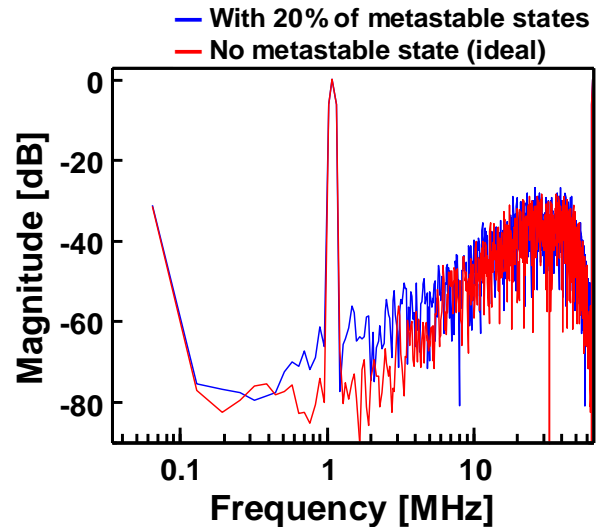

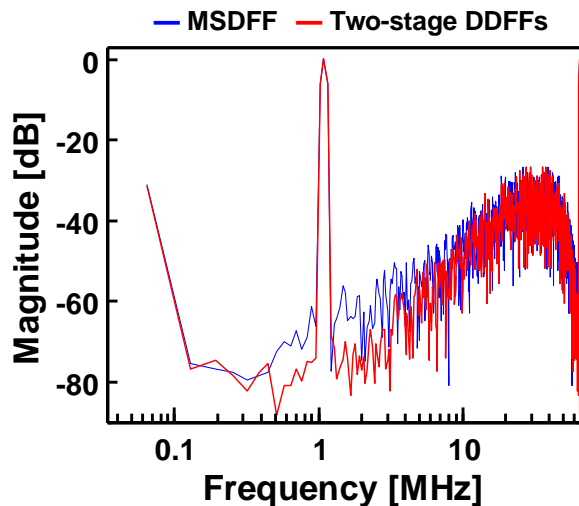Figure 9   Output spectra in the GROTDC with the conventional MSDFF.

Figure 10 Output spectra in the GROTDCs with the conventional and the proposed QNP.

VI. SUMMARY

We described a 62-dB second-order GROTDC. The second-order noise shaping characteristic is achieved by a novel QNP with two-stage DDFFs that propagate a correct quantization noise. The proposed architecture obviates analog circuits such as opamps and switched capacitors. The control of the TDC is implemented with digital circuits. The proposed TDC thereby maintains scalability with future advanced processes. As process technology advances, the ring oscillator frequency is expected to increase, which will be beneficial for the proposed TDC. A three-order or multiple-order TDC will be possible in our proposed TDC architecture.

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