Multiple-Cell-Upset Hardened 6T SRAM Using NMOS-Centered Layout

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Abstract— **This paper presents a proposed NMOS-centered 6T SRAM cell layout that reduces a neutron-induced multiple-cell-upset (MCU) SER on a same wordline. We implemented an 1-Mb SRAM macro in a 65-nm CMOS process and irradiated neutrons as a neutron-accelerated test to evaluate the MCU SER. The proposed 6T SRAM macro improves the horizontal MCU SER by 67–98% compared with a general macro that has PMOS-centered 6T SRAM cells.**

Keywords; SRAM, soft error rate (SER), multiple cell upset (MCU), neutron particle, twin well, triple well

I. INTRODUCTION

Nano-scaled integrated circuits are susceptible to particle-induced single event effect (SEE) because of their low signal charge and noise margin [1]. Particularly multiple cell upsets (MCUs), which are defined as simultaneous errors in more than one memory cell induced by a single event, have been closely investigated. The MCUs are caused by a collection of charges produced by secondary ions in neutron-induced nuclear reaction. The ratio of the MCUs to single-event upsets (SEUs) is predicted to increase drastically in nano-scaled SRAMs [2].

Figure 1 shows a layout of a general 6T SRAM cell with a 65-nm CMOS logic rule. The 6T cell consists of PMOS load transistors (PL0, PL1), NMOS driver transistors (ND0, ND1) and access transistors (NA0, NA1). A wordline (WL) and two bitlines (BL, BLN) are horizontally and vertically connected among cells, respectively. In the layout of the general 6T cell, the PMOS transistors are centered in the memory cell; this structure is called an NMOS-PMOS-NMOS (NPN) layout in this paper.

We have observed that the NMOS has a four-times larger SEU cross section than a PMOS for a wide range of supply voltages (see Fig. 2) [3]. In the conventional 6T SRAM, the sensitive NMOS nodes are in a same P-well in the horizontal direction; horizontal upsets can be easily incurred.

II. PROPOSED NMOS-CENTERED 6T SRAM CELL AND MACRO DESIGN

The proposed 6T cell is designed as a PMOS-NMOS-PMOS (PNP) layout in Fig. 3. The NMOS-centered 6T layout has the same transistors as the general one. The PNP 6T cell can lower a horizontal MCU rate because the NMOS-centered layout can separate the horizontally adjacent NMOS sensitive nodes. The proposed layout has the same schematics and the cell area on the 65-nm logic rule basis, so that the proposed design can be implemented only by replacing its cell layout.

We designed and fabricated an 1-Mb SRAM test chip consisting of 256-Kb macros of four types (NPN layout with twin well, PNP layout with twin well, NPN layout with triple well, and PNP layout with triple well), as presented in Fig. 4.

III. EXPERIMENTAL RESULTS

Figure 5 presents an experimental setup for a neutron-accelerated test. The neutron irradiation experiment is conducted at The Research Center for Nuclear Physics (RCNP), Osaka University. Spallation neutron beam generated by the 400-MeV proton beam irradiates a board under test (BUT) 7892-mm far from a tungsten target, on which three sample chips are placed in a BUT, for 30 hrs. The neutron flux is normalized to 13 cph / cm^2 above 10 MeV at ground level in New York City [4], which incorporates scattering effect [5], attenuation effect [6], and board screening effect [7].

We measured MCU SER using two data patterns presented in Fig. 6: (a) checker-board (CKB) and (b) all-zero (ALL0). As presented in Fig. 7, an MCU SER in the vertical direction is called $MCU_{BL=1}$ in this paper, and an MCU SER in the horizontal direction is called $MCU_{BL>1}$. The $MCU_{BL>1}$ is more important for designers to adopt the interleaving and/or ECC strategy.

Figure 8 shows MCU SER depending on a space from a tap cell. The MCU SER is higher in the triple well than that in twin well. In addition, we observed that the SER is increased in the far place from the tap cell.

Figures 9(a) and 9(b) illustrate measured MCU SER in the data patterns at the supply voltage of 1.2 V. The $MCU_{BL>1}$ in the PNP 6T SRAM can be suppressed by 67–98% compared to the general NPN layout. The proposed PNP layout separates NMOSes from adjacent ones in the horizontal direction, which reduces the $MCU_{BL>1}$ SER.

IV. CONCLUSION

Reducing the horizontal $MCU_{BL>1}$ SER is more crucial than the vertical one, which can be suppressed by SEC-DEC ECC. This paper presented a proposed PNP (NMOS-centered) 6T SRAM that makes a neutron-induced $MCU_{BL>1}$ SER lower than the general NPN 6T SRAM in the horizontal direction. We designed a 65-nm 1-Mb SRAM test chips including the NPN and PNP SRAM macros. The measurement results demonstrate that the PNP layout suppresses the horizontal $MCU_{BL>1}$ SER by

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67–98% in the CKB and ALL0 patterns with the twin-well and triple-well structure.

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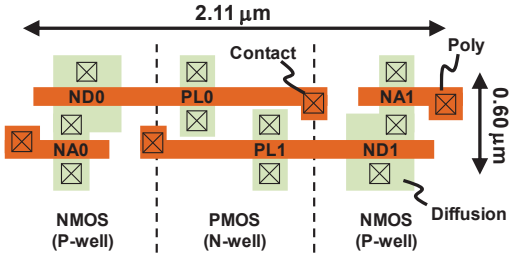

Figure 1. General NMOS-PMOS-NMOS (NPN) 6T SRAM cell layout.

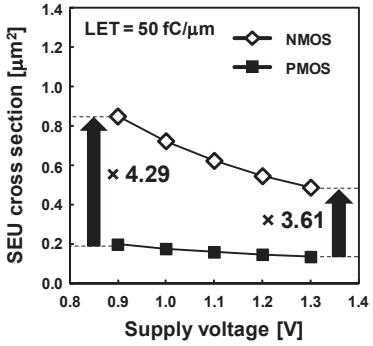

Figure 2. SEU cross sections of NMOS and PMOS.

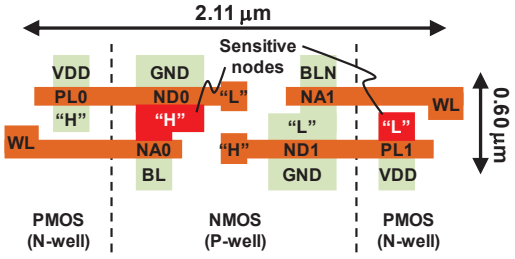

Figure 3. Proposed PMOS-NMOS-PMOS (PNP) 6T SRAM cell layout.

Figure 4. Implemented test chip photograph.

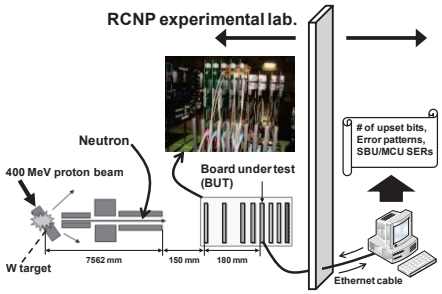

Figure 5. Setup for neutron-accelerated test.

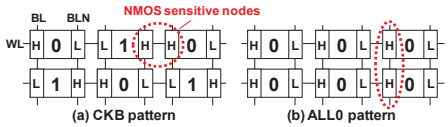

Figure 6. MCU error patterns: (a) checker-board (CKB) pattern and (b) all-zero (ALL0) pattern.

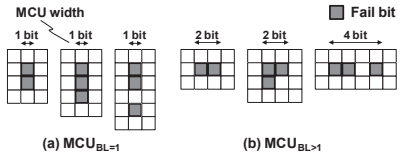

Figure 7. Multiple-cell-upset patterns: (a) MCU$_{BL=1}$ and (b) MCU$_{BL>1}$.

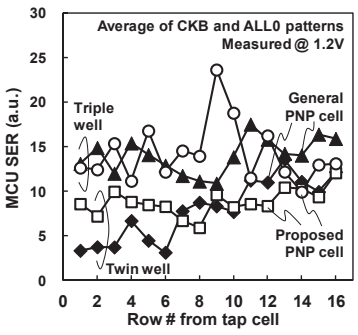

Figure 8. MCU SER results depending on a space from a tap cell.

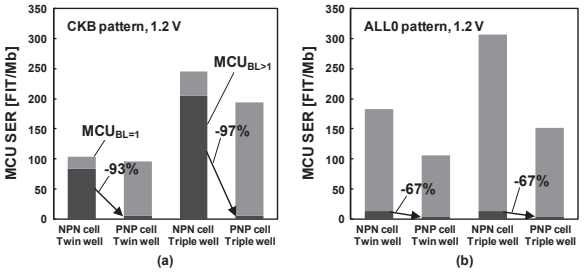

Figure 9. MCU SER measurement results in (a) CKB pattern and (b) ALL0 pattern