The Area Criteria of 6T and 8T SRAM Cells

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1. Background

SRAM (Static Random Access Memory)

Trend of operating voltages

6 transistor SRAM (6T SRAM)

8 transistor SRAM (8T SRAM)

2. Simulation condition

Simulation setups

β, γ ratio VS Memory capacity

Optimization of gate length

1. Results and future works

Minimum gate length

Optimum gate length

Area criteria of 6T and 8T Cells

Future works

Cell area is important for cost, yield, and etc for SRAM. However, more metrics of performance are required to choose 6T or 8T.

- Speed
- Macro area
- Power
- and etc...

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Xeon Nehalem-EX (Intel)

A Flip-Flop stores a datum. The datum is selected by horizontal word line and vertical bit line.

Feature
- compatible to CMOS logic process.
- Fast random access latency.
- A lot of application: L1 Cache, large capacity memory.

Core 5

Core 6

Core 7

Core 0

Select word line

Word Line (WL)

Bit Line (BL)

GND

VDD

V1

V2

Read port

Write port

Optimization of gate length decreases the cell size.

- b ratio is suppressed to minimum ratio.
- 8T SRAM can be smaller than 6T SRAM at low-voltage operation.

When memory capacity is large, 6T Cell requires large β and γ ratio. On the other hand, 8T Cell only needs γ ratio and suppresses its b ratio.

Static Random Access Memory

Stand operation voltage of LSI is going down as technology scaling. However, Minimum operating voltage is going up because threshold voltage variation is increased. The minimum operating voltage restricts LSI operating voltage scaling. Low-voltage operating SRAM is strongly needed.

Xeon Nehalem-EX (Intel)

Optimization of gate length decreases the cell size.

Et SRAM cell has a trade off: SNM and WNM. Large b and g ratios increase cell size at low voltage.

When we design an SRAM, supply voltage and capacity are important factors. For example, 8T Cell is smaller than 6T Cell at 26.4Kbit, 1.0V in 32nm with a minimum gate.