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A 40-nm 0.5-V 12.9-pJ/Access 8T SRAM Using Low-Energy Disturb Mitigation Scheme*

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SUMMARY This paper presents a novel disturb mitigation scheme which achieves low-energy operation for a deep sub-micron 8T SRAM macro. The classic write-back scheme with a dedicated read port overcame both half-select and read-disturb problems. Moreover, it improved the yield, particularly in the low-voltage range. The conventional scheme, however, consumed more power because of charging and discharging all write bitlines in a sub-block. Our proposed scheme reduces the power overhead of the write-back scheme using a floating write bitline technique and a low-swing bitline driver (LSBD). The floating bitline and the LSBD respectively consist of a precharge-less CMOS equalizer (transmission gate) and an nMOS write-back driver. The voltage on the floating write bitline is at an intermediate voltage between the ground and the supply voltage before a write cycle. The write target cells are written by normal CMOS drivers, whereas the write bitlines in half-selected columns are driven by the LSBDs in the write cycle, which suppresses the write bitline voltage to VDD - V_{tn} and therefore saves the active power in the half-selected columns (where V_{tn} is a threshold voltage of an nMOS). In addition, the proposed scheme reduces a leakage current from the write bitline because of the floating write bitline. The active leakage is reduced by 33% at the FF corner, 125°C. The active energy in the write operation is reduced by 37% at the FF corner. In other process corners, more writing power reduction can be expected because it depends on the V_{tn} in the LSBD. We fabricated a 512-Kb 8T SRAM test chip that operates at a single 0.5-V supply voltage. The test chip with the proposed scheme respectively achieves 1.52-μW/MHz writing energy and 72.8-μW leakage power, which are 59.4% and 26.0% better than those of the conventional write-back scheme. The total energy is 12.9 μW/MHz (12.9 pJ/access) at a supply voltage of 0.5 V and operating frequency of 6.25 MHz in a 50%-read/50%-write operation.

key words: *SRAM, 8T, low energy, disturb, half select, write back*

1. Introduction

As process technology has been scaled down, it has become increasingly difficult to realize a stable bitcell design in a 6T SRAM because of the tradeoff between read and write margins [2]. An 8T bitcell with a dedicated read port is proposed to obviate the 6T's read margin, which achieves low-voltage operation in nature.

The separation of read and write ports frees the bitcell design of the read/write tradeoff. The area of the 8T cell is expected to be smaller than that of the 6T cell in a future process [3]. Although low-voltage and high-yield 8T SRAMs under 1.0-V operation are proposed [4]–[6], the power per operation cycle (= energy) is larger than that in 6T SRAMs [6]–[8] because the 8T cell needs an extra 2T read port. Furthermore, an assist circuit must be implemented to avoid the disturb (half-select) problem [9]. Figure 1 portrays the tendency of power per cycle among recent SRAMs. Our research object is to achieve a low-voltage and low-energy SRAM: 0.5-V and sub-100 μW/MHz/Mb operation is the target.

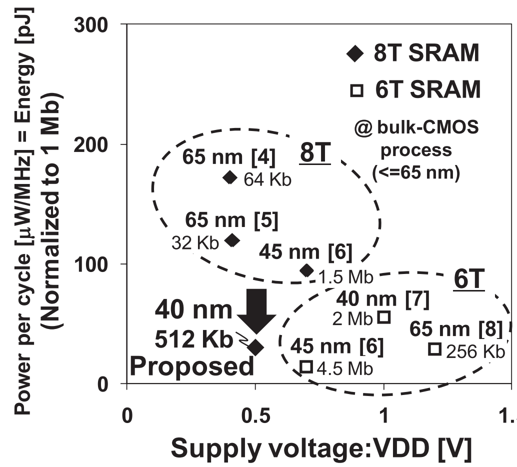

Fig. 1 Supply voltage versus energy among low-power bulk-CMOS SRAMs [4]–[8].

Figure 2(a) depicts selected and half-selected cells in an SRAM array. On an activated wordline, the selected cells are written by write drivers. However, half-selected cells are disturbed by the precharged write bitlines. When the writability of the SRAM cell is enhanced, the static noise margin of the half-selected cell is decreased, and vice versa. The half-select problem degrades the SRAM operation margin. To mitigate the half-select problem and lower the operating voltage, the divided wordline structure [10] and the write-back scheme [11] (Fig. 2(b)) are useful in the 8T SRAM at a single supply voltage.

The divided wordline structure produces no half-selected cells by incorporating separate wordlines, but aligning a word with physically adjacent bits (word-interleaving) weakens a soft error immunity against single-event multiple-cell upsets (MCU) caused by ionized-particle strikes. A recent work [12] reports that a ratio of MCU to

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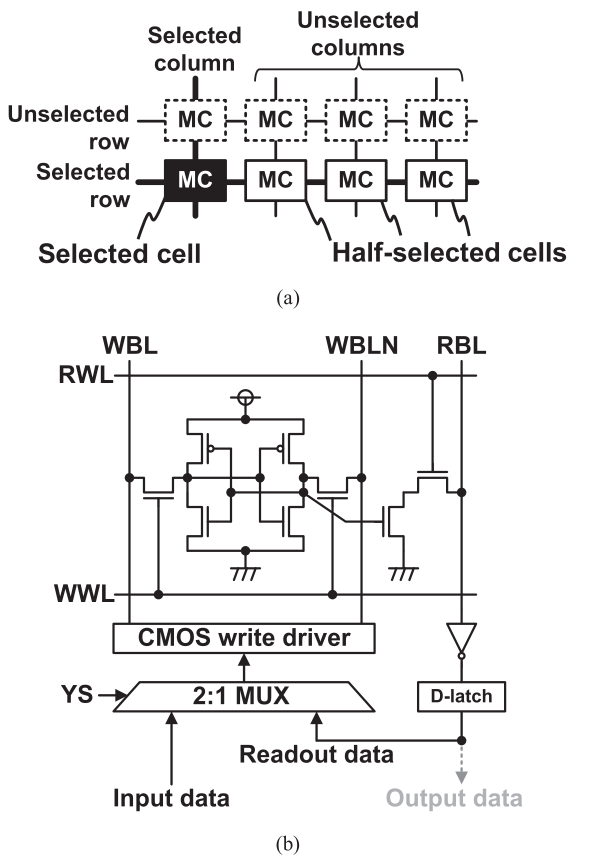


Fig. 2 (a) Selected cell and half-selected cells in the SRAM array. (b) Conventional write-back scheme [3] with a single-ended 8T cell.

the total single-event upsets is as high as about 50% and that the failed bits spread out in more than 1,000 × 1,000 (= 1 M) bits at a 22-nm node. In a bit-leaving structure, multiple-bit upsets (MBU = MCU in a same word) can be, however, suppressed to a reasonable FIT (failure in time) value by single-bit error correction coding (ECC) [13], because more than 99% of the MCU in a wordline direction are adjacent two bits [12]. In contrast, the MBU in the divided wordline structure cannot be suppressed by single-bit ECC because the failed two bits are physically adjacent in the same word.

Although different design requirements [14] in the latest SRAMs necessitate various functionalities, and although one functionality is the partial-write operation [15], the partial-write operation cannot be implemented in the divided wordline structure because a separated wordline is incorporated.

The write-back scheme for the 8T SRAM design can be implemented in the bit-interleaving structure, which provides soft-error immunity and partial-write functionality. The write-back scheme eliminates the half-select problem; however, a read operation is required even in a write cycle. In the write-back scheme in the write operation, input data to be written go to target cells at target columns, but at half-selected columns, readout data are written back to half-selected cells. Because the readout data at the half-selected columns do not need to be transferred to output buffers, the speed penalty in the write-back scheme can be minimized.

The write-back scheme has power overhead because the CMOS write drivers fully pull the write bitlines (WBL/WBLN) up or down at all half-selected columns. The WBLs are usually longer than read bitlines (RBL) to preserve array efficiency [5]. Consequently, the active energy in the half-selected columns degrades the energy efficiency.

To achieve low-energy operation without the divided wordline structure, we propose a novel disturb mitigation scheme in this paper. The proposed scheme reduces the active power and a leakage power using a low-swing bitline driver (LSBD) and a precharge-less CMOS equalizer (transmission gate) for a floating write bitline.

The remaining part of this paper is organized as follows. The circuit implementation of the proposed LSBD and the precharge-less CMOS equalizer for the floating write bitline in the disturb mitigation scheme are discussed in Sect. 2 with simulation results. The proposed scheme improves the energy efficiency of the 8T SRAM. In Sect. 3, we present the experimentally-obtained results of a 40-nm 512-Kb SRAM test chip. Section 4 concludes the paper.

2. Proposed Disturb Mitigation Scheme

To reduce extra energy for the half-select problem, we propose a disturb mitigation scheme that features the following: floating WBLs with a precharge-less equalizer (CMOS transmission gate) and the low-swing bitline driver (LSBD) with nMOS pull-up transistors for the WBLs, which limit the swing of the WBLs in the half-selected columns.

Figures 3(a) and 3(b) portray a local cell array (128 rows × 8 columns) and a 16-Kb sub-block (16 local cell arrays) configuration of the proposed SRAM. Figure 3(a) also shows circuitry of the local read circuit, the LSBD, and the precharge-less equalizer. The single-ended 8T cell is adopted in the SRAM as presented in Fig. 2(b). The proposed 8T SRAM employs a hierarchical read bitline (RBL) structure. The number of cells per RBL is 16 for stable read operation. In contrast, a WBL is shared by 128 cells to preserve the array efficiency. The WBLs are not precharged to a supply voltage, but floated because of the precharge-less equalizer. A local read circuit and an LSBD are shared by 32 cells. A CMOS write driver is shared by a local cell array.

Figure 4 portrays operating waveforms of the proposed scheme. In a read cycle, a read enabling (RDE) signal is activated; then a global read bitline (GRBL) is discharged when an RBL is pulled down. In the write cycle, the dedicated read ports transport the data to the local read circuits. Column line enable (CLE) signals are high in the selected columns and the LSBDs are disabled as presented in Fig. 5. In the half-selected columns (CLE = "L"), the proposed LSBDs drive the WBLs according to the readout data when the driver enable (DRN) signal is grounded. The LSBD consists only of nMOSes. Thereby, the swing of WBLs is limited by the threshold voltage of the nMOSes. After the WBLs are pulled up or down by nMOS-based LSBDs, the write wordline (WWL) is activated. The selected cell is written by the

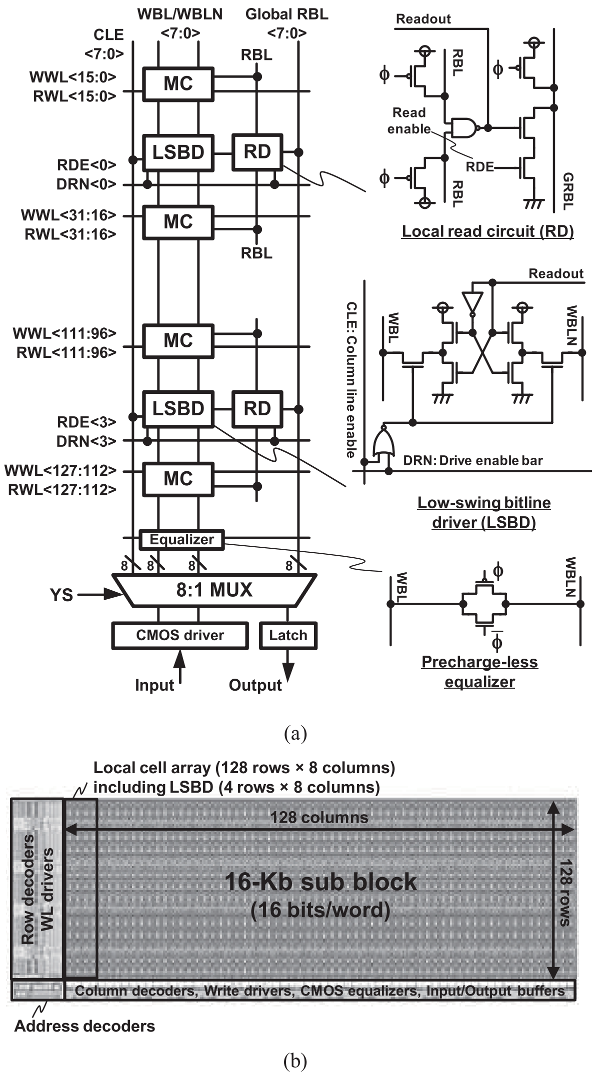


Fig. 3 (a) Local cell array and (b) 16-Kb sub-block with the proposed circuitry including a low-swing bitline driver (LSBD) and precharge-less equalizer. "MC" signifies "single-ended 8T memory cell", as presented in Fig. 2(b).

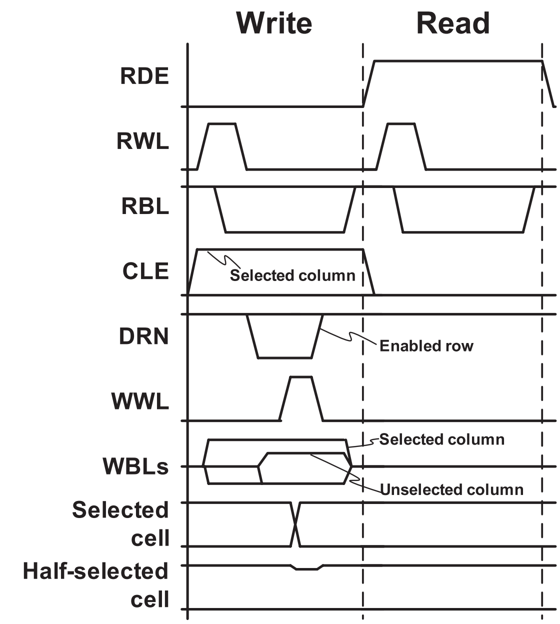


Fig. 4 Operating waveforms.

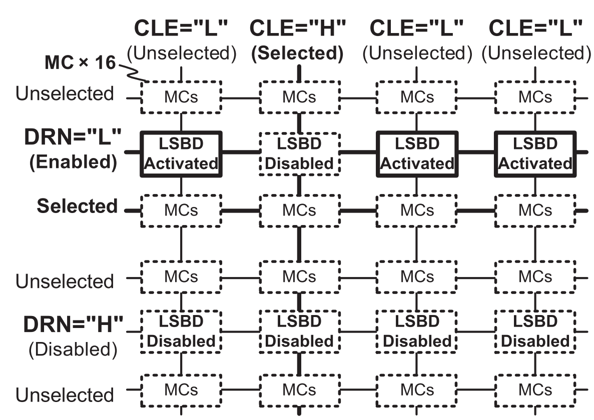


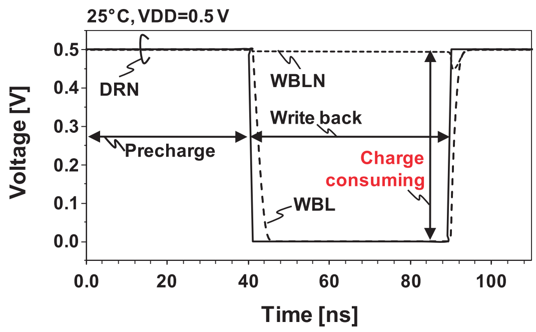
Fig. 5 Activated LSBDs exist on low-state CLE (column line enable) and low-state DRN (driver enable bar) signals.

CMOS write driver and the write margin is not degraded.

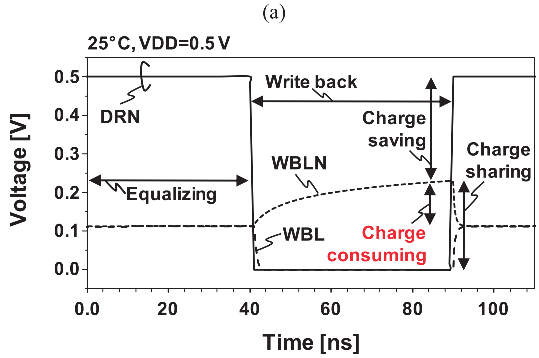
Figures 6(a) and 6(b) respectively show waveforms of the write bitline pair (WBLs: WBL and WBLN) in the half-selected columns with the conventional write-back scheme and the proposed scheme. In the conventional write-back scheme, the WBLs are precharged to supply voltage until the DRN signal is pulled down. The WBL is grounded and the WBLN is pulled up by the CMOS drivers. When the write operation is finished, the WBLs are precharged again. In contrast, the WBLs in the proposed scheme are floated until the DRN activation. When the WBL and WBLN are pulled down and up by the proposed LSBD, then the charging energy is saved because the rising write bitline voltage is saturated at an intermediate voltage by the threshold voltage of an nMOS in the LSBD. At the end of the write cycle, the write bitlines' voltages are again equalized with charge sharing. The floating WBLs reduce bitline leakage current because no precharge transistors are incorporated.

Figure 7 shows that a pulled-up WBL level depends on V_{tn}: if an nMOS is fast, then the V_{tn} drop is small, the disturb mitigating assist becomes effective. However, a slow nMOS can save power because its swing is small. The enlarged margin and saving power are a tradeoff. Figure 8 portrays the active power reduction compared to the conventional write-back scheme at the write cycle. The active energy on the WBLs is reduced by 37%, 60%, and 79%, respectively at the FF, CC, and SS corners at 25°C.

We investigated the disturbance margins of the half-select cells with the proposed disturb mitigation scheme. Monte-Carlo analyses are executed at the five process corners and at three temperatures when VDD is 0.5 V. The simulation considers threshold voltage variation in the LSBD shared by 32 bitcells. The yield in Table 1 shows that the SS corner at −40°C is the worst case and its yield is 3.27σ, in



(a)



(b)

Fig. 6 Waveforms of the half-selected cells assisted by (a) the conventional write-back scheme and (b) the proposed scheme.

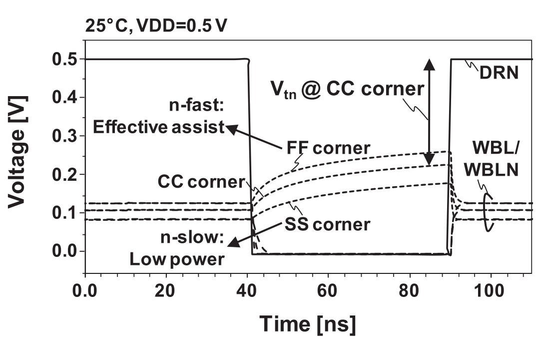


Fig. 7 Pulled-up WBL level dependence on the global corner.

Table 1 Yields of half-selected cells in the proposed scheme.

Yield @ 0.5 V (based on Monte Carlo)		Temperature [°C] -40	25 (RT)	125
Global corner	FF	5.39σ	> 7σ	> 7σ
	FS	4.79σ	5.59σ	> 7σ
	CC	4.31σ	5.49σ	> 7σ
	SF	4.04σ	5.45σ	> 7σ
	SS	3.27σ	4.47σ	6.85σ

which the pull-up transistors in the LSBD is weakened. In the worst case, the voltage of the suppressed WBL, "VDD − V_{tn}" is decreased. The weak pull-up transistor and the more suppressed WBL causes more disturbing current flowing through the pass gate transistor of the SRAM cell. The tradeoff between the yield at the global corner and the saved

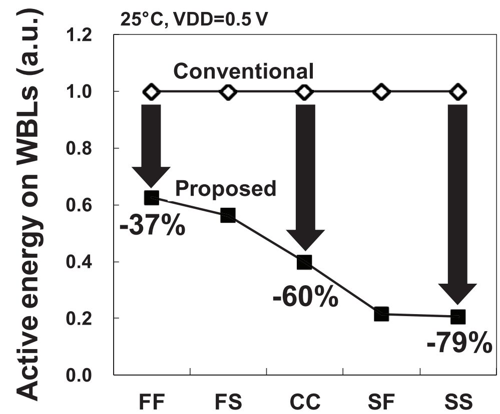


Fig. 8 Active energy reductions on WBLs at the five process corners (RT, room temperature; VDD = 0.5 V).

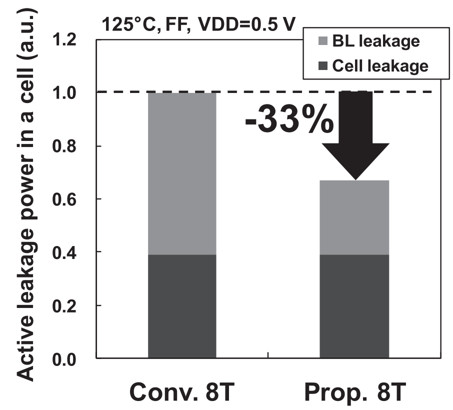


Fig. 9 Comparison of the active leakage powers of the conventional and proposed schemes (FF corner, 125°C, VDD = 0.5 V).

energy must be considered in the SRAM design.

Figure 9 portrays simulation results of the leakage power on the WBLs at the activated cycle in 8T bitcells. The leakage power in the worst corner is improved by 33% because of the low-swing feature of the LSBD.

3. Measurement Results

As presented in Fig. 10, we fabricated the proposed and conventional 512-Kb 8T SRAM macros using a 40-nm CMOS bulk process for comparison. The conventional macro incorporates a write bitline precharger connected to a supply voltage. Therefore, its write bitlines are fully charged and discharged in the write-back operation. The proposed 512-Kb macro consists of 32 × 16-Kb sub-blocks, as shown in Fig. 3(b). Table 2 shows specifications of the proposed SRAM test chip. The 8T bitcell area is 0.706 μm^2, which is 28% larger than a 6T cell with a β ratio of two. The transistor width of access gates is doubled to enhance a write margin while the other transistors are minimum sizing. The numbers of cells in a RBL and WBL are 16 and 128, respectively. The cell density is 701 Kb/mm^2.

Figure 11 presents a measured Shmoo plot of the pro-

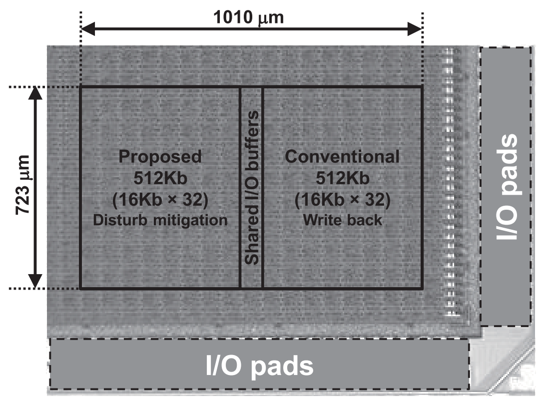


Fig. 10 Micrographs of the test chip: 1 Mb SRAMs include the proposed disturb mitigating scheme and the conventional write back scheme.

Table 2 Features of the test chip.

Technology	40-nm bulk CMOS
Macro size	0.723 mm × 1.010 mm
Macro configuration	512 Kb (16 Kb × 4 × 8), 16 bits/word
Cell size	0.706 mm (logic rule)
# of cells / BL	16 (RBL), 128 (WBL)
Cell density	701 Kb/mm^2
Power supply	0.5–0.8 V
Write active energy	1.52 μW/MHz @ 0.5 V, 6.25MHz, RT
Total energy (R/W=50/50)	12.9 μW/MHz @ 0.5 V, 6.25MHz, RT
Access time	160 ns @ 0.5 V, 4.5 ns @ 0.8 V

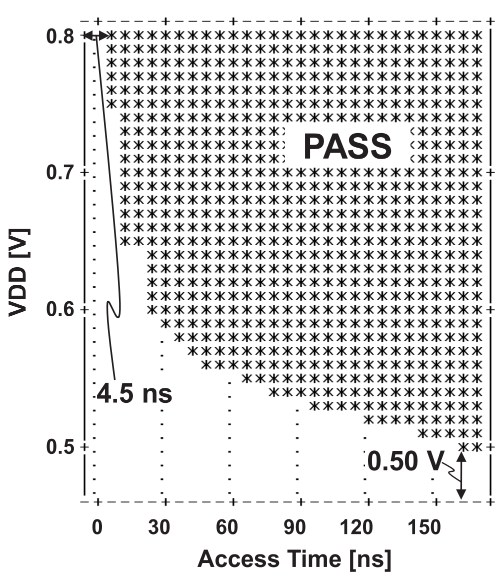


Fig. 11 Shmoo plot of the proposed 512-Kb SRAM macro.

posed 8T SRAM macro. The access time is restricted by the read operation. The minimum operating voltage is 0.5 V at an access time of 160 ns at room temperature (RT). Figures 12 and 13 respectively show that the measured leakage power and active energy, which are improved by 26.0% and 59.4% at the supply voltage of 0.5 V. The active energy in

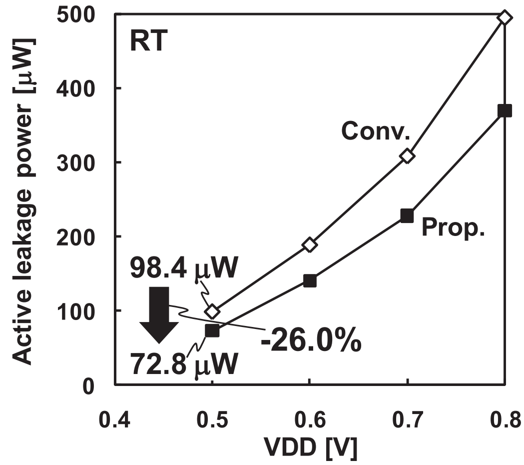


Fig. 12 Measured active leakage power at RT.

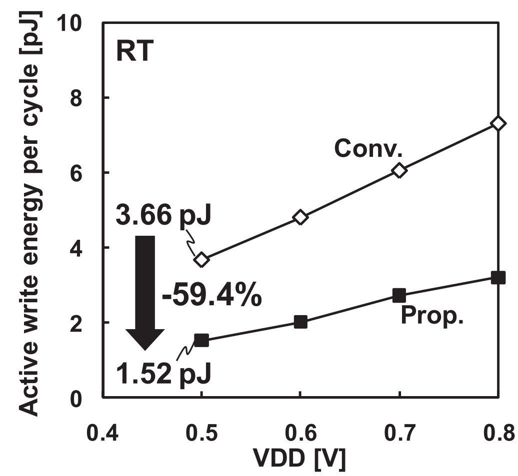


Fig. 13 Measured active energy per write cycle without leakage at RT.

the write cycle is 1.52 pJ (= μW/MHz). The total energy is 12.9 pJ when the read and write cycles are 50–50 at 0.5 V.

4. Conclusion

As described in this paper, a novel disturb mitigation scheme is proposed. It achieves low-power and low-voltage operation for an 8T SRAM. The proposed scheme has a 3.27σ yield at 0.5 V at the SS corner and low temperature. The active energy is improved by 37%, 60%, and 79% at FF, CC, and SS corners, respectively at 25°C. The 512-Kb 8T SRAM test chips were implemented in a 40-nm bulk-CMOS process. The SRAM operates at a single 0.5-V supply voltage at room temperature and achieves 1.52-μW/MHz active energy in a write cycle and 72.8-μW leakage power, which are 59.4% and 26.0% better than the conventional write-back scheme. The total energy is 12.9 μW/MHz at 0.5 V in a 50%-read / 50%-write operation.

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