A Negative-Resistance Sense Amplifier for Low-Voltage Operating STT-MRAM

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Abstract - This paper exhibits a 65-NM 8-Mb spin transfer torque magnetoresistance random access memory (STT-MRAM) operating at 0.38V. The proposed sense amplifier comprises a boosted-gate nMOS and negative-resistance pMOSes as loads, which maximizes the readout margin. The STT-MRAM achieves a cycle time of 1.9 µs (= 0.526 MHz) at 0.38 V. The operating power is 1.70 µW at that voltage.

I. Introduction

The capacity of embedded memory on a chip has been increasing. In fact, the ITRS predicts that leakage power in embedded memory will account for 40% of all power consumption by 2024 [1]. A spin transfer torque magnetoresistance random access memory (STT-MRAM), which stores data using magnetic tunnel junction (MTJ), is promising for use as non-volatile memory to reduce the leakage power. The MTJ has two states: a parallel state and anti-parallel state. The MTJ resistances are, respectively, low and high. The magnetization direction of the free layer determines the two states. Although the MTJ presents the potential for operating at less than 0.4 V [2], the low-voltage operating feature has not been demonstrated to date as an STT-MRAM macro because the design of peripheral circuitry is difficult. A pMOS load sense amplifier [2] or a sense amplifier with an opamp for a replica bias [3] does not function at that voltage. Figure 1 shows conventional operating VDDs and cycle times of the STT-MRAM previous studies. Operating voltage of the conventional studies are 1.0 V or more, which indicates that the peripheral circuits operate at low voltage is difficult. Herein, we present an STT-MRAM operating at a single 0.4-V supply voltage.

II. 8-Mb STT-MRAM Design

Figure 2 portrays the block diagram of a 1-Mb STT-MRAM macro and voltage domains. The boosted voltage(VDD_B=1.6V) is supplied by charge pump circuit provides. The macro comprises four 256-kb blocks, each of which consists of 512 bits × 512 words. The supply voltage (VDD) is 0.4 V. Figure 3 shows an STT-MRAM bitcell layout. The MTJ dimension is 59 × 59 nm^2. The STT-MRAM process is the same as that described in earlier reports [4, 5]. A detailed schematic of the proposed sense amplifier is exhibited as Fig. 4. Figure 5 shows the details of the current flowing through the proposed circuit. In the initial state, the initializing switch grounds Node "S". It can cuts off the leakage current through M_{p0} (I_{neg0}) in the current mirror of the negative-resistance pMOS load. In the read state, read enable signal becomes "High" and the nMOS load transistor (M_{n0}) turns on. Then a load current (I_{load}) flows from VDD. The voltage of the node "S" becomes higher in the early phase of the read operation. This is because of the output current from node "S"; it flows to clamp transistor and MRAM cell; is smaller than the input current "S" I_{load}. When the node "S" voltage becomes higher than the Vth of M_{n1}, the M_{p1} drives current from VDD. The readout current I_{load} and I_{neg1} flows from VDD, which exhibits a 0.4-V operation. The boosted voltage of VDD_B is used for the gate of the nMOS load transistor (M_n) and the initializing switch in the reading structure. Figure 6 shows operating curves of the load circuits. The total load current I_{cell}, $I_{cell} = I_{load} + I_{neg1}$, is a function of the Node "S" voltage. The intersection of the load current and I_P ("L") or I_{AP} ("H") results in I_{cell}. The voltage difference between "L" and "H" is greater than 250 mV, which is much more than that of a conventional pMOS load circuit [2]; VDD/2 serves well as a reference voltage (VREF).

III. Chip Implementation and Measurement Results

We fabricated a 65-nm test chip at the TT process corner, as presented in Fig. 7, to evaluate the low-voltage and low-leakage operation. The detailed process of the MTJ device used in the test chip is presented in the references [2, 5]. The macro size is 2.2 × 2.9 mm^2. Figure 8 shows a Shmoo plot of the test chip. We confirm that a 0.38-V operation at a cycle time of 1.9 µs (the operating frequency is therefore 0.526 MHz), for which conditions the operating power is 1.70 µW. At the low voltage, the read operation is achieved with the proposed sense amplifier; the write operation is done by applying a long write pulse of a small write current. TABLE 1 shows test chip characteristics.

IV. Summary

We presented a new sense amplifier with process variation tolerance for low-voltage operating STT-MRAM. The proposed sense amplifier can distinguish parallel states and anti-parallel states in 0.38V VDD. We fabricated an 8-Mb STT-MRAM in a 65-nm process technology. The test chip exhibits 0.38-V operation at a frequency of 0.526 MHz, where the power consumption is 1.70 µW.

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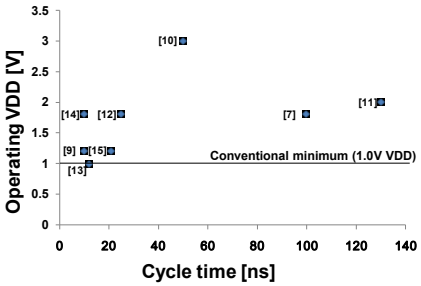

Fig. 1 Conventional operating VDDs and cycle times.

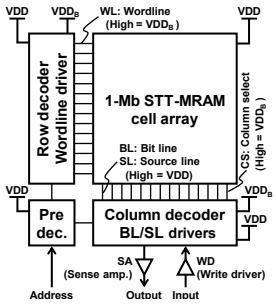

Fig. 2 1-Mb STT-MRAM macro.

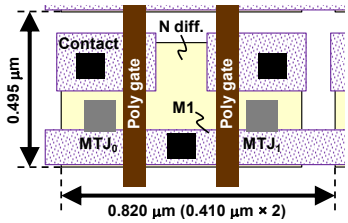

Fig. 3 STT-MRAM bitcell layout.

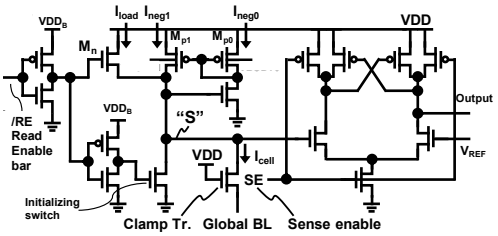

Fig. 4 Proposed sense amplifier.

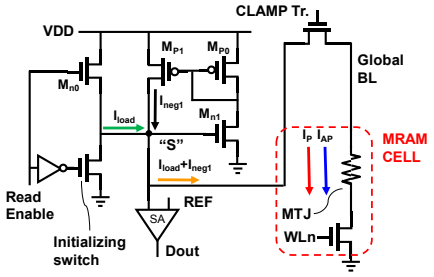

Fig. 5 Details of the current flowing through the proposed sense amplifier.

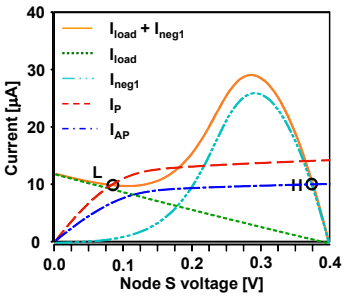

Fig. 6 Sense amplifier current characteristics.

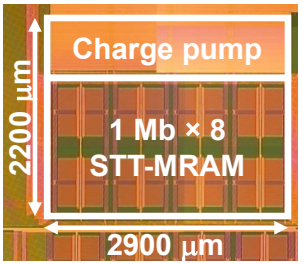

Fig. 7 Chip photograph.

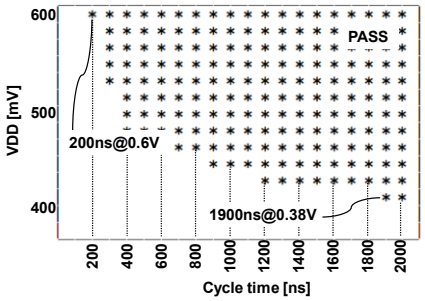

Fig. 8 Shmoo plot.

TABLE 1 Test chip characteristics.

Process technology	65-nm bulk CMOS
Nominal voltage	1.2V
Charge pump output	1.6V
Capacity	8Mb
Cell size	0.203mm2 (0.495mmx0.41mm)
Operating VDD	0.38V-0.6V
Oparating frequency	0.536MHz-5.00MHz
Oparating power	1.70mW@0.526MHz
Minimum energy per access	1.12 pJ/bit at 0.44 V and 1.66MHz
Charge pump output	1.6V