14-5

A 0.38-V Operating STT-MRAM with Process Variation Tolerant Sense Amplifier

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***Abstract*—This paper exhibits a 65-nm 8-Mb spin transfer torque magnetoresistance random access memory (STT-MRAM) operating at a single supply voltage with a process-variation tolerant sense amplifier. The proposed sense amplifier comprises a boosted-gate nMOS and negative-resistance pMOSes as loads, which maximizes the readout margin in any process corner. The STT-MRAM achieves a cycle time of 1.9 µs (= 0.526 MHz) at 0.38 V. The operating power is 6.15 µW at that voltage. The minimum energy per access is 3.89 pJ/bit when the supply voltage is 0.44 V. The proposed STT-MRAM operates at lower energy than SRAM when a utilization of a memory bandwidth is 14% or less.**

Keywords—STT-MRAM, Low voltage, Process variation tolerant

I. INTRODUCTION

The capacity of embedded memory on a chip has been increasing. In fact, the ITRS predicts that leakage power in embedded memory will account for 40% of all power consumption by 2024 [1]. A spin transfer torque magnetoresistance random access memory (STT-MRAM), which stores data as magnetic resistance states, is promising for use as non-volatile memory to reduce the leakage power. It is useful as embedded memory because it can function at low voltage and because it endures over 10^{16} write cycles [2]. In addition, the STT-MRAM technology makes its bitcell smaller than an SRAM so that it is suitable for use in high-density products [3–7].

Figure 1 presents a schematic 1T1M bitcell that has one transistor and one magnetic tunnel junction (MTJ) STT-MRAM bitcell. The MTJ has pinned and free layers, with a tunnel barrier (MgO barrier) between them as an insulator. The MTJ has two states: a parallel state and anti-parallel state. In the free layer, its magnetization direction can be switched by the current flowing through the MTJ, which corresponds to a datum stored in a bitcell. The MTJ resistances are, respectively, low and high in the parallel and anti-parallel states. In read operation, the stored datum is read out as a difference of the flowing current.

Although the MTJ presents the potential for operating at less than 0.4 V [8], the low-voltage operating feature has not been demonstrated to date as an STT-MRAM macro because the design of peripheral circuitry is difficult. A pMOS load sense amplifier [8] or a sense amplifier with an opamp for a replica bias [9] does not function at that voltage. Herein, we present an STT-SRAM operating at a single 0.4-V supply voltage. Our proposed sense amplifier functions well below 0.4 V at any process corner, with help from a charge pump circuit.

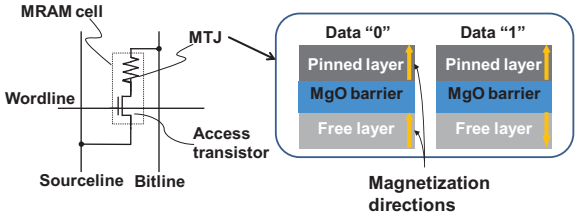

Fig. 1. STT-MRAM bitcell.

II. 8-MB STT-MRAM DESIGN

Figure 2 shows a macro-block diagram of the proposed 8-Mb STT-MRAM. The charge pump circuit provides a boosted voltage to eight 1-Mb STT-MRAM macros. A schematic of the charge pump circuit is depicted in Fig. 3. A 0.4-V clock swing is doubled to a 0.8-V amplitude by the double boost clock (DBC) generator, which is then forwarded to a charge pump capacitor. This charge pump supplies 1.6 V (= VDD_B).

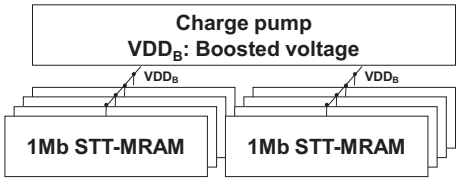

Fig. 2. 8-Mb STT-MRAM macro-block diagram.

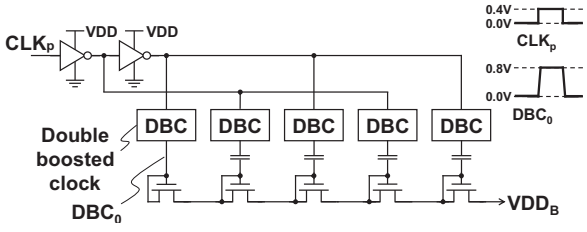

Fig. 3. Charge pump circuit and its waveforms.

Figure 4 portrays the block diagram of a 1-Mb STT-MRAM macro and voltage domains. The macro comprises four 256-kb blocks, each of which consists of 512 bits × 512 words. The supply voltage (VDD) is 0.4 V. Figure 5 specifically depicts the bitcell array and the data paths. To minimize the voltage drop through a bitline, a column selector using a transmission gate is adopted; the gate voltage of the transmission gate is controlled with the boosted voltage (VDD_B) of 1.6 V. Figure 6 presents the operating waveforms. When writing a datum "1", a bitline (BL) is increased to 0.4 V, or a source line (SL) is raised to 0.4 V when writing a datum "0". VDD_B is provided as a wordline voltage, which suppresses a cell current variation caused by variation in the access transistors.

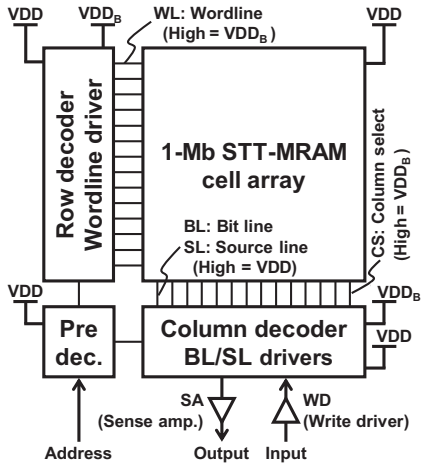

Fig. 4. 1-Mb STT-MRAM macro.

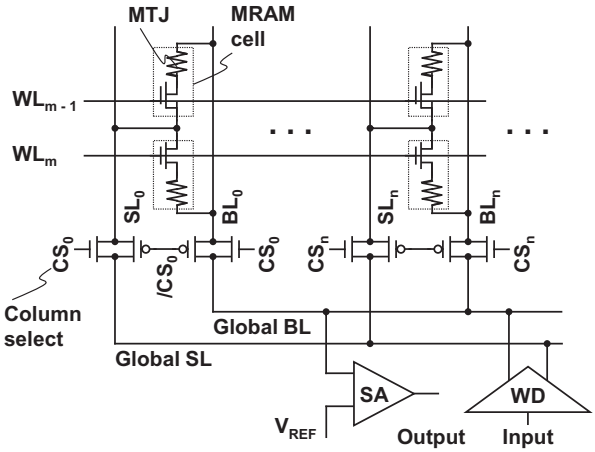

Fig. 5. Bitcell array and peripheral circuits.

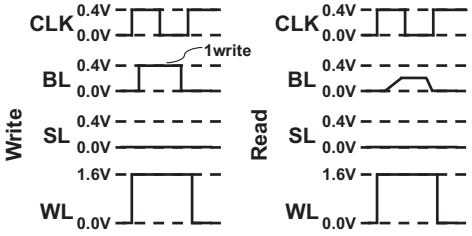

Fig. 6. Operating waveforms.

Figures 7 and 8 are, respectively, an SEM micrograph of a CoFeB-based MTJ and an STT-MRAM bitcell layout. The MTJ dimension is 59 × 59 μm^2. The STT-MRAM process is the same as that described in earlier reports [2, 11].

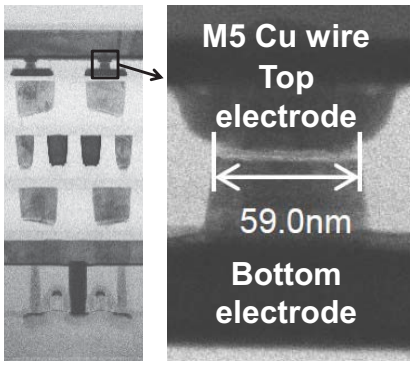

Fig. 7. SEM micrograph.

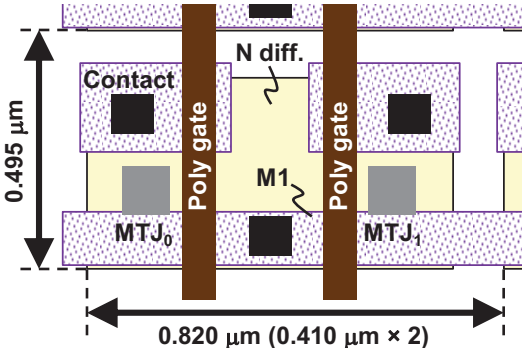

Fig. 8. STT-MRAM bitcell layout.

A detailed schematic of the proposed sense amplifier is exhibited as Fig. 9. The bitcell datum is determined by the Node "S" voltage; it is the input to the sense amplifier. The initializing switch grounds Node "S" in an idle state and cuts off the leakage current through M_{p0} (I_{neg0}) in the current mirror of the negative-resistance pMOS load. A readout current (I_{cell}) flows from VDD, which exhibits a 0.4-V operation. The boosted voltage of VDD_B is used for the gate of the nMOS load transistor (M_n) and the initializing switch in the reading structure.

Figure 10 shows operating curves of the load circuits at the typical process corner (TT: pMOS = typical, nMOS = typical). The total load current, $I_{load} + I_{neg1}$, is a function of the Node "S" voltage. The intersection of the load current and I_P ("L") or I_{AP} ('H") results in I_{cell}. The voltage difference between "L" and "H" is greater than 250 mV, which is much more than that of a conventional pMOS load circuit [3]; VDD/2 serves well as a reference voltage (V_{REF}). The size of the boosted nMOS load M_n can be reduced (moreover, its standby leakage can be reduced) because it operates in a linear region by virtue of its boosted voltage. Therefore, the load current is sufficient even with the small transistor. The proposed sense amplifier is process-variation tolerant, as shown in Figs. 11(a)–11(d). Even at the FF, FS, SF, and SS corners, the proposed sense amplifier can distinguish parallel from anti-parallel states.

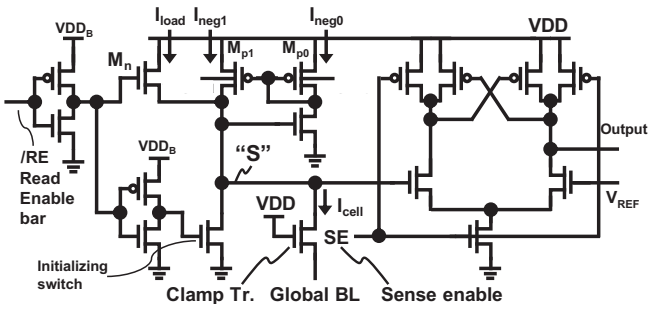

Fig. 9. Proposed sense amplifier.

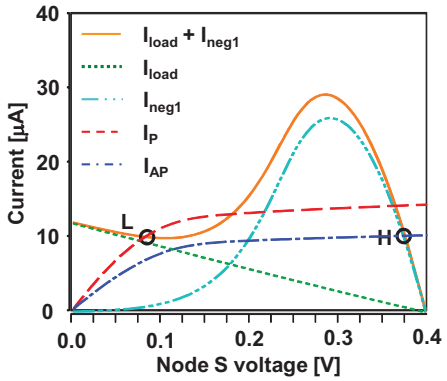

Fig. 10. Sense amplifier current characteristics at a typical (TT) process corner.

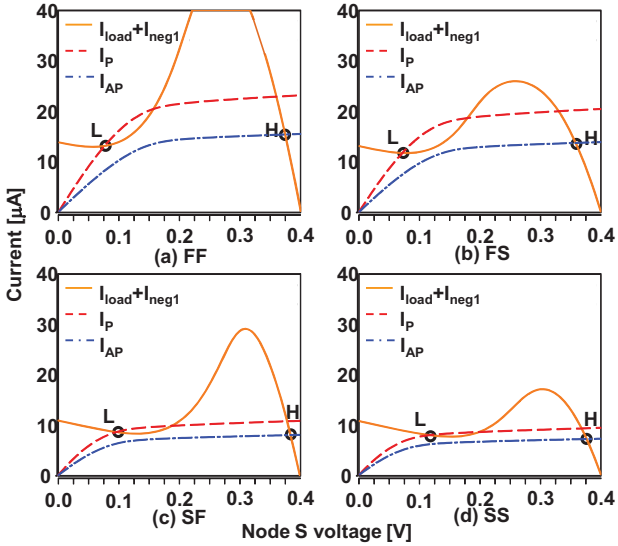

Fig. 11. Sense amplifier current characteristics at process corners: (a) FF, (b) FS, (c) SF, and (d) SS.

III. Chip Implementation and Measuremrnt Results

We fabricated a 65-nm test chip at the TT process corner, as presented in Fig. 12, to evaluate the low-voltage and low-leakage operation. The detailed process of the MTJ device used in the test chip is presented in the references [2, 11]. The macro size is 2.2 × 2.9 mm^2. Figure 13 shows a Shmoo plot of the test chip. We confirm that a 0.38-V operation at a cycle time of 1.9 μs (the operating frequency is therefore 0.526 MHz), for which conditions the operating power is 6.15 μW. At the low voltage, the read operation is achieved with the proposed sense amplifier; the write operation is done by applying a long write pulse of a small write current.

Figure 14 shows the energy-consumption of the proposed STT-MRAM and a low-voltage SRAM [10] in the same process technology. Both are measured values. The ratio of read and write accesses is 50:50. At an operating voltage of 0.5 V, the energy consumed in the STT-MRAM is 3.03 times larger than that in the SRAM. Figure 15 presents a breakdown of energy components. The respective ratios of active energy (E_{active}) to total energy (E_{active} + E_{leak}) are 96.7% and 15.4% in the STT-MRAM and SRAM. Figure 16 shows an energy comparison when a utilization of memory bandwidth is changed. The STT-MRAM is superior to the SRAM in terms of energy consumption if the utilization of memory bandwidth is 14% or less, which means the STT-MRAM is suitable in less-active application such as a healthcare system or sensor network. TABLE 1 shows test chip characteristics.

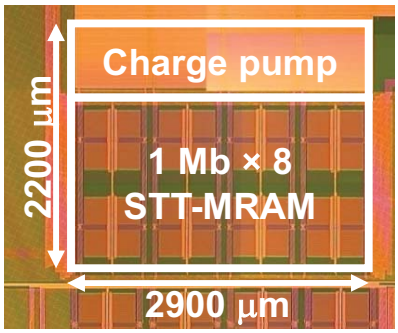

Fig. 12. Chip photograph.

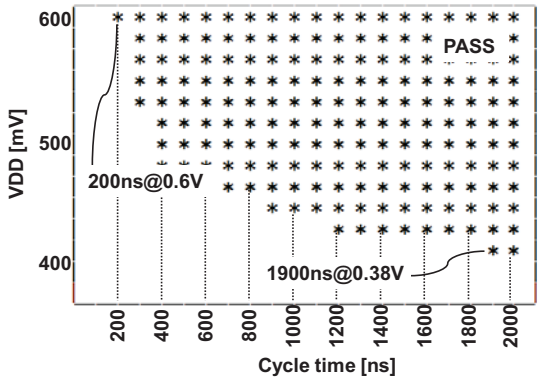

Fig. 13. Shmoo plot.

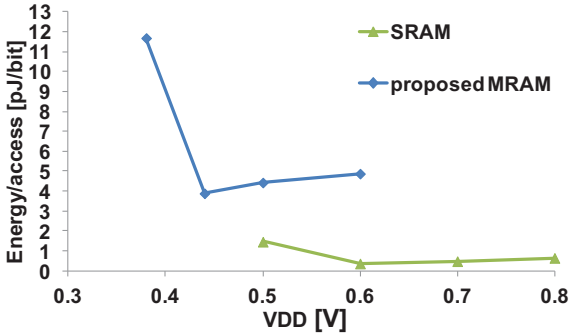

Fig. 14. Energy/bit comparison between the proposed STT-MRAM and the conventional SRAM.

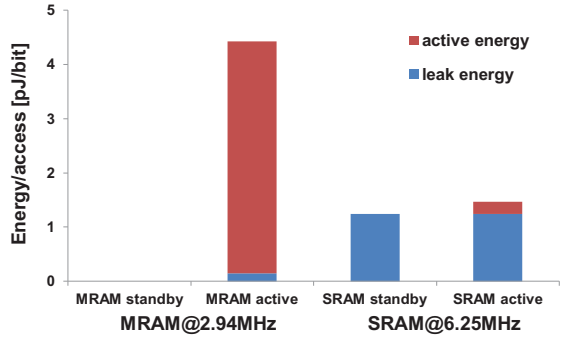

Fig. 15. Energy breakdowns in the STT-MRAM and SRAM at 0.5-V VDD.

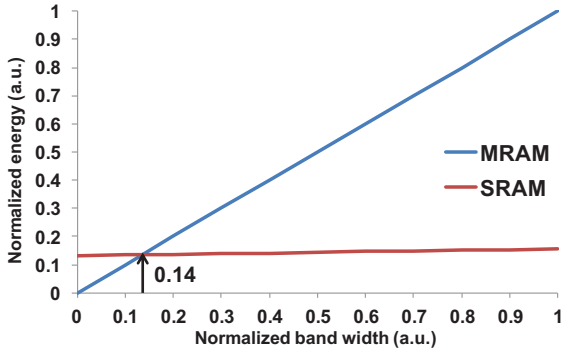

Fig. 16. Energy versus utilization of memory bandwidth in the STT-MRAM and SRAM.

TABLE I. Test chip characteristics

Process technology	65-nm bulk CMOS
Nominal voltage	1.2 V
Charge pump output	1.6 V
Capacity	8 Mb
Cell size	0.203 mm^2 (0.495×0.41 mm^2)
Operating VDD	0.38–0.6 V
Operating frequency	0.526–5.000 MHz
Operating power	6.15 µW at 0.526 MHz
Minimum energy per access	3.89 pJ/bit at 0.44 V and 1.66 MHz

IV. Summary

We presented a new sense amplifier with process variation tolerance for low-voltage operating STT-MRAM. The proposed sense amplifier can distinguish parallel states and anti-parallel states in all process corners. We fabricated an 8-Mb STT-MRAM in a 65-nm process technology. The test chip exhibits 0.38-V operation at a frequency of 0.526 MHz, where the power consumption is 6.15 µW. The proposed STT-MRAM operates at lower energy than the SRAM when a utilization of a memory bandwidth is 14% or less.

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