Analysis of Soft Error Propagation considering Masking Effects on Re-convergent Path

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Abstract— As technology nodes continue to shrink, the impact of radiation-induced soft error on processor reliability increases. Estimation of processor reliability and identification of vulnerable flip-flops requires accurate soft error rate (SER) analysis techniques. This paper presents a proposal for a soft error propagation analysis technique. We specifically examine single event upset (SEU) occurring at a flip-flop in sequential circuits. When SEUs propagate in sequential circuits, the faults can be masked temporally and logically. Conventional soft error propagation analysis techniques do not consider error convergent timing on re-convergent paths. The proposed technique can analyze soft error propagation while considering error-convergent timing on a re-convergent path by combinational analysis of temporal and logical effects. The proposed technique also considers the case in which the temporal masking is disabled with an enable signal of the erroneous flip-flop negated. Experimental results show that the proposed technique improves inaccuracy by 70.5%, on average, compared with conventional techniques using ITC 99 and ISCAS 89 benchmark circuits when the enable probability is 1/3, while the runtime overhead is only 1.7% on average.

Keywords- single event effect; single event upset; soft error propagation; logical masking; temporal masking

I. INTRODUCTION

Technology scaling degrades the critical charge, decreases operating voltage and increases the circuit scale on a chip. For those reasons, soft errors have come to occur easily in recent years [1]. Accurate soft error rate (SER) estimation is therefore necessary to design soft-error-tolerant processors. However, verifying the effectiveness of soft error mitigation techniques is difficult because processors have become extremely complicated. Radiation testing of fabricated test chip, which entails a great deal of time and cost, is conducted only for simple test circuits [2, 3]. Moreover, system-level verification by radiation testing is difficult. Consequently, a processor SER evaluation technique that uses no radiation testing is required.

In the past, soft errors in large SRAM arrays were regarded as the main contributor to processor SER. However, error correction code (ECC) with a bit-interleave structure can mitigate SRAM SER sufficiently [4]. In recent years, soft errors have come to occur in logic blocks, creating growing concern about processor reliability. [4, 5]. For soft error of logic blocks, we particularly examine single event upsets (SEUs) in flip-flops. Radiation-hardened flip-flops are affected by area and power overhead. Therefore, it is inefficient to apply soft error mitigation techniques uniformly to all flip-flops. Contributions to processor SER differs among flip-flops. Consequently, identifying those flip-flops susceptible to soft error can efficiently mitigate the impact of soft error on processors because developers can apply soft error mitigation techniques selectively to these flip-flops: softerror-tolerant and cost-effective processors can be designed.

Soft errors occur in flip-flops and propagate to downstream flip-flops through combinational circuits. There, the error might cause a primary output flip and system-level malfunction. The processor SER evaluation should be conducted using the following three steps: device-level soft error occurrence analysis, circuit-level propagation analysis, and system-level effect analysis [4]. As described herein, we propose an accurate analysis technique for soft error propagation. It evaluates the probability that an SEU occurring at a flip-flop flips the value in a downstream flipflop and thereby affects the primary output. Existing techniques are classifiable into fault injection techniques [6-9] and analytical techniques [4, 12-15]. Exhaustive fault injection techniques require vastly numerous input vectors. Fault injection simulation using comprehensive input vectors for a complicated circuit takes an enormous amount of time because the number of input vectors increases exponentially according to the number of primary inputs. Monte Carlo simulation using random input vectors cannot ensure that all circuit states are verified uniformly. FPGA-based fault injection for speed up [8, 9] cannot evaluate temporal masking effects depending on circuit delays. Analytical techniques estimate the state of the circuit probabilistically without test cases for each input vector sequence. They are suitable for the analysis of a complicated processor. First we describe an effect that cannot be evaluated using conventional analytical techniques. Then we propose an analytical technique that can evaluate the effect.

The remainder of this paper is organized as follows. Several masking effects and conventional SEU propagation analysis techniques are described in Section II. Section III explains problems of the conventional and proposed techniques. Section IV shows the experimental setup and results. Finally, Section V presents a summary of the results.

II. CONVENTIONAL METHODS FOR SOFT ERROR PROPAGATION ANALYSIS

Actually, SEUs in flip-flops do not always propagate to the downstream flip-flops. The possibility exists that SEUs are masked temporally and logically. These masking effects are respectively designated as temporal masking and logical masking. Therefore, the probability that the error propagates to the downstream flip-flop, defined as the Masking Factor (MF), is calculated as shown below.

$$MF = TMF \times LMF \tag{1}$$

Therein, the Temporal Masking Factor (*TMF*) is the error propagation probability considering temporal masking. The Logical Masking Factor (*LMF*) is the error propagation probability considering logical masking. Analytical techniques have been proposed, but the conventional technique evaluates these masking effects individually. This section presents a description of these two masking effects and conventional analysis techniques.

A. Temporal Masking

When an SEU occurs at a certain time in a clock cycle, the SEU cannot be sampled temporally at the downstream flipflops before the next clock edge. Therefore, the downstream flip-flop does not latch the error; the erroneous flip-flop latches error-free input data at the next clock edge. As a result, all error effects are masked in the circuit, as presented in Fig. 1. This masking effect is *temporal masking*, which depends on the occurrence timing of SEU and propagation delays between flip-flops. The probability of error propagation considering the temporal masking, TMF, is evaluated by the propagation delays between flip-flops [10]. TMF is the ratio of a vulnerable window (T_{error}) to a clock cycle (T_{cycle}) in Fig. 2. When an SEU occurs in the vulnerable window, the SEU can propagate to the downstream flip-flop temporally. In Fig. 2, t_{setup} and t_{hold} respectively denote the setup time and hold time of the downstream flip-flop. t_{prop} is the sum of the delays of the erroneous flip-flop and the combinational logic. α is the probability with which the SEU reaches to the downstream flip flop within the period of $(t_{setup} + t_{hold})$ and is latched. In this paper, α is set to 0.5 because we consider that the probability for latching the SEU decrease linearly from start of the setup time to end of the hold time. TMF_{org} is calculated as shown below.

$$TMF_{org} = \frac{T_{error}}{T_{cycle}} = \frac{T_{cycle} - t_{setup} - t_{prop} + \alpha(t_{setup} + t_{hold})}{T_{cycle}}$$
(2)

The propagation delays are evaluated using static timing analysis (STA).

B. Logical Masking

When an error propagates to a gate input with a value that does not affect the gate output logically (e.g. two-input AND gate when another input is "0"), the error is masked. This masking effect, *logical masking*, depends strongly on the input vector of the circuit. As described before, analytical techniques are practical for logical masking analysis [12–15].







Figure 2. Analytical technique for temporal masking.

An analysis technique using binary decision diagrams (BDD) analyzes the Boolean function of combinational logic and error propagation efficiently [12]. A technique proposed in an earlier report [13] evaluates the logical behavior of the circuit and the error propagation using a Probabilistic Transfer Matrix (PTM) and Ideal Transfer Matrix (ITM). In [14], error propagation considering logical masking is evaluated using error propagation rules with four-value logic. However, the accuracy of this technique degrades because of re-convergent paths because the signal correlation of errors is not considered on re-convergent paths. Chen proposed the Correlation Coefficient Method (CCM) considering signal correlation [15]. In this technique, error propagation is modeled as a function. The model is implemented by Boolean combinational logic and is connected to the circuit under evaluation. The error propagation considering logical masking is evaluated by the signal probability of the circuit. The signal probability, the probability p(x) that a signal x is "1", is calculated using a technique proposed in an earlier report [16]. This technique realizes fast and accurate error propagation analysis considering logical masking. As described in this paper, CCM is used for logical masking analysis, but the proposed technique is not restricted to the analysis technique.



Figure 3. Re-convergent path having two paths with different propagation delays.

C. Re-convergent Path

A re-convergent path comprises a series of two or more paths with a common source register or gate (divergent site) and a common sink register or gate (convergent site) as shown on the left side of Fig. 3. Generally, the propagation delay differs among paths, so the timing by which an SEU reaches a convergent site differs for each path. Figure 3 shows a case in which the SEU propagates through CL₀ and CL₁ and converges at a two input AND gate. Assuming that the propagation delay of CL₀ is longer than that of CL₁, a time region A exists when an SEU reaches only node j because of the difference of propagation delay. Then, whether an SEU is masked or not is determined by the logical function and inputs of the gate. The SEU from the divergent site exhibits causes node k only in region A in this case. When an SEU occurs at FF_a in a certain timing, the SEU might be sampled at FF_b in the next clock edge. To conduct accurate analyses of the masking effects for SEU propagation, a difference of propagation delay on the re-convergent path must be considered. However, conventional techniques do not consider masking effects on the re-convergent path [12-15].

III. PROPOSED ANALYSIS TECHNIQUE

A. Temporal Masking Disablement

Temporal masking can be disabled when data latching of the erroneous flip-flop is controlled by the enabling signal, as portrayed in Fig. 4. The disabled erroneous flip-flop does not latch error-free input data at the next clock edge; the error remains. The remaining error can propagate in the next clock cycle even if the error cannot propagate in the error occurrence cycle. In the next clock cycle, the error is affected only by logical masking without temporal masking because the error exists at the beginning of the cycle. Similarly, temporal masking can be disabled when the clock-gating scheme controls data latching of the erroneous flip-flop. Conventional individual analysis for temporal masking and logical masking cannot evaluate temporal masking disablement because the effect depends on the temporal and logical behavior of the circuit, which results in too optimistic analysis.

Temporal masking disablement can be evaluated by the probability that the erroneous flip-flop enables at clock edges, defined as p(enable). Actually, p(enable) is calculable by the signal probability because the enabled state depends on the logical behavior of the circuit. The signal probability is



Figure 4. Temporal masking disablement depending on the enabled state of the erroneus flip-flop.

calculated in the logical masking analysis. In the proposed analysis technique, *TMF* is compensated by p(enable) considering that the error is affected by temporal masking if the erroneous flip-flop enables and temporal masking is disabled if the flip-flop disables, as

$$TMF_{comp} = p(enable) \times TMF_{org} + (1 - p(enable))$$
(3)

where TMF_{comp} stands for the compensated error propagation probability considering enable state of erroneous flip-flop and TMF_{org} signifies the probability calculated using eq. (2).

B. Masking Effects on Re-convergent Path

The impact of masking effects on the re-convergent path depends on logical masking and temporal masking. Therefore, we propose a soft error propagation analysis technique that calculates LMF with considering temporal masking effects based on conventional logical masking factor analysis [15]. In the conventional technique, the LMF of output of a gate is calculated using LMF and the signal probability of inputs of the gate. However, the proposed technique uses the product of LMF and TMF of input of the gate instead of LMF. Multiplying TMF means that LMF is corrected by considering the effects of the difference of convergent timing, which are treated as simultaneous in logical masking analysis. For example, a re-convergent path exists that comprises a path with a small TMF and another path with large TMF. Small TMF means that the propagation delay is large. Therefore, multiplying smaller TMF is equal to delay the convergent timing more. In this way, propagation probability is fixed according to propagation delay on each path and error convergent timing on re-convergent path is considered.

1) Method

The proposed technique requires multiplication of the node-proper TMF to calculate the error propagation probability at each node. Consequently, TMF between flip-flops, which is obtainable using Eq. (2), is divided into node-proper TMFs. The TMF division method is described later. The node-proper TMF is designated as the divided TMF. The method that calculates the MF of each node is presented in this subsection. In conventional techniques, the signal probability and LMF of each node are calculated successively from the



Figure 5. Calculation flow using the proposed technique.

primary inputs and/or outputs of flip-flops to primary outputs and/or inputs of flip-flops in order. Using the proposed technique, after evaluating LMF(i), which is the LMF at node *i*, MF(i) is calculable by multiplying LMF(i) and TMF(i). MF (i) represents the probability that SEU propagates to node i without being masked logically or temporally. Then, LMF of the downstream gate output is calculated using MF calculated earlier. The calculation flow is presented in Fig. 5. $MF(n_{-0})$ is calculated by multiplying $TMF(n_0)$ and $LMF(n_0)$, which is 1.0 when FF_a is a erroneous flip-flop. $LMF(n_{l})$ is calculated from the signal probability of the input of gate g_1 and $MF(n_0)$ using the conventional method. Then, $MF(n_{l})$ is calculated by multiplying $LMF(n_{l})$ and $TMF(n_{l})$. These calculation flows are repeated for primary outputs and inputs of downstream flip-flops. Eventually, we can calculate the error propagation probability for a flip-flop considering temporal masking and logical masking on a re-convergent path.

2) Divided TMF

As described above, divided *TMF* is used to calculate *MF* at each node. Divided *TMF* of input signal of a gate g (*TMF(i*)) is the probability that a bit-flip occurring on node *i* propagates to the output of gate g_i by the next clock edge. Let $n_0, n_1, ...$, be nodes on the path between erroneous flip-flop and downstream flip-flop in order starting from the near side of the erroneous flip-flop. Then, the divided *TMF* of output n_0 of erroneous flip-flop is

$$TMF(n_{-0}) = \frac{T_{base} - delay(FF_{SEU})}{T_{cycle}}$$
(4)

where $delay(FF_{SEU})$ is the erroneous flip-flop delay, and T_{base} is *TMF* assuming no delay between FFs. In other words, T_{base} is T_{error} when t_{prop} is 0. Subsequently, the divided *TMF* of node n_i on path between the erroneous flip-flop and downstream flip-flop is calculation by Eq. (5).

$$TMF(n_{-i}) = \frac{T_{base} - delay(FF_{SEU}) - delay_out(n_{-i})}{T_{base} - delay(FF_{SEU}) - delay_out(n_{-i})} \quad (i \ge 1)$$
(5)

In that equation, $delay_out(n_i)$ is a propagation delay from the erroneous flip-flop to node n_i ; $delay_in(n_i)$ is a propagation delay from erroneous flip-flop to input of gate with output n_i . When the calculation is performed according to Eqs. (4) and (5), the product of all divided *TMFs* corresponds to *TMF*_{org}. In the case of Fig. 5, the product of *TMF*(n_{-0}), *TMF*(n_{-1}), *TMF*(n_{-2}) and *TMF*(n_{-4}) corresponds to *TMF*_{org}. The divided *TMF* should be compensated by Eq. (3) to consider temporal masking disablement. The *delay*(*FF*_{SEU}), *delay_in*(n_{-i}), and *delay_out*(n_{-i}) are obtainable using a static timing analyzer (STA).

IV. EXPERIMENT

The proposed technique can accurately analyze the soft error propagation probability considering masking effects on a re-convergent path and temporal masking disablement. No conventional technique considers these effects.

A. Experimental Setup

The proposed technique is applied to sequential circuit benchmarks ITS 99 and ISCAS 89 for experiment. The circuits are synthesized using a 65 nm CMOS library. In this evaluation, the circuit from the erroneous flip-flop to the downstream flip-flop is extracted from the benchmark circuit because Monte Carlo simulation is difficult for sequential circuits, as described in section I. Monte Carlo simulation can evaluate the extracted circuit because it is substantially a combinational circuit. The LMF of each node is evaluated using the correlation coefficient method (CCM) [15] because the method can evaluate LMF rapidly and accurately. The signal probability of primary inputs is 0.5, except for the reset and enable signal. If actual signal probabilities are required for primary inputs of a circuit, the signal probabilities can be got by logic simulation in advance. The TMF of each node is calculated using Eqs. (2), (3) and (4). We use Synopsys Design Compiler as the Static Timing Analyzer to calculate the propagation delay of gates and flip-flops. p(enable) is assumed. Monte Carlo simulation is done using gate-level circuit annotated delay information. The SEU is injected randomly in the unit of 1 ps in a cycle. We use Monte Carlo simulation with 1,000,000 test cases for each benchmark circuit while the input vector and SEU injection timing are varied.

B. Results

This section presents a comparison of the accuracy of error propagation probability as evaluated using the conventional technique and the proposed technique. The accuracy is evaluated using the *Absolute Error* (*AE*) and *Mean Absolute Error* (*MAE*) as shown below.

$$AE(i) = MF_{sim}(i) - MF(i)$$
(6)

$$MAE = \frac{1}{N} \sum_{i} |AE(i)| \tag{7}$$

Therein, N stands for the number of pairs of the erroneous flip-flop and the downstream flip-flop, MF(i) represents the error propagation probability evaluated by the analytical techniques for pair *i*, and $MF_{sim}(i)$ denotes the probability evaluated using the Monte Carlo simulation for pair *i*.

Figure 6 presents experimentally obtained results without temporal masking disablement ((a) p(enable) = 1.0) and with p(enable) set to 1/3 (b) using ITC 99 benchmark circuit b01. In Fig. 6, the x axis shows the names of the erroneous flip-flop and the downstream flip-flop; the y axis shows AE. The proposed technique improves the average AE by 47.3% and 78.9% when the respective p(enable) are 1.0 and 1/3. In Fig. 6(a), AE of path between stato[0] and outp is unchanged because the path does not include a re-convergent path. When p(enable) is 1.0 and 1/3, the AE of path between stato[0] and stato[0] is worse because of inaccuracy inherent in the logical masking analysis technique. MAE evaluation for ITC 99 and ISCAS 89 benchmark circuits is depicted in Fig. 7. Compared with the conventional technique, the proposed technique improves average MAE by 37.8% and 70.5%, respectively, when p(enable) is 1.0 and p(enable) is 1/3. The proposed technique improves MAE for all circuits. The conventional technique underestimates the propagation probability of flipflops with low p(enable) because the temporal masking disablement is not considered. Thus the smaller p(enable) is, the more the proposed technique improves the accuracy. The proposed technique requires more analysis time than the conventional technique to calculate MF using circuits annotated with divided TMF. We evaluate the runtime





Figure 6. Absolute Error of the experimentally obtained result for b01 using conventional and proposed techniques when (a) p(enable) is 1 and (b) *p*(*enable*) is 1/3.



Figure 7. Mean Absolute Error of the experimentally obtained result obtained using the conventional technique and the proposed technique when (a) p(enable) is 1 and (b) p(enable) is 1/3.

(b)

600

521

Benchmark Circuits

b02

601

Average

s298

s208

0.04

0.02

0

Table 1. Runtime overhead from the proposed techniques

Benchmark Circuits	Analysis Technique	Evaluation Time [s]	Normalized Evaluation Time
b01	Conventional	7.073	1.000
	Proposed	7.173	1.014
b02	Conventional	6.966	1.000
	Proposed	7.030	1.009
b06	Conventional	15.82	1.000
	Proposed	16.10	1.018
s208	Conventional	39.82	1.000
	Proposed	40.56	1.019
s298	Conventional	70.12	1.000
	Proposed	71.32	1.017
Average	Conventional	27.96	1.000
	Proposed	28.44	1.017

overhead for analysis. The results for each benchmark circuit are shown in Table 1. The maximum runtime overhead is 1.9% for s208. The average is 1.7%, so the runtime overhead is insignificant. The experimentally obtained results demonstrate that the proposed technique can perform more accurate analysis than conventional technique by considering masking effects on re-convergent path and temporal masking disablement with slight runtime overhead. Thereby, the proposed technique is useful for identifying flip-flops susceptible to soft error.

V. CONCLUSION

This paper presents a proposal for an accurate soft error propagation analysis technique for processor soft error rate evaluation. Conventional analysis techniques evaluate temporal and logical effects individually. They do not consider temporal masking and logical masking effects on the re-convergent path and temporal masking disablement. The proposed technique evaluates soft error propagation probability through combinational analysis of temporal and logical effects. Experimentally obtained results demonstrate that the proposed technique achieves 70.5% better accuracy of the error propagation probability, on average, than the conventional technique when the enabled probability of the erroneous flip-flop is 1/3. Consequently, the proposed technique can evaluate the soft error propagation more accurately and identify flip-flops susceptible to soft error.

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