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PAPER Special Section on Analog Circuits and Related SoC Integration Technologies

An I/O-Sized ADC with Second-Order TDC and MOM Capacitor Voltage-to-Time Converter*

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SUMMARY We present an I/O-size second-order analog to digital converter (ADC) combined with a time-to-digital converter (TDC) and a voltage-to-time converter (VTC). Our proposed VTC is optimized for metal–oxide–metal (MOM) capacitances, and is charged to the MOM capacitances by an input voltage. In a standard 65-nm CMOS process, a signal to noise and distortion ratio (SNDR) of 50 dB (8 bits) is achievable at an input signal frequency of 78 kHz and a sampling rate of 20 MHz, where the respective area and power are 6468 mm^2 and 509 μW. The measured maximum integral nonlinearity (INL) of the proposed ADC is −1.41 LSBs. The active area of the proposed ADC is smaller than an I/O buffer. The proposed ADC is useful as an ADC I/O.

key words: *ADC, I/O-size, VTC, MOM capacitance*

1. Introduction

Various techniques have been developed to realize ubiquitous computing for sensors. With implementation of more sensors, more analog-to-digital converters (ADCs) are required by the many sensors to digitize the many channel signals [1], [2]. To date, the ADCs on an LSI chip have been limited numerically by the chip area. To achieve high accuracy, for instance, an SAR ADC requires large capacitors for which the area cannot be scaled down with process scaling.

Figure 1 presents the points of emphasis of this work. We propose a smaller ADC than an I/O buffer size. We adopt a time-to-digital converter (TDC) suited to multiple-channel applications because it can be configured by digital circuits and because it can be extended easily to advanced CMOS process node. However, the small-area TDC, which can be realized within performance constraints at a low cost, needs an external circuit to convert an analog signal to a time-domain signal. Several voltage-to-time converters (VTCs) have been reported, one of which is a combination of a current-starved inverter and a capacitor [3]–[5] in Fig. 2(a). Another VTC uses a voltage-to-delay line comprised of the current-starved inverters [6]–[8] in Fig. 2(b). The current-starved inverter controls its output pulse width based on an analog input voltage (V_{IN}) applied to MN2, and thus can be implemented in a small area; its linearity is, however, strongly affected by the gate-source voltage. The high-linearity range is narrow, which results in a small input voltage range.

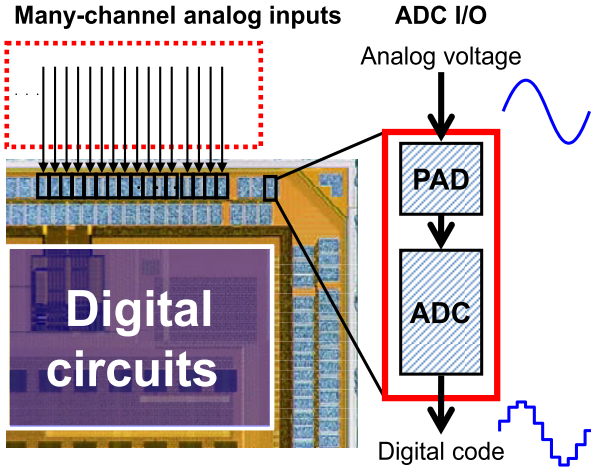

Fig. 1 ADC I/Os for multiple-channel analog inputs.

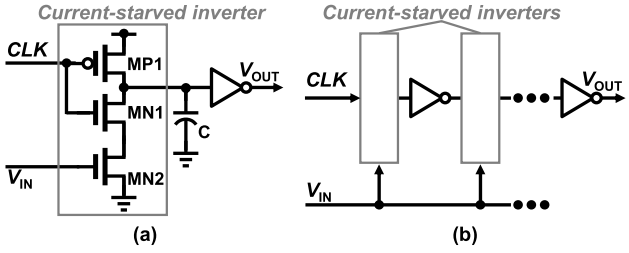

Fig. 2 Conventional VTC circuits.

To achieve a small area yet a large input voltage range, we propose a new VTC using metal–oxide–metal (MOM) capacitances in the next section. Our proposed VTC achieves a large input voltage range by charging the MOM capacitance and detecting its discharging time. Although the MOM capacitances require a certain area on higher metals, ADC circuitry can be accommodated under the MOM capacitances; thus, an area overhead is minimized. We explain an I/O-sized ADC architecture with the proposed VTC in Section 3. Measured results with a test chip are described in Section 4. In Section 5, we discuss the nonlinearity in the proposed ADC. The final section summarizes this paper.

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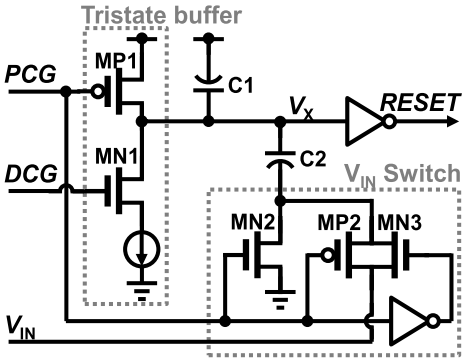

Fig. 3 Schematic of the proposed voltage-to-time converter.

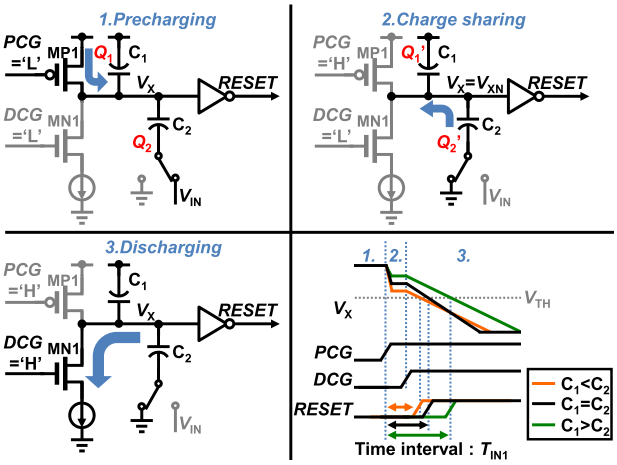

Fig. 4 Operation of the proposed VTC core circuit.

2. Proposed Voltage-to-time Converter Core Circuit

A schematic of our proposed VTC core is depicted in Fig. 3. Our proposed VTC circuit, which consists of two MOM capacitances, converts V_{IN} to a time interval. The circuit changes a discharging charge by V_{IN}. The two MOM capacitances, C_1 and C_2, are connected with the supply voltage (VDD) and a V_{IN} switch circuit. The V_{IN} switch circuit propagates a V_{IN} analog voltage or the ground (VSS) to C_2. Therefore the charge amount of C_2 is changed by V_{IN}. A tristate buffer includes a current source. The non-overlap signals (DCG and PCG) control the C_1 and C_2 charges and discharges.

Figure 4 shows the mechanism and the timing diagram of proposed VTC core circuit. First, while DCG and PCG are 'low,' the pMOS transistor (MP1) charges V_X to VDD; the charge on V_X is a sum of the charges of C_1 and C_2 represented as

$$Q_1 + Q_2 = 0 + C_2 \cdot (VDD - V_{IN}), \quad (1)$$

where Q_1 and Q_2 are charges of C_1 and C_2. Next, when the PCG becomes 'high,' the V_{IN} switch is flipped from V_{IN} to VSS. The charges of C_1 and C_2 are shared at V_X. Therefore,

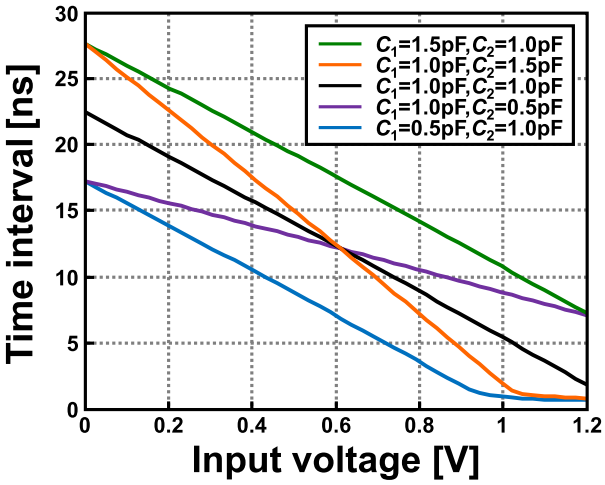

Fig. 5 Simulation result of the VTC core.

its voltage is controlled by V_{IN} as

$$Q_1' + Q_2' = C_1 \cdot (V_{XN} - VDD) + C_2 \cdot (V_{XN} - VSS), \quad (2)$$

where V_{XN} is a stable voltage after PCG becomes 'high.' Eventually, from (1) and (2), V_{XN} can be given as

$$V_{XN} = VDD - \frac{C_2}{C_1 + C_2} \cdot V_{IN}. \quad (3)$$

The charge amount is defined by the capacitances of C_1 and C_2, and the voltage of V_{IN}. Next, DCG becomes 'high,' and the nMOS transistor (MN1) and a current source discharges the charge. When V_X becomes lower than a threshold voltage (V_{TH}) of the inverter, $RESET$ becomes 'high.' From (3), the interval in which V_X becomes lower than V_{TH} depends on V_{XN} and depends on the time at which the rising edge of $RESET$ is changed. Therefore, this VTC core circuit can convert the voltage domain to the time domain.

Figure 5 presents the SPICE simulation result of the proposed VTC core circuit. The vertical axis is the time interval from the rising edge of PCG to the rising edge of $RESET$. The horizontal axis is the analog input voltage V_{IN}. In this simulation, V_{IN} is swept from 0 V to 1.2 V. As C_1 and C_2 become larger, the input voltage range and the conversion gain are enlarged, respectively; the larger capacitances, however, occupy a large area. Hence, there is a trade-off between the input voltage range, the conversion gain, and the area. To achieve a 1.0-V input voltage range and a 25-ns time interval (note that the time interval is limited to a half of a sampling period in our design, which is 25 ns.), we take $C_1 = C_2 = 1$ pF. The output characteristic is not completely linear because the discharging speed of the current source is not perfectly constant. To eliminate the nonlinearity characteristics, the proposed ADC has a nonlinearity corrector (see the next section).

3. I/O-Sized ADC with Proposed VTC

We propose an IO-sized ADC that consists of the small area

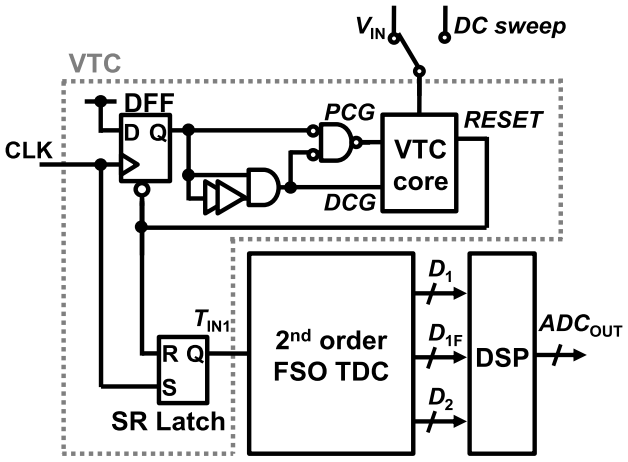

Fig. 6 Proposed I/O-sized ADC architecture.

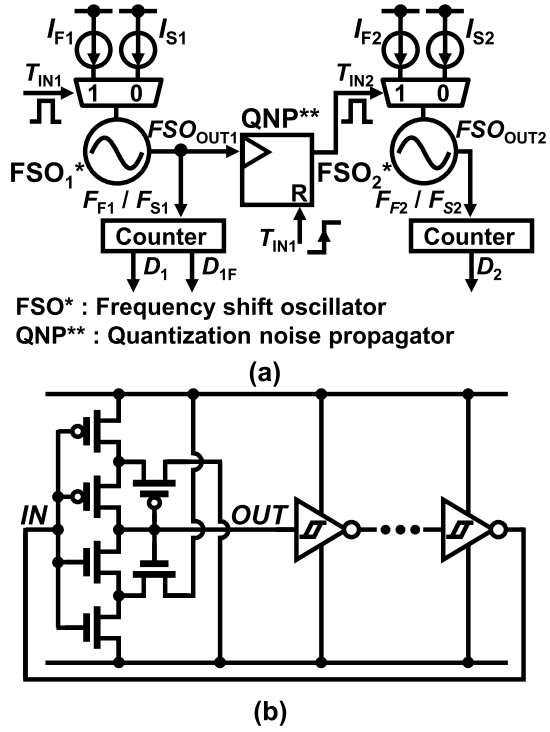

Fig. 7 Schematics of (a) FSO TDC and (b) Schmitt trigger inverter ring.

VTC and a frequency shift oscillator (FSO) TDC [9], as presented in Fig. 6. The VTC generates non-overlap signals, *DCG* and *PCG*, using a clock signal (*CLK*) to control the VTC core circuit. An SR Latch connected to the VTC core circuit outputs the time interval, T_{IN1} (time from the rising edge of *CLK* ($\approx$ *PCG*) to the rising edge of *RESET*), as explained in the previous section. The VTC core circuit is precharged again by its own *RESET*. In doing so, it is possible to make the circuit operation fast and to prepare for the next *CLK* pulse.

Figure 7(a) shows the architecture of the second-order $\Delta\Sigma$ FSO TDC. T_{IN1} is converted to digital values (D_1 and D_{1F}) by the first-stage FSO TDC (FSO_1), which oscillates at a low frequency (F_{F1}) or high frequency (F_{S1}).

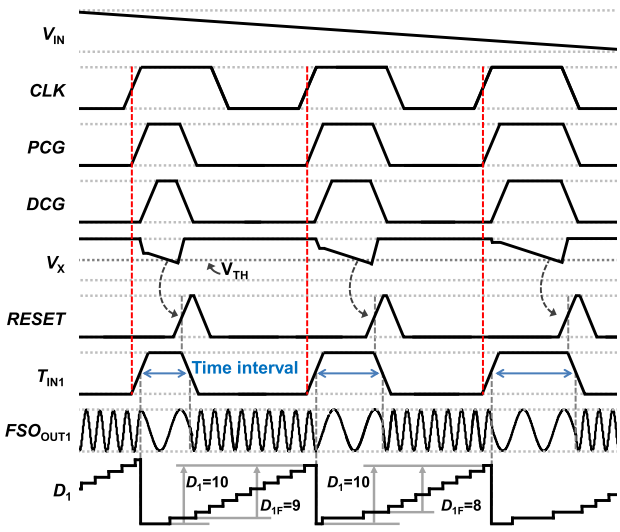

Fig. 8 Schematic of FSO and Schmitt trigger inverter ring.

The FSO TDC has a first-order noise shaping characteristic and achieves higher-order noise shaping by propagating its quantization noise to the next-stage FSO TDC: The quantization noise propagator (QNP) propagates the quantization noise to the next-stage FSO TDC. The QNP output (T_{IN2}) includes the previous quantization noise, which is digitized as a digital code (D_2) by the second-stage FSO TDC. The digital signal processor (DSP in Fig. 6) after the FSO TDCs calculates the final digital output (ADC_{OUT}) from D_1, D_{1F}, and D_2 [9]. After converting an analog voltage to the digital code, the ADC can correct its nonlinearity using the DSP because the VTC characteristic is monotonic.

In the FSO TDC, the performance is affected by a timing jitter in the inverter of the oscillator, which determines its noise floor. To reduce the timing jitter, enlarging a transistor size in the oscillator is an effective way [10]; a circuit area and power are, however, increased. Instead, we adopt an FSO comprised of Schmitt trigger inverters, as illustrated in Fig. 7(b), which can absorb a power supply noise and reduce its jitter [11].

Figure 8 shows the operating waveforms of the proposed ADC. When CLK becomes 'high,' the DFF outputs 'high' for *PCG* and *DCG*. After *DCG* enables 'high,' V_X begins to be discharged toward *VSS*; V_X is, however, precharged on the way again by a trigger of *RESET* pulse when V_X crosses V_{TH}. Then, T_{IN1} becomes 'low.' That is, the SR latch generates the output pulse (T_{IN1}: time from the rising edge of *CLK* to the rising edge of *RESET*). The T_{IN1} width is defined by V_{IN}. After the VTC converts V_{IN} to T_{IN1}, the FSO TDC converts T_{IN1} to a digital code using a frequency difference.

After converting to the digital code with the ADC, the DSP corrects the VTC nonlinearity and suppresses harmonic noises. To correct the ADC output, the DSP needs the voltage to digital characteristic. The ADC is applied a ramp signal at an initial calibration phase. Figure 9 shows the ADC characteristic of the SPICE simulation result. The

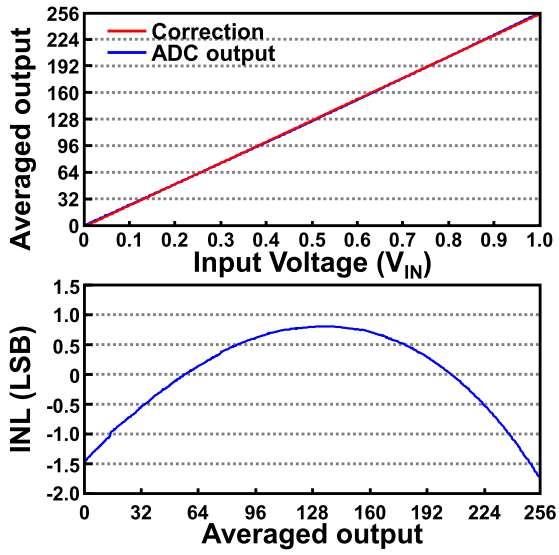

Fig. 9 Characteristics of the original ADC output and calculation.

blue line shows the averaged ADC output at a sampling rate of 20 MHz with 500 kHz low-pass filtering. The red line is an approximation straight line of the blue line. The integral non-linearity (INL) in the figure shows the deference of the blue and red line. The coefficients of the nonlinearity correction for the DSP are obtained by the DC sweep in Fig. 6 at the initial calibration phase. By correcting the ADC output with this method, the DSP cancels the harmonic noise.

4. Measurement Results

A test chip was made using a 65-nm CMOS process (Fig. 10). The VTC occupies 6468 μm^2 as an active area. The MOM capacitance consists of higher metal to put in the FSO TDC under the VTC. The MOM capacitance needs somehow large area; however the ADC needs no additional area without the VTC because the MOM capacitance consists of the higher metals. A digital input I/O in a 65 nm occupies 6800 μm^2. The proposed ADC is 95.1% of the digital I/O, and is useful as an ADC I/O to convert a signal from analog to digital. The total power consumption is 509 μW.

Figure 11 shows the measured output spectra of the proposed ADC. In the spectra, the input signal frequency is 78 kHz at a 20-MHz sampling rate. The original signal-to-noise and distortion ration (SNDR) in Fig. 11 is 43 dB at a bandwidth of 500 kHz and a spurious free dynamic range (SFDR) is 45 dB. The harmonics of ADC are produced by the nonlinearity of the VTC. After making the nonlinearity correction, the SFDR is improved to 58 dB, and the SNDR is improved to 50 dB, which exhibits an 8-bit resolution ADC.

Next the INL of the proposed ADC is measured by applying a ramp input. The input range is from 0.0 V to 1.0 V. The measured result of the DC transfer curve at a sampling rate of 20 MHz with 500 kHz low-pass filtering is shown in Fig. 12. The measured maximum INL is −1.41 LSBs.

The test chip performance is summarized in Table 1 and Fig. 13. Our purpose is the area reduction of the ADC.

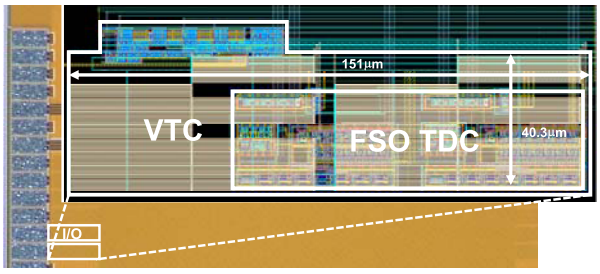

Fig. 10 Micrograph of the proposed ADC chip.

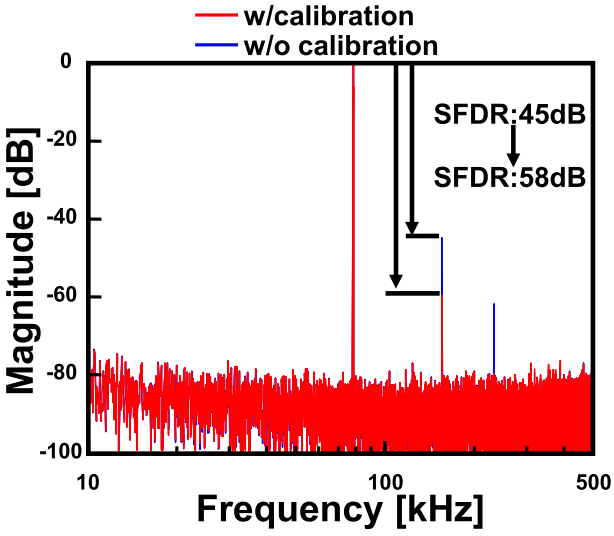

Fig. 11 Output spectra of IO-sized ADC w/o calibration and w/calibration.

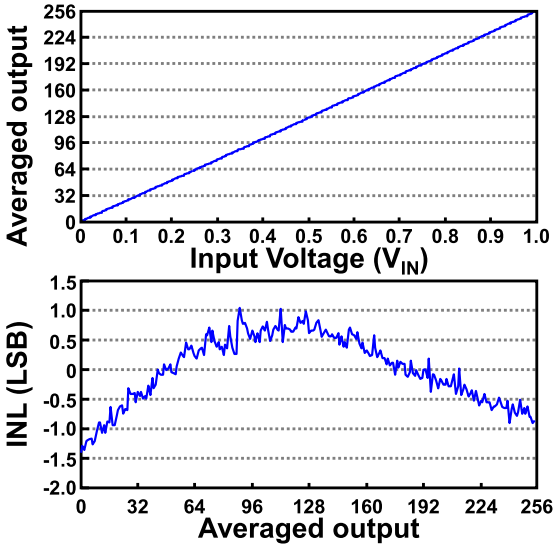

Fig. 12 Measured static performance. (a) DC transfer, (b) INL.

Therefore, we compare area-FoMs of other state-of-the-art ADCs [12]. Our proposed ADC exhibits better area-FoM among the near-bandwidth ADCs.

Table 1 Chip Characteristics.

Item	This work		[9]	[10]
Technology (nm)	65		90	40
Band width (kHz)	500		500	550
Sampling rate (MS/s)	20		96	1.1
Power (mW)	VTC	0.228	2.6	0.0012
	TDC	0.281		
	Total	0.509		
SFDR (dB)	58		N/A	N/A
SNDR (dB)	50		76	46.8
ENOB (bits)	8.0		12.3	7.5
Active area (mm^2)	0.0065		0.4	0.012
Power-FoM (fJ/conv.step)*	1970		504	6
Area-FoM ($mm^2 \cdot$ ps/conv.step)**	23		78	49

$^{*}Power-FoM = \frac{Power}{2 \cdot BW \cdot 2^{ENOB}}$ $^{**}Area-FoM = \frac{Area}{2 \cdot BW \cdot 2^{ENOB}}$

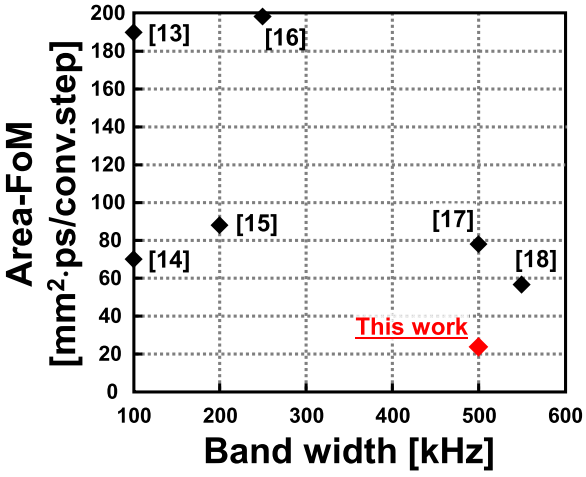

Fig. 13 Comparison with other state-of-the-art ADCs.

5. Effects of the Nonlinearity

The resolution of the ADC is lower than that of [9] because of the nonlinearity characteristics. The reason of the nonlinearity is the current source in the proposed VTC. The timing diagram considering the drain-source current (I_{DS}) characteristic is shown in Fig. 14. The gray line shows the timing diagram with the ideal current source, in which case I_{DS} stays at a fixed amount. The proposed VTC core, however, has nonlinearity because of its unstable current source.

Figure 15 shows the ADC output spectra, using the SPICE and MATLAB simulation result. The simulation without the ideal current source and the correction (section 3) has the harmonic noise because the VTC has nonlinearity. On the other hand, the characteristic of the VTC with the ideal current source achieves better linearity and the simulation result has no harmonic noise. To improve the proposed ADC, the I_{DS} characteristic of the current source must be carefully redesigned.

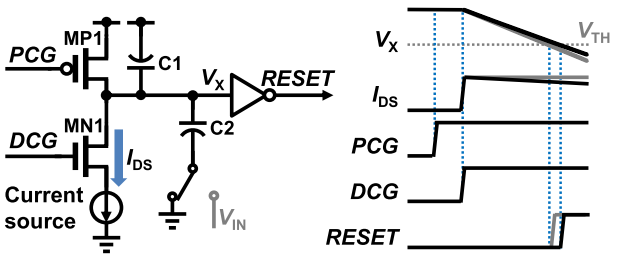

Fig. 14 Timing diagram of the VTC core circuit with considering the effects of the I_{DS} characteristic.

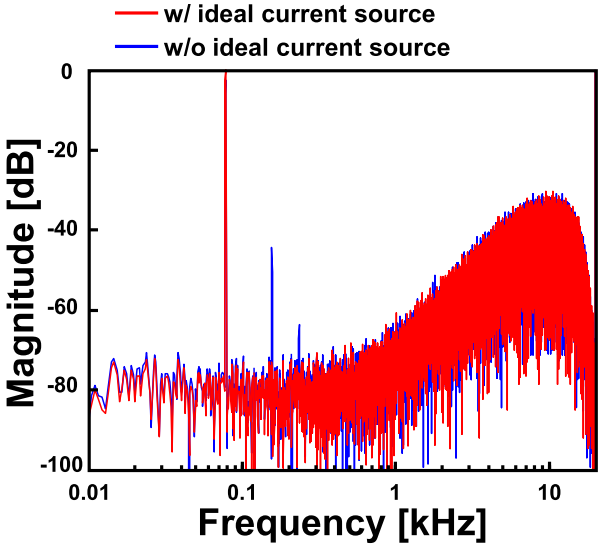

Fig. 15 Simulation result with the ideal current source.

6. Conclusion

We described a 50-dB I/O-sized second-order ADC. The proposed architecture obviates analog circuits such as opamps and switched capacitors. The proposed VTC is especially affected by the I_{DS} characteristic of the current source. By improving the current source, the proposed ADC would achieve higher resolution. The proposed ADC thereby maintains scalability with future advanced processes. As process technology advances, the ring oscillator frequency is expected to increase, which will be beneficial for the proposed ADC. A three-order or multiple-order ADC will be possible in our proposed ADC architecture.

Acknowledgments

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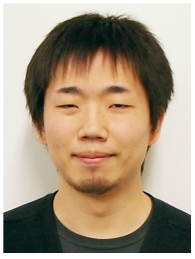

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