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An Ultra Low Power Motion Estimation Processor for MPEG2 HDTV Resolution Video

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SUMMARY This paper describes an ultra low power, motion estimation (ME) processor for MPEG2 HDTV resolution video. It adopts a Gradient Descent Search (GDS) algorithm that drastically reduces required computational power to 6 GOPS. A SIMD datapath architecture optimized for the GDS algorithm decreases the clock frequency and operating voltage. A low power 3-port SRAM with a write-disturb-free cell array arrangement is newly designed for image data caches of the processor. The proposed ME processor contains 7-M transistors, integrated in 4.50 mm × 3.35 mm area using 0.13 μm CMOS technology. Estimated power consumption is less than 100 mW at 81 MHz@1.0 V. The processor is applicable to a portable HDTV system.

key words: *HDTV, MPEG, motion estimation processor, Gradient Descent Search algorithm, SIMD datapath architecture*

1. Introduction

The international video compression standard, MPEG2, is a key-technology in building digital video applications. MPEG2 applications such as digital TV are expanding to include High Definition TV resolution, as well as Standard Definition TV. HDTV resolution monitors are becoming more widely used in the home. Therefore, portable HDTV systems such as the MPEG camera will continue to gain popularity.

Figure 1 shows a block diagram of an MPEG video encoder. The conventional motion estimation technique requires more than 90% performance of the encoder. It requires about 1000 GOPS to operate the HDTV resolution video system. A highly efficient ME processor is essential to realize a high quality and low power MPEG codec in the system.

Figure 2 shows the power consumption trend of an ME processor. The power consumption in the 0.13 μm processor developed with the conventional technology is more than 1200 mW even for 1/4 sub-sampling technique. Power consumption is prohibitively large for portable products. The objective of this work is to produce a very low power motion estimator for the HDTV resolution video system.

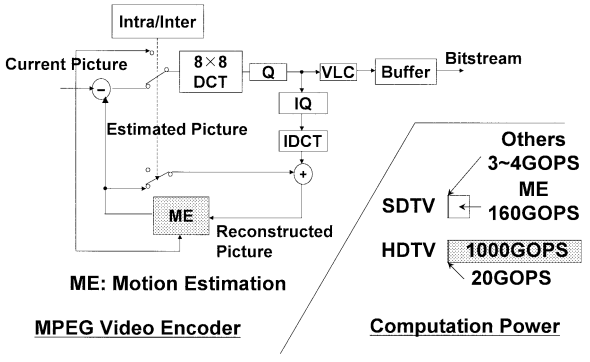

Fig. 1 MPEG encoder block diagram.

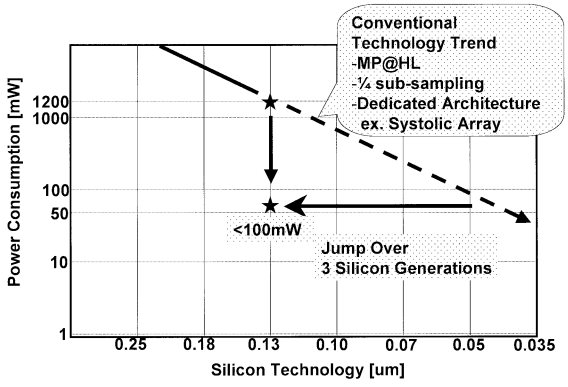

Fig. 2 ME processor power consumption trend.

Many MPEG2 codec LSIs have been reported [1]–[4]. These LSIs perform MP@ML video encoding; several LSIs can also perform MP@HL video encoding. Unfortunately, they usually cannot perform motion estimation for HDTV resolution video with a single chip configuration. Several MPEG4 codec LSIs adopt fast motion estimation algorithms and reduce power consumption [6], [7]. They can handle QCIF or CIF resolution video, but usually leave HDTV resolution video out of consideration. A low power ME processor useful

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for a portable HDTV system has not been reported.

This paper proposes a novel algorithm, architecture and circuit design technique for a motion estimation processor dedicated to a portable HDTV system that requires very low power consumption. Features of the newly developed ME processor are as follows:

- The GDS algorithm [5] is introduced for motion estimation. The GDS algorithm realizes motion estimation for HDTV resolution video only using 6 GOPS computational power, while the conventional search algorithm requires about 1000 GOPS.
- A SIMD datapath architecture optimized for the GDS algorithm is designed. The SIMD datapath contains 32 processing elements (PE). It can calculate the mean square error (MSE) in 8 cycles per macro block (MB). Its performance is 10 GOPS at 81 MHz@1.0 V. It operates at low frequency and low voltage, so its power consumption is quite low.
- The 32 Kb 3-port SRAM macro that has a write-disturb-free cell arrangement with a symmetrical memory cell layout is newly introduced. Estimated power consumption of this SRAM macro is 1.32 mW at 1.0 V and 81 MHz.

2. Algorithm

2.1 GDS Algorithm

Figure 3 shows an example of the distortion function over the search area for the GDS algorithm. The criterion of the function is the mean square error of a macro block indicated by a motion vector. The next search starts toward a direction that produces the steepest gradient of the function. The vector with the minimum function value over the search area is the solution to the procedure.

Figure 4 illustrates the searching procedure by the GDS algorithm. Technical terms are defined here to describe the GDS algorithm. "Template buffer" (TB) is a memory that stores a MB pixel data in a current frame. "Search Window Buffer" (SW) is a memory that stores pixel data in the previous frame. Brightness of the pixel that is located in $TB(i, j)$ is described as $TB_{i,j}$. The search vector is described as (Vx, Vy). The GDS algorithm is described as follows:

Step1. Decide start vector

Calculate MSE for the following four vectors. Start searching from the vector that has the smallest MSE among them.

1. 0 vector
2. The left MB motion vector
3. The upper MB motion vector
4. The motion vector of the MB that is located in the same position of the previous frame.

Here, MSE is defined as:

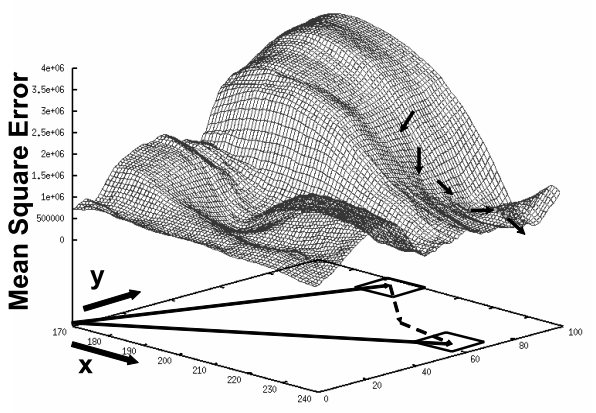

Fig. 3 Distortion function over the search area.

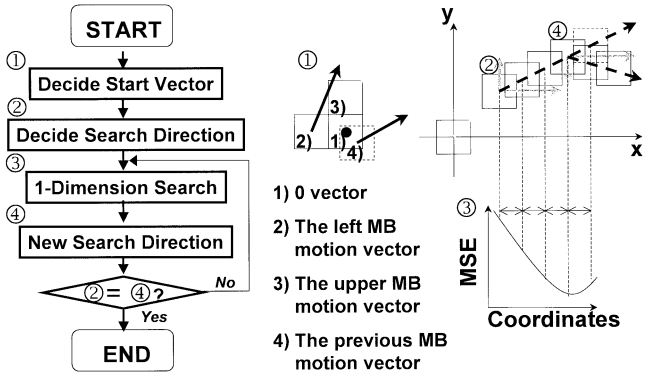

Fig. 4 GDS algorithm.

$$E = \sum_i \sum_j (TB_{i,j} - SW_{i+Vx,j+Vy})^2. \tag{1}$$

Step2. Decide search direction

Calculate x and y differential coefficients of the distortion function at the point indicated by the start vector.

$$\frac{\partial E}{\partial x} = \sum_i \sum_j (TB_{i,j} - SW_{i+Vx,j+Vy}) * (SW_{i+1+Vx,j+Vy} - SW_{i-1+Vx,j+Vy}) \tag{2}$$

$$\frac{\partial E}{\partial y} = \sum_i \sum_j (TB_{i,j} - SW_{i+Vx,j+Vy}) * (SW_{i+Vx,j+1+Vy} - SW_{i+Vx,j-1+Vy}) \tag{3}$$

$$\tan\theta = \frac{\frac{\partial E}{\partial y}}{\frac{\partial E}{\partial x}} \tag{4}$$

Step3. 1-Dimensional Search

- Search vectors toward the direction θ with step width λ.
- Continue to search vectors until MSE increase.
- The vector whose MSE is minimum is a temporary

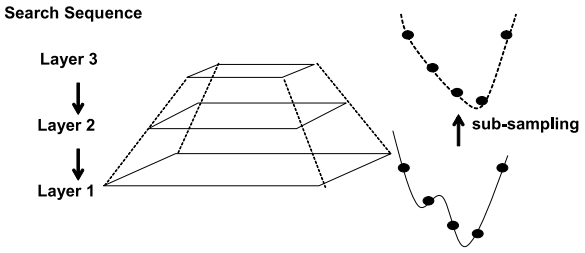

Fig. 5 Hierarchical GDS algorithm.

solution.

Step4. Decide to repeat or not

- Calculate differential coefficients and new direction θ' at the point obtained in Step3.
- If θ does not equal to θ', then go to Step3, and search in the new direction θ'.
- If θ equals to θ', finish the procedure. The latest temporary solution is taken as the final solution.

The simple GDS algorithm as above has a tendency to fall in a local minimum solution. It is effective to add a hierarchical search method in order not to fall in a local minimum, because a smoothing effect in an upper layer removes a noise effect and make it possible to search vectors in a long distance. The hierachical GDS algorithm is illustrated in Fig. 5. The hierarchical GDS algorithm is applied for three image layers. Layer 1 is the original picture. Layer 2 is obtained by 1/4 sub-sampling of layer 1, and layer 3 is obtained by 1/4 sub-sampling of layer 2. The hierarchical GDS algorithm starts searching in layer 3. This is followed by searching in layer 2 and layer 1.

2.2 Picture Quality and Computational Power Estimation

The PSNR between the original picture and the predicted picture obtained by the GDS algorithm is measured through a simulation. Simulation conditions are summarized as:

- Motion estimation algorithm:
  - Full search (FS)
  - 1/4 sub-sampling full search (QFS)
  - Gradient descent search (GDS)
- Sample picture:
  - Buildings along the Canal (Fig. 6)
  - Church (Fig. 7)
  - Yacht Harbor (Fig. 8)
- Resolution: 1920×1035
- Number of frames: 150
- Search range: H:−128, +127/V:−64, +63
- Forward frame prediction
- Half-pel precision.

Fig. 6 Buildings along the Canal.

Fig. 7 Church.

Fig. 8 Yacht Harbor.

Figures 9, 10 and 11 show simulation results. The average PSNR obtained by the GDS algorithm is almost the same as the FS and QFS algorithms.

The conventional FS algorithm estimates all vectors in a search range. Then, the optimal vector must be found, but the number of operations is huge. The computational power required by the FS algorithm for HDTV resolution video is

$$(16 * 16) * 2 * (256 * 128) * ((1920 * 1080) /(16 * 16)) * 30 = 4077\,\text{GOPS}.$$

The two operations to calculate mean absolute error (MAE), H:−128, +127/V:−64, +63 of the search range, 1920×1080 pixels resolution, 30 fps of the bit rate are assumed in the equation. The computational power is about 1000 GOPS even for the 1/4 sub-

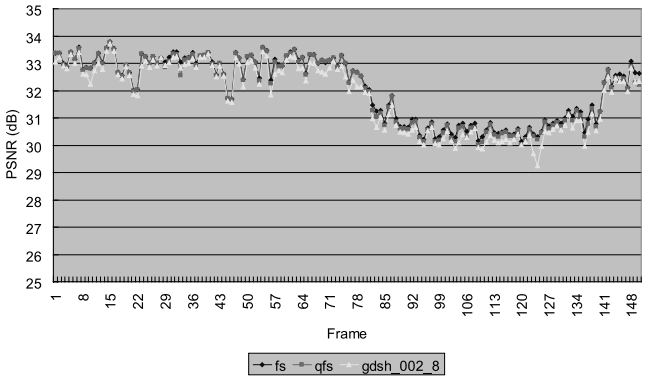

Fig. 9 Average PSNR per frame, Buildings along Canal.

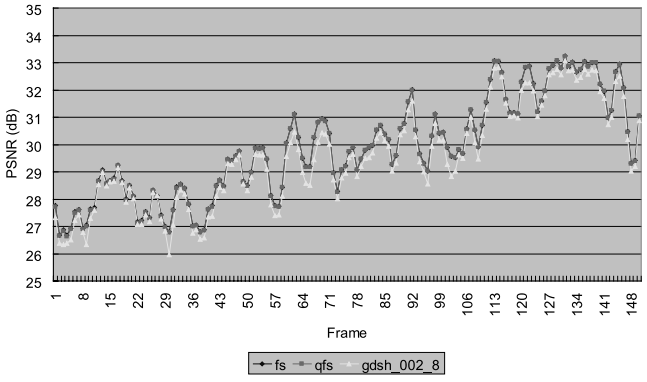

Fig. 10 Average PSNR per frame, Church.

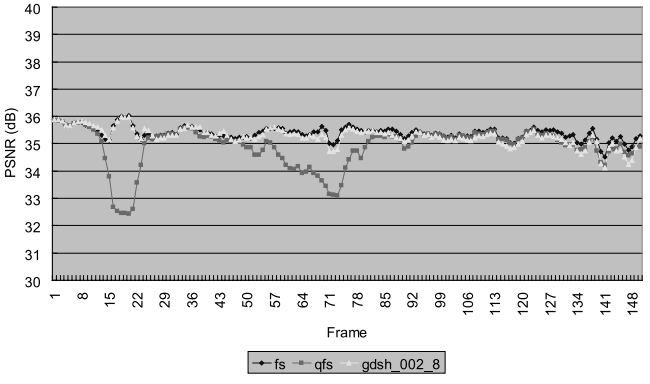

Fig. 11 Average PSNR per frame, Yacht Harbor.

sampling technique.

The computational power required by the GDS algorithm is investigated with the simulation. The number of block matchings per macroblock obtained by the simulation is 24, then the computational power can be calculated as

$$(16 * 16) * 4 * 24 * ((1920 * 1080)/(16 * 16)) * 30 = 6\,\text{GOPS}.$$

The four operations to calculate the MSE and differential coefficients for 1 pixel is assumed here. The GDS algorithm requires only 6 GOPS to process HDTV

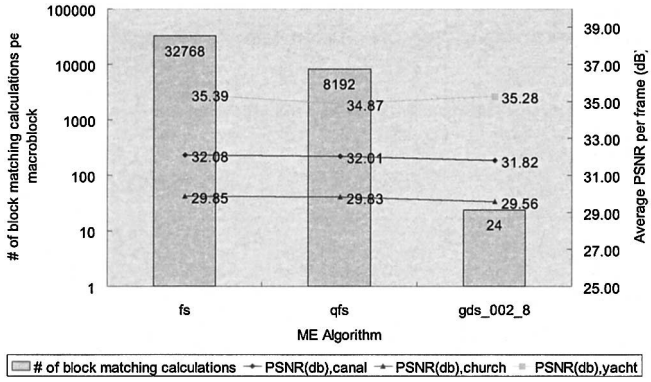

Fig. 12 Computational power and picture quality.

resolution video. The computational power and picture quality for three motion estimation techniques simulated here are summarized in Fig. 12. A drastic power reduction maintaining picture quality as the FS algorithm is obtained using the GDS algorithm.

3. Architecture

Figure 13 shows the block diagram of the ME processor. The SIMD datapath is optimized for the GDS algorithm. It contains 1 TB, 16 SWs, 32 PEs, and an adder tree. A MemoryBus feeds new image data to TB and SWs. The TB and SWs are image data caches. The TB, SWs, and PEs are connected by two CrossPaths. The PE executes a calculation for 1 pixel in a cycle. The PEs are followed by an adder tree which completes the calculation. The control part contains a MCORE, an instruction RAM (IRAM), a sequencer (SEQ), and address generators (AG). Features of this architecture are as follows:

- Concurrent data transfer
- 32 PE SIMD datapath
- Adaptive control by MCORE.

3.1 Concurrent Data Transfer

The TB and SWs receive the next MB data from MemoryBus and feed pixel data to PEs concurrently as illustrated in Fig. 14. Thus, TB and SWs keep supplying pixel data to PEs so that pipeline operation of PEs can be maintained continuously. The TB, SWs, and PEs are connected by two CrossPaths, which sort the sequence of pixel data from SWs corresponding to the sequence of pixel data from TB. The CrossPath is implemented with 1:16 demultiplexers.

The next MB data received by SWs are illustrated in Fig. 15. The SWs must receive the next MB data within 1 macroblock cycle. The bandwith to transfer the next MB data can be calculated as

$$(16 * 144) * ((1920 * 1080)/(16 * 16)) * 30$$

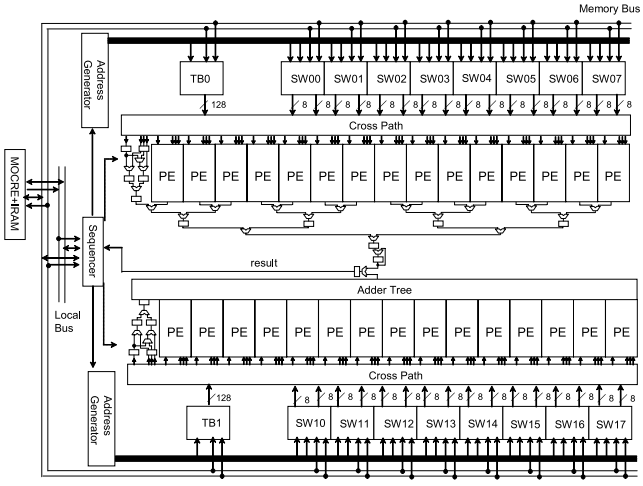

Fig. 13 ME processor block diagram.

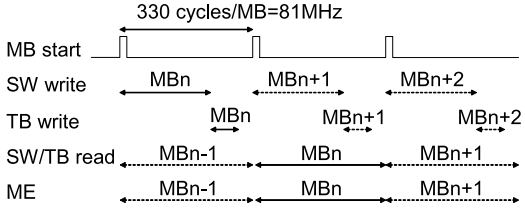

Fig. 14 ME processor timing diagram

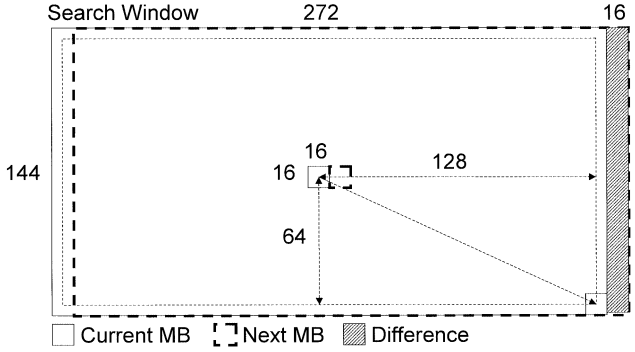

Fig. 15 Search window configuration.

$$= 559,872,000\,(\text{Bytes/s}).$$

The width of the MemoryBus is 64 bit; it operates at 81 MHz. Therefore, the bandwidth of the MemoryBus is 648,000,000 (Bytes/s), a sufficient memory bandwidth. It is assumed that the MemoryBus connects the ME processor with a frame memory dedicated to the ME. The ME processor generates addresses very regularly to read pixel data from the frame memory. Thus 86% utilization of the MemoryBus can be attained if the frame memory is composed of SDRAMs, with its pipeline feature.

3.2 32-PE SIMD Datapath

The ME chip contains 32 PEs. The PE is optimized for the GDS algorithm. A PE can execute the calculation for MSE and differential coefficients. Figure 16 shows the block diagram of the PE. Figure 16(a) depicts the PE configuration for the MSE calculation. The PE receives 1-pixel data from TB and 1-pixel data from SW. Figure 16(b) describes the PE configuration to calculate a differential coefficient in the x direction. The PE receives 1-pixel data from TB and 3-pixel data from SWs. The data from S1 terminal represents a center pixel; the other two data from S0 and S2 are left and right pixels. Figure 16(c) describes the PE configuration for a differential coefficient in the y direction. The PE receives 1-pixel data from TB, 2-pixel data from SWs and 1-pixel data from the opposite PE. The data from S3 is a center pixel; the other two data from S1 are upper and lower pixels. Delay buffers are inserted for delay adjustment for these pixel data. The PEs are followed by adders and accumulators which complete calculation of MSE or differential coefficient for the search vector.

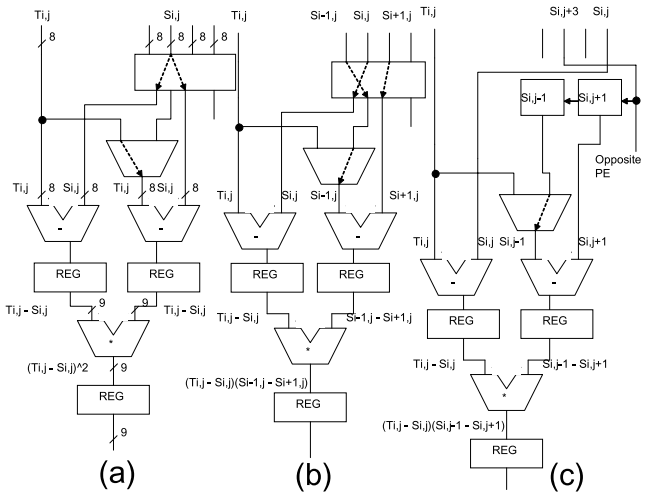

Fig. 16 PE block diagram.

A PE can perform above computation for 1 pixel in a cycle, so 32 PEs can evaluate one search vector (or 1 MB) in 8 cycles. A PE can execute 2 subtractions, 1 multiplication and 1 addition simultaneously, so that 32 PEs can execute 128 operations in a cycle. The performance of this SIMD is 10 GOPS at 81 MHz. The GDS algorithm requires 6 GOPS to execute motion estimation for the HDTV resolution video as described in Sect. 2.2; therefore this SIMD is able to execute it.

Several ME processors connected to the same MemoryBus can work concurrently to obtain a high quality picture. For example, two ME processors start searching from different initial vectors, and a better result can be taken from one of two ME processors. In this case, the way that a codec circuit performs half pel motion estimation is more efficient than that the ME processor does it. Thus the ME processor doesn't have a half pel motion estimation cirtuit.

3.3 Adaptive Control by MCORE

The control part of the ME processor consists of an MCORE, an instruction RAM (IRAM), a sequencer (SEQ), and address generators (AG). The MCORE is a RISC processor developed by Motorola for embedded systems. It executes instructions in IRAM. It sets commands and parameters in SEQ registers and can control the SIMD datapath indirectly. The command set includes "initial vector evaluation," "search vector evaluation," "differential coefficients calculation," and "1-dimensional search." The parameter set includes "the number of cycles," "the image layer number," "the size of TB," "the size of SW," "initial vectors," "search vector," "search direction," and "search step width." The SEQ supplies control signals to PEs according to the commands and parameters. It supplies a search vector and start signal to AG. The AG translates a search vector from SEQ to memory addresses and supplies them to TB and SWs.

Adaptive and efficient control of motion estimation processing is realized by a combination of MCORE and SEQ. For example, an appropriate search step width can be calculated by MCORE using MSE and differential coefficients at the start point of 1-dimensional search. The MCORE makes the control system adaptive. On the other hand, in a 1-dimensional search, if MCORE accesses SEQ registers every time the evaluation completes, the MCORE overhead is not negligible. The SEQ has been designed so as to execute a series of evaluations and stop searching when it finds a temporary solution without control by MCORE. The SEQ makes the control system efficient.

4. Circuit Design

The block diagram of the 3-port SRAM macro, which is utilized for SWs, is illustrated in Fig. 17. The macro has concurrent 3-port access capability (2R1W) and a 4 Kword by 8-bit configuration. The ME chip integrates 16 pieces of the macro for about 500 kbit storage as SWs. As a result, a low power design for the 3-port SRAM macro is essential to realize sub-100 mW ME LSI.

The 3-port SRAM macro has three major features to reduce power dissipation. A symmetric 3-port memory cell layout has been introduced to avoid influence to the cell ratio by misalignment and processing issues. This enhances cell stability, particularly under low voltage condition less than 1 V. Also, the write-disturb problem, which frequently appears in the operation of the conventional multi-port RAM, is completely eliminated by a newly developed cell-array arrangement. This is realized by a combination of full divided wordline structure [8] for the entire 3-port circuit and a wordline scheme which is connected to only one row of eight memory cells (1 pixel). The above two features enable 1 V operation, allowing low power characteristics. Moreover, the divided wordline structure drastically reduces the bitline current, which occupies a significant amount of total power consumption of the macro, to 1/8 of its previous value.

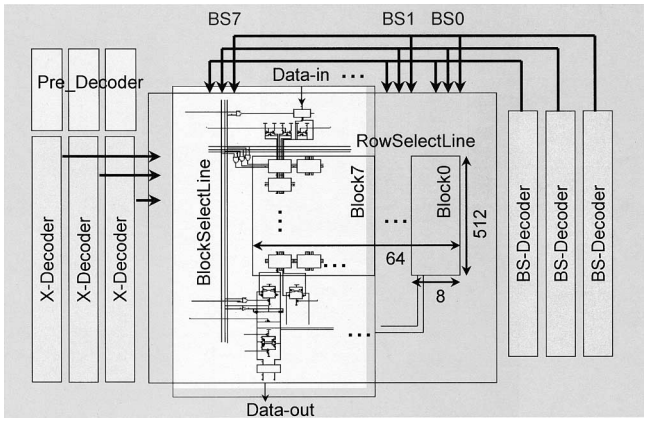

Fig. 17 3-port SRAM macro block diagram.

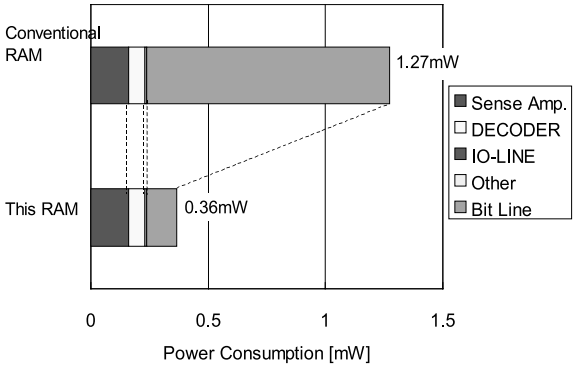

Fig. 18 3-port SRAM power consumption.

Figure 18 shows a breakdown of power consumption of the 3-port SRAM macro. The macro of 4 K × 8 bit consumes only 0.36 mW at 0.7 V and 1.32 mW at 1 V under 81 MHz operation condition. Hence, the power dissipation of total search window buffer is suppressed to 25 mW under 1 V operation, which is about one-third of that using the conventional design technique shown in Fig. 18.

5. Implementation and Performance Estimation

5.1 Delay Analysis

Figure 19 shows a simulation waveform of the 3-port SRAM obtained by HSPICE. It is verified that the SRAM operates at 100 MHz@0.7 V. It is also verified that the logic part operates at 81 MHz@0.7 V using circuit simulation and static timing analysis. Then, the ME processor can operate at 81 MHz@1.0 V certainly.

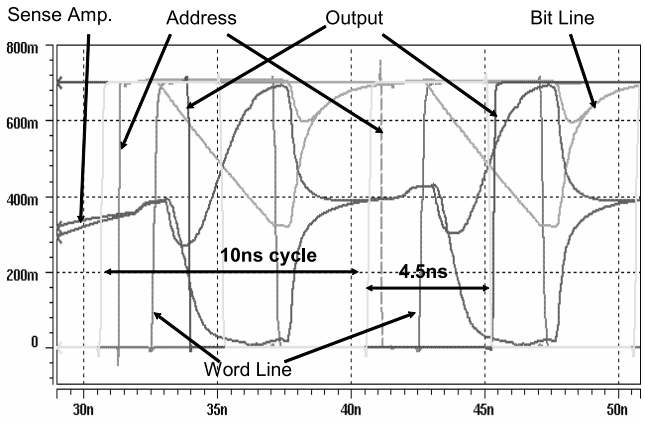

Fig. 19 3-port SRAM simulation waveform.

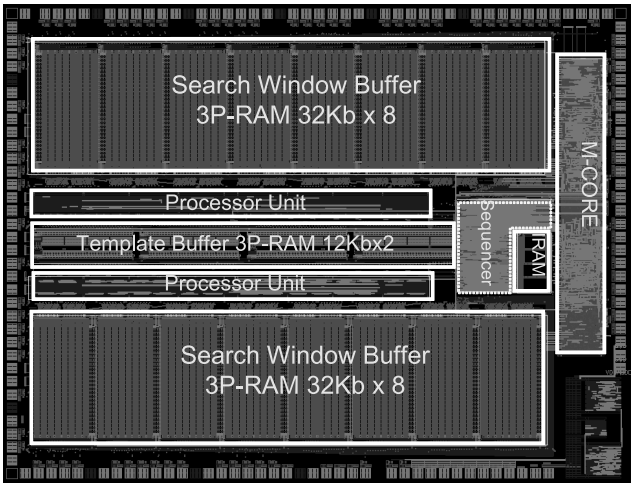

Fig. 20 ME processor plot image.

5.2 Power Consumption Analysis

Power consumption is estimated by HSPICE and PowerMill. As described in Sect. 4, power dissipation of total search window buffer is suppressed to 25 mW under 1 V operation. The estimated power consumption of the logic part and interconnection part is 20 mW and 20 mW, respectively. So, 65 mW of power consumption for the ME core under 81 MHz@1.0 V condition is attained.

5.3 Plot Image and Characteristics

The plot image of the newly developed ME processor is shown in Fig. 20. Characteristics of the processor are summarized as follows:

- Technology: 0.13 μm CMOS, 5 metal layers
- Chip Size: 4.80×3.65 mm
- Number of Transistors: about 7 million
- Function: frame structure, forward frame prediction, integer-pel precision (in realtime)
- Resolution: 1920×1080 pixels
- Frame Rate: 30 fps
- Search Range: H:-128, $+127$/V:-64, $+63$
- Clock Frequency: 81 MHz
- Power Supply: 1.0 V
- Power Consumption: 65 mW (estimated by circuit simulation).

6. Conclusion

A motion estimation processor for MPEG2 HDTV resolution video encoding is newly designed. The estimated power consumption is less than 100 mW at 81 MHz@1.0 V, which is equal to less than 10% of the power dissipation realized by 1/4 sub-sampling technique. This low power characteristic is obtained through the development of the GDS algorithm whose required computational power is about 0.1% of the FS algorithm and the VLSI architecture with little degradation of video quality. Consequently, it can be applicable to portable HDTV systems.

Acknowledgement

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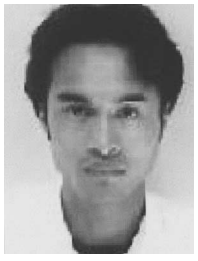

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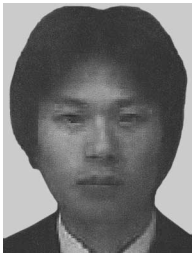

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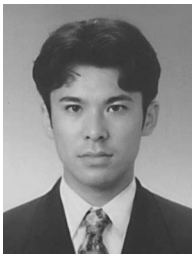

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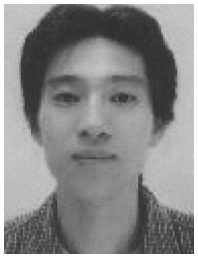

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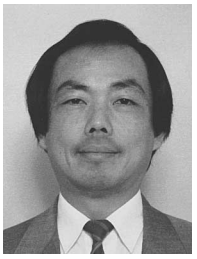

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