Low-power Hardware Implementation of Noise Tolerant Heart Rate Extractor for a Wearable Monitoring System

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***Abstract*—To prevent lifestyle diseases, wearable bio-signal monitoring systems for daily life monitoring have attracted attention. Wearable systems have strict size and weight constraints, which impose significant limitations of the battery capacity and the signal-to-noise ratio of bio-signals. The novelty of this work is the hardware implementation of a noise-tolerant heart rate extraction algorithm that can achieve low-power performance with high reliability. This report describes comparisons of the heart rate extraction algorithm performance and the dedicated hardware implementation of short-term autocorrelation (STAC) method. The proposed heart rate extractor, implemented in 65-nm CMOS process using Verilog-HDL, consumes 1.65 μA at 32.768-kHz operating frequency with 1.1 V supply voltage.**

I. Introduction

MOBILE health is expected to play an increasingly prominent role in health provision because of the advent of an aging society. Especially, daily life monitoring is important to prevent lifestyle diseases, which are expected to raise the number of patients and elderly people requiring nursing care. This report specifically describes a noise-tolerant Instantaneous Heart Rate (IHR) detection algorithm for a wearable ECG monitoring system. The IHR is useful for heart disease detection, heart rate variation analysis, and exercise intensity estimation.

Key factors affecting wearable system usability are miniaturization and weight reduction (see Fig. 1). However, strict limitations on power consumption and electrode distance of wearable ECG monitors render them sensitive to noise of various kinds. The signal-to-noise ratio (SNR) of ECG signals is especially degraded if a subject is not at rest (e.g. exercising).

In general, to prevent SNR degradation, sophisticated analog front-end circuits are necessary to prevent SNR degradation. The analog front-end of the ECG monitoring system mainly comprises amplifiers, analog filters, and an analog-to-digital converter (ADC). Unfortunately, analog circuits have large circuit area and high power consumption. Battery mass and power consumption must be reduced because battery mass dominates wearable systems.

Ultra-low-power ADCs, which have sub-μW power consumption and a limited sample rate, have been developed for biomedical applications [1]. Furthermore, according to Moore's law, the power of digital components increases with the progress of process technology. However, the power consumption of analog circuits will not decrease similarly. Therefore, as presented in Fig. 2, the features and purposes of our approach are the use of digital signal processing to reduce the performance requirements of analog components and to minimize the system's overall power consumption.

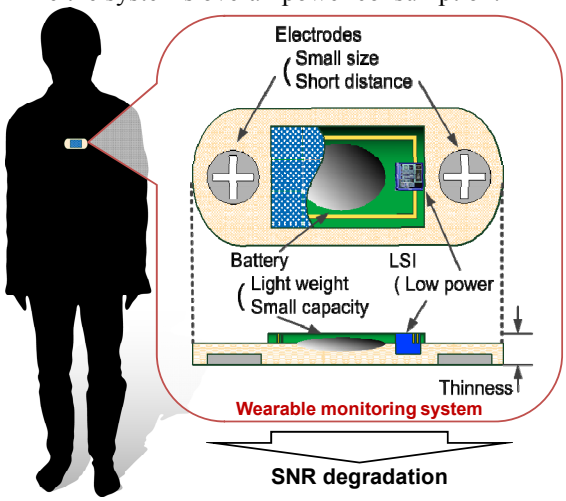

Fig. 1. Constraints of wearable monitoring system.

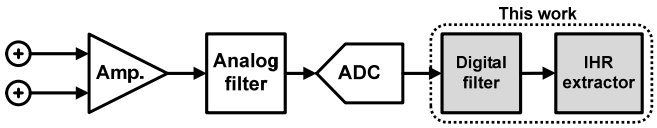

Fig. 2. Block diagram of IHR extraction.

II. Heart Rate Extraction Techniques

Recently, various algorithms have been proposed to improve the accuracy and reliability of heart rate extraction.

Extracting R-waves using threshold determination is a widely used approach for IHR detection from ECG. The Pan–Tompkins (PT) algorithm [2] is most commonly used for beat detection. This algorithm uses band-pass filtering, differentiation, squaring, and moving window integration. Periodically, the threshold is adjusted automatically using QRS morphology and the heart rate.

The SQRS [3] and WQRS [4] algorithms, which have been published in PhysioNet, can respectively detect QRS based on ECG slope and length transform. The SQRS uses band

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pass filtering for noise reduction, which uses only the integer coefficient. The WQRS also uses a low-pass filter to remove baseline wander.

The Discrete Wavelet Transform (DWT) [5–7] uses a wavelet transform with quadratic spline wavelet (QSW). The threshold is calculated using the root mean square value of the wavelet transform. This algorithm has been used in robust ECG monitoring LSIs [7–9]. The QSW requires a small amount of calculation and hardware cost because it can be implemented using only adders and shift operators.

The Quad Level Vector (QLV) algorithm [10] is implemented in dedicated hardware for ECG monitoring LSI [11, 12]. The QLV is generated using DWT and the adaptive threshold. Then, the threshold is determined by the maximum mean deviation (MD) of the previous heartbeats.

The Continuous Wavelet Transform (CWT) algorithm [13–15] employs a Mexican hat wavelet in the frequency interval of 15–18 Hz. The R-peak can be extracted using the adaptive threshold, which is calculated using the modulus maxima of the CWT. This algorithm is also implemented in [12].

Autocorrelation [16, 17] and template matching [18] use the similarity of QRS complex waveforms and have no threshold calculation process. Autocorrelation has been used in a non-invasive monitoring system. However, the method necessitates numerous computations because it calculates the average heart rate over a long duration (30 s). Our previous work proposed a short-term autocorrelation (STAC) technique for IHR detection. It combined QSW and the autocorrelation method [19].

III. Performance Comparison

To evaluate the noise tolerance of heart rate extraction algorithms, we implemented PT, SQRS, WQRS, QLV, DWT, CWT, and STAC using MATLAB.

First, we investigated the successful rate of heart rate extraction using 22 waveforms from the MIT-BIH arrhythmia database [20]. Table 1 shows that no significant difference was found among the successful rates in clean waveforms, although they include arrhythmia.

Next, we evaluated the noise tolerance using the MIT-BIH noise stress test database [21]. Figs. 3 and 4 show the relation between the intensity of noise and the success rate of IHR detection. Then, the signal-to-noise ratio (SNR) is defined as shown below.

$$SNR = 10\log\frac{S}{N \times a^2}$$

Here, S, N, and a are defined respectively as the signal power, frequency-weighted noise power, and scale factor.

As shown in Figs. 3 and 4, the CWT and STAC have better noise tolerance in each condition. Based on these results, we chose the STAC algorithm for our heart rate extractor hardware in this work.

TABLE I
Comparison of Heart Rate Extraction Success Rates

DB#	PT [2]	SQRS [3]	WQRS [4]	DWT [5]	QLV [10]	CWT [13]	STAC [19]
100	99.9	99.8	99.8	99.9	99.9	99.8	99.9
101	99.8	99.7	99.3	99.7	99.4	99.6	99.7
102	99.9	99.9	99.9	99.8	98.2	99.7	99.8
103	100.0	99.9	99.9	100.0	99.9	100.0	99.8
104	95.6	96.5	95.5	97.0	95.3	92.2	99.5
105	70.7	94.1	92.8	95.2	93.5	98.0	97.7
106	84.6	89.7	96.4	95.2	87.9	93.4	96.7
107	96.8	99.3	94.8	99.6	94.6	99.1	97.8
108	86.9	80.9	84.7	74.1	70.5	99.1	98.5
109	99.6	98.1	99.4	99.6	99.6	99.6	99.0
111	99.3	99.4	99.8	97.4	17.0	99.8	99.7
112	99.9	99.7	99.8	99.4	99.9	100.0	99.2
113	99.8	99.4	97.2	99.8	99.6	99.6	99.9
114	99.8	99.7	99.3	99.9	99.6	99.8	98.4
115	99.9	99.5	99.1	99.7	99.7	99.8	99.9
116	95.4	98.6	98.1	99.6	98.3	99.2	95.6
117	100.0	99.9	99.9	99.7	99.1	100.0	99.9
118	99.9	97.9	99.1	99.7	96.2	99.4	99.2
119	99.8	98.5	96.1	95.9	99.1	97.4	96.8
121	99.9	99.4	99.7	99.2	91.1	99.9	99.8
122	100.0	99.9	99.9	99.9	97.2	100.0	99.8
123	100.0	99.2	98.6	99.7	99.4	99.4	99.6
124	98.4	99.4	99.3	99.5	96.7	98.2	99.7
average	96.8	97.8	97.8	97.8	92.7	98.8	99.0

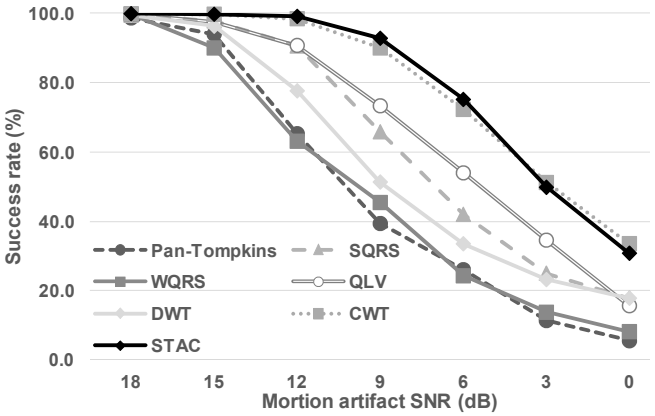

Fig. 3. Relation between SNR (MIT-BIH #100 with motion artifact) and success rate of IHR extraction.

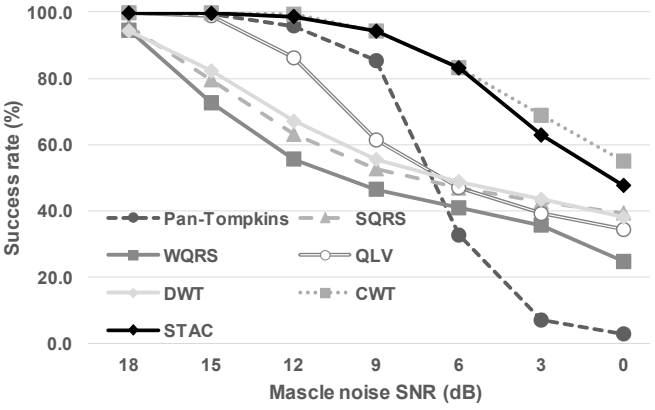

Fig. 4. Relation between SNR (MIT-BIH #100 with muscle noise) and success rate of IHR extraction.

IV. Hardware Implementation of IHR Extractor

A. Algorithm overview

In this work, we use STAC algorithm for a robust IHR extractor. Fig. 5 portrays IHR extraction using STAC. As depicted in Fig. 5 and (1–4), the IHR at time t_n (IHR_n) is obtained as the window shift length (T_{shift}) that maximizes the correlation coefficient between the template window and the search window (CC_n).

$$CC_n[T_{shift}] = w_1 \cdot \sum_{i=0}^{L_{win}-1} Q_w[t_n - i] \cdot Q_w[(t_n - T_{shift}) - i] \quad (1)$$

$$IHR_n = \arg_{\substack{T_{shift} \\ 0.25\times F_s \le T_{shift} \le 1.5\times F_s}} \max \{CC_n[T_{shift}]\} \quad (2)$$

$$L_{win} = 1.5 \times F_s \quad (3)$$

$$w_1 = \begin{cases} 1 & (T_{shift} \le 0.546 \times F_s) \\ 0.75 & (0.546 \times F_s < T_{shift} \le 0.983 \times F_s) \\ 0.5 & (0.983 \times F_s < T_{shift}) \end{cases} \quad (4)$$

In the equations presented above, F_s, L_{win}, and w_1 respectively denote the sampling rate (samples/s), the window length, and the weight coefficient. The value of T_{shift} is set as 0.25 s to 1.5 s because the heart rate of a healthy subject is 40 bpm to 240 bpm. The L_{win} is updated according to the estimated IHR to reduce the computational amount and to improve the IHR estimation accuracy. Then, the range of L_{win} and w_1 is determined by the maximum rate of the beat-to-beat variation, which is generally 20% in a healthy subject.

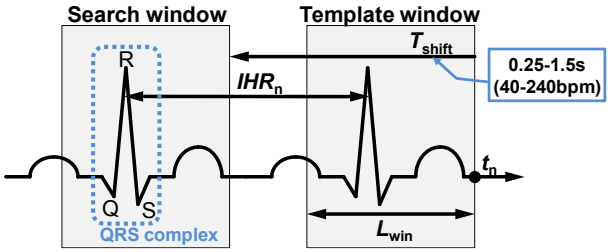

Fig. 5. IHR extraction using autocorrelation.

B. Architecture

The STAC is implemented as dedicated hardware to minimize the power overhead. Fig. 6 presents the block diagram of the IHR monitor and STAC processing core. Each STAC core has CC buffer to store the intermediate value of $CC_n[T_{shift}]$ in (1). The CC buffer is updated in synchronization with the ECG input (see Fig. 7). Because the L_{win} is 1.5 s and because IHR is updated every second, two STAC cores alternately calculate IHR with 0.5 s overlap.

Fig. 8 presents a block diagram and frequency characteristics of the QSW with 128-Hz sampling rate. The base-line wander and hum noise can be removed easily using QSW. Unfortunately, it is difficult to remove the myoelectric noise and electrode motion artifacts using QSW alone because these frequency ranges are similar to the desired ECG signal. Therefore, in the second stage, the IHR is extracted using the autocorrelation method.

To optimize the architecture of STAC hardware, we assess the influence of the resolution and sampling rate of the ECG waveform using a MATLAB model and a noise stress test. Fig. 9 depicts the relation between the ECG waveform resolution (bit width) and the successful rate of IHR extraction. As presented in Fig. 9, if the bit width is greater than eight, then the successful rate is not degraded. Fig. 10 shows the influence of the sampling rate. The accuracy of IHR is degraded rapidly if the sampling rate is lower than 64 samples/s. Consequently, eight-bit resolution and a 128 samples/s sampling rate were chosen for our system.

The dual STAC core architecture also contributes to reduction of the operating frequency. Fig. 11 shows the required operating frequency to realize the real-time STAC calculation. The sampling rate target was set as 128 samples/s for this study. Therefore, the required frequency is lower than 32 kHz when applying dual core architecture. Therefore, this STAC hardware can operate only using 32.768-kHz real-time clocks. The real-time clock, which has low power consumption, is a necessary component of a wearable monitoring system.

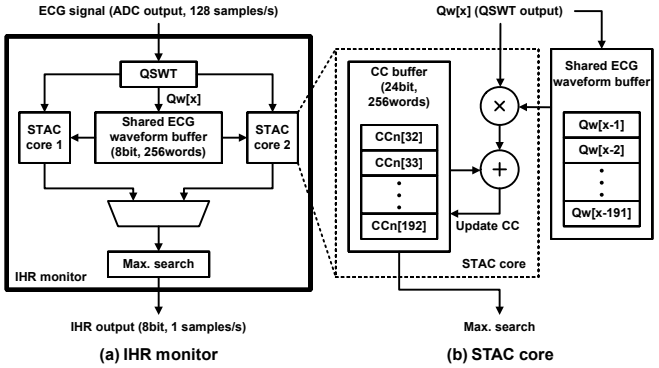

Fig. 6. Block diagram of a robust IHR extractor.

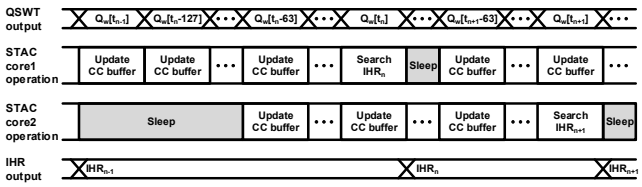

Fig. 7. Timing chart of IHR extraction.

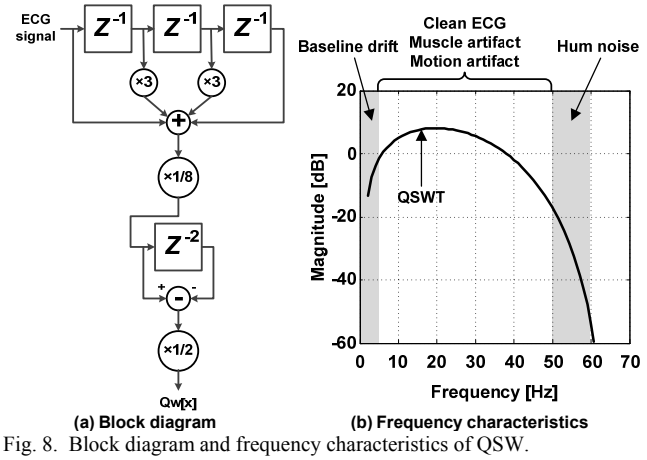

Fig. 8. Block diagram and frequency characteristics of QSW.

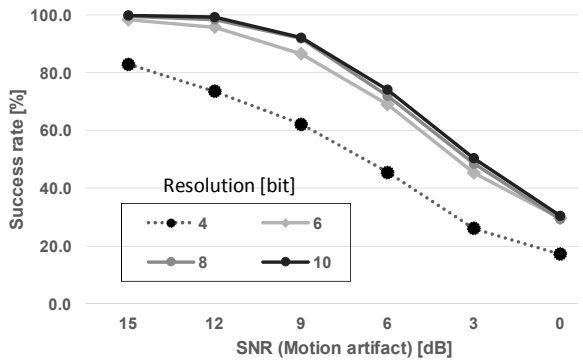

Fig. 9. Influence of ECG resolution (bit width) in IHR extraction.

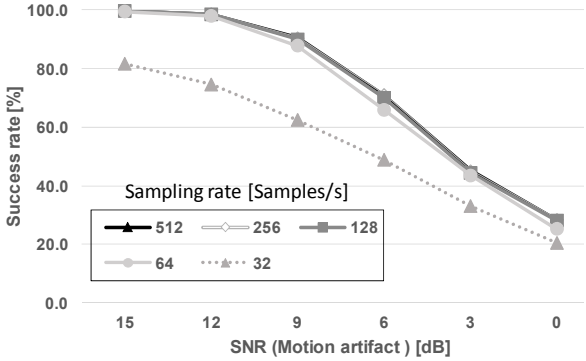

Fig. 10. Influence of ECG sampling rate in IHR extraction.

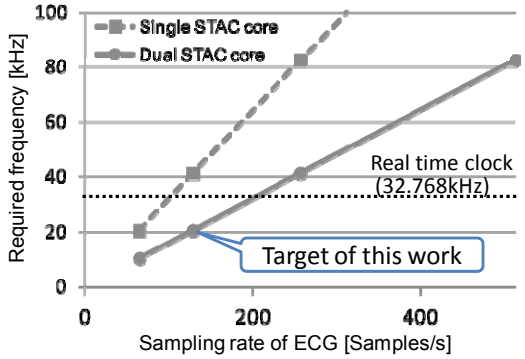

Fig. 11. Required operating frequency for real time IHR extraction.

C. VLSI implementation

We implemented the proposed IHR extractor using Verilog-HDL. Fig. 12 portrays a chip layout in a 65-nm CMOS technology. The core area is 350 × 300 μm^2. The power consumption, as estimated using a Synopsys Power Compiler, is 1.65 μW at 32.768 kHz operating frequency with 1.1 V supply voltage. The estimated result indicates that about 55% of the power is dissipated by the leakage current of the memory.

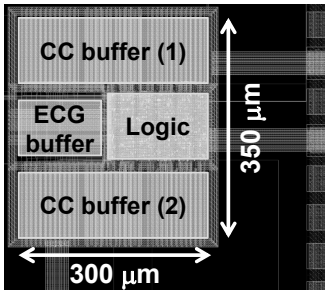

Fig. 12. Chip layout of the IHR extractor.

V. Conclusion

As described herein, we presented a low-power digital hardware design of a noise-tolerant IHR extractor. The implementation result shows that the proposed hardware has 1.65-μW power consumption and 350 × 300 μm^2 area. The leakage current is dominant in our architecture. Therefore, our future efforts will reduce the memory capacity.

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