A 6.14µA Normally-Off ECG-SoC with Noise Tolerant Heart Rate Extractor for Wearable Healthcare Systems

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Abstract— **This paper describes an electrocardiograph (ECG) monitoring SoC using a non-volatile MCU (NVMCU) and a noise tolerant instantaneous heart rate (IHR) monitor. The novelty of this work is the combination of the non-volatile MCU for normally-off computing and a noise-tolerant-QRS (heart beat) detection algorithm to achieve both low-power and noise tolerance. To minimize the stand-by current of MCU, a non-volatile flip-flop and a 6T-4C NVRAM are employed. Proposed plate-line charge-share and bit-line non-precharge techniques also contribute to mitigate the active power overhead of 6T-4C NVRAM. The proposed accurate heart beat detector employs a coarse-fine autocorrelation and a template matching technique. Accurate heart beat detection also contributes system level power reduction because the active ratio of ADC and digital block can be reduced using a heart beat prediction. Then, at least 25% active time can be reduced. Measurement results show the fully integrated ECG-SoC consumes 6.14µA including 1.28-µA non-volatile MCU and 0.7-µA heart rate extractor.**

Keywords— biomedical signal processing; electrocardiography; heart rate extraction; mobile healthcare; wearable sensors

I. INTRODUCTION

Mobile health is expected to play an increasingly prominent role in health provision because of the advent of an aging society. Daily life monitoring is especially important to prevent lifestyle diseases, which raise the number of patients and elderly people who need nursing care. Key factors affecting wearable system usability are miniaturization and weight reduction. Battery weight is a dominant characteristic of a wearable system. Therefore, the battery capacity and power consumption must be limited to the greatest degree possible. This report specifically describes an electrocardiograph (ECG) monitoring SoC for use in a wearable healthcare system. The proposed SoC has normally-off computing using nonvolatile memory and a dedicated Instantaneous Heart Rate (IHR) extractor. The IHR is an important bio-signal used for heart disease detection, heart rate variation analysis, and exercise intensity estimation.

II. NORMALLY-OFF ECG-SOC ARCHITECTURE

The proposed ECG-SoC consists of an ECG sensing block, NVMCU, and extra interfaces (see Fig. 1). The ECG sensing block has an analog front end (AFE), an 8-bit SAR ADC, and a robust IHR extractor. The NVMCU (see Fig. 2) includes a Cortex M0 (CM0) core with ferroelectric-based nonvolatile FFs (NVFF) [1], a 16Kbyte 6T-4C NVRAM for instruction and data memory, and peripherals. Because the frequency range of vital signals is low, both the standby power reduction and sleep time maximization is important to system level
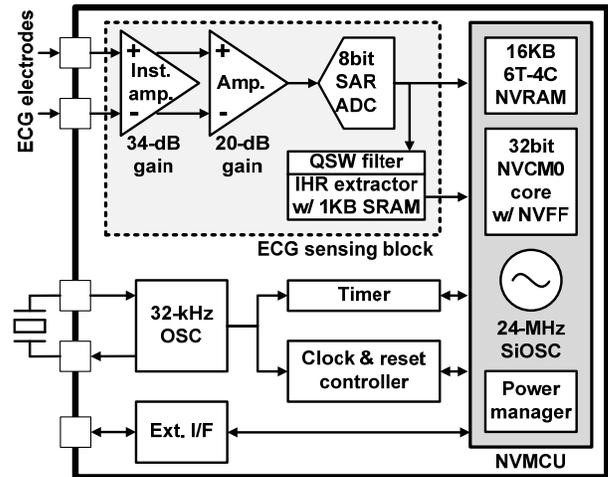
Fig. 1.   Block diagram of normally-off ECG-SoC.
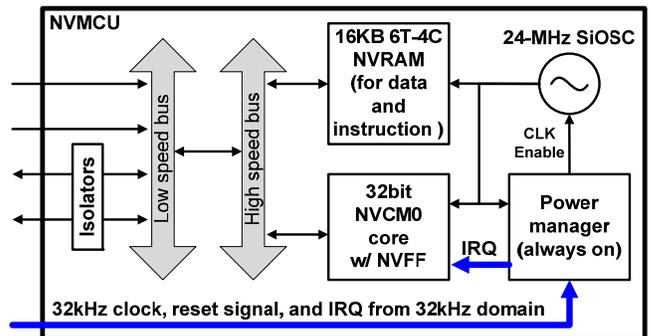
Fig. 2.   Block diagram of nonvolatile MCU (NVMCU).
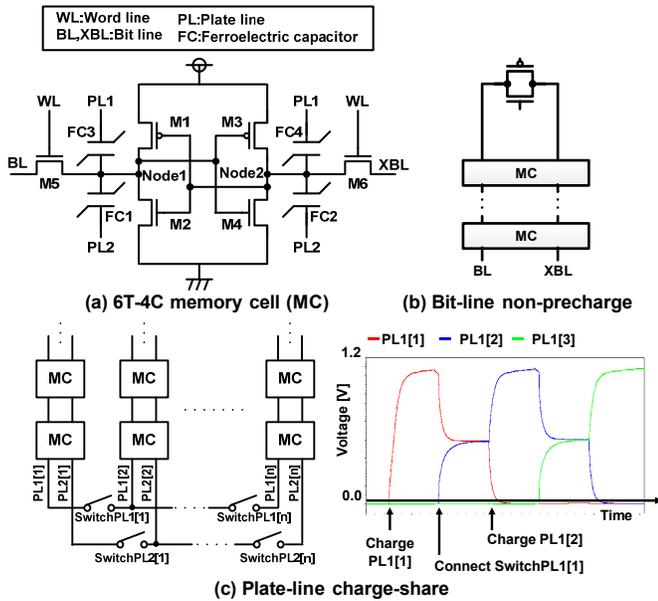
Fig. 3. Proposed NVRAM with (a) 6T-4C memory cell, (b) bit-line non-precharge technique, and (c) plate-line charge-share technique.
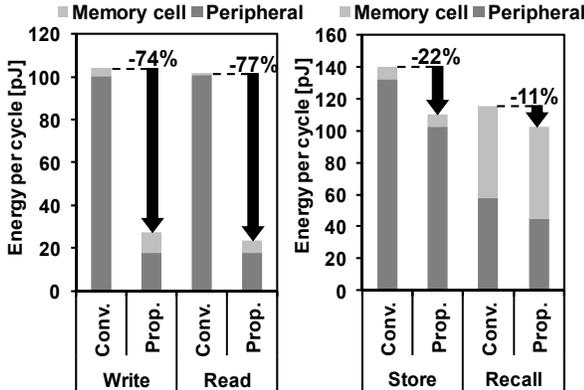
Fig. 4. .Measured energy consumption of conventional and proposed 6T-4C NVRAM.

power reduction.

We employed a 6T-4C memory cell (see Fig. 3 (a)) for the NVRAM because it has the advantage of non-volatility and fast access time [2]. However, active power dissipation is caused by the large ferroelectric capacitor, which is connected directly to plate-lines and internal nodes. This work presents plate-line charge-share and bit-line non-precharge techniques to reduce the power overhead (see Fig. 3). Additional switches between plate-lines are used to share the charge used for store and recall operations. The charge is transported sequentially from a plate-line to the next one. Furthermore, the 6T-4C cell is tolerant to the half-select problem because the ferroelectric capacitors are connected to the internal nodes. Therefore, the bit-line precharge can be omitted and only equalizing is used in this design. As shown in Fig. 4, energy consumptions of NVRAM in store, recall, write, and read operations are reduced respectively by 22%, 11%, 74%, and 77% compared with original 6T-4C memory.
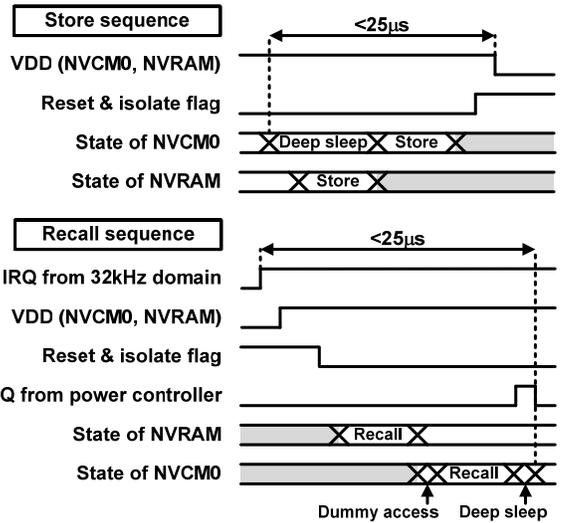
Fig. 5. Timing diagram of store/recall sequence in NVMCU.
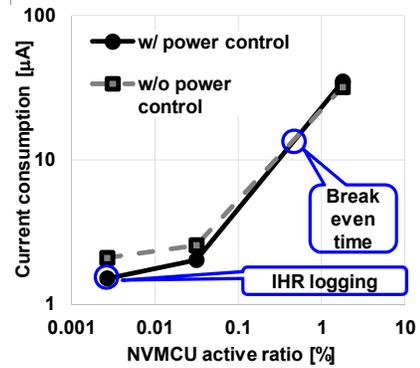
Fig. 6. Measured current consumption of NVMCU.

Fig. 5 shows the shut-down and wake-up sequence of NVMCU. The operating frequency of the NVMCU is 24 MHz, whereas the operating frequency of other digital blocks is 32 kHz. Slow signals in the 32 kHz domain are synchronized at the low-speed bus to the 24 MHz domain. Standby current of the entire 24 MHz domain including an on-chip 24-MHz oscillator can be cut when the state of CM0 core transits to deep sleep. Then the data in the NVRAM and register values of CM0 core in the NVFF are stored sequentially to ferroelectric capacitors. The data and register values of NVMCU will be recalled if the interrupt occurs from the 32 kHz domain. The store and recall operation dissipate up to 25μs overhead. As shown in Fig. 6, the energy break-even time using the normally-off function is about 0.5% active ratio.

III. NOISE TOLERANT HEART RATE EXTRACTOR

The ECG signal in wearable systems is sensitive to various noises because the electrode distance, size and the battery capacity are strictly limited. The SNR will be especially degraded if a user is not at rest. The purpose of our approach is digital signal processing to mitigate the performance requirements for the analog portion and to minimize the overall system power consumption. We implemented a quadratic spline wavelet (QSW) filter and a two-stage IHR extractor. The QSW is commonly used as the low-power noise reduction
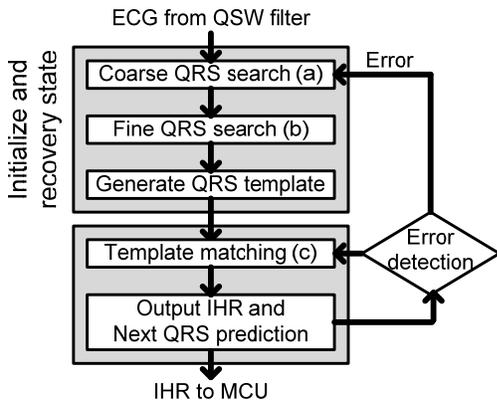
Fig. 7. Flow chart of IHR extractor.
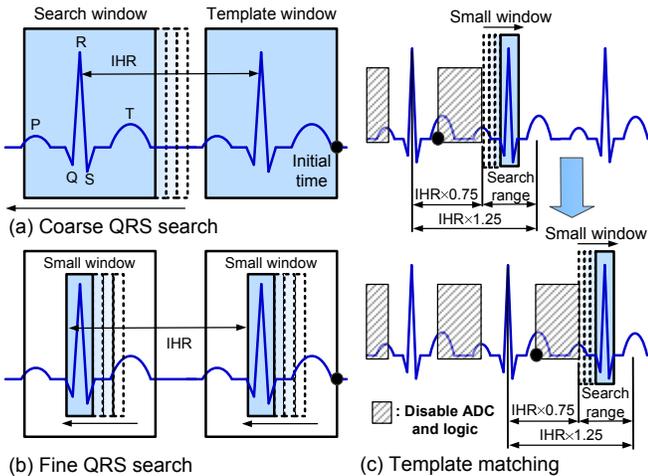
Fig. 8. Algorithm overview of coarse-fine QRS template generation and template matching with QRS prediction.

Record	Se [%]	+P [%]
100	99.9	100.0
101	99.7	99.8
102	99.9	100.0
103	99.7	100.0
104	94.4	97.7
105	98.9	97.5
106	95.6	98.6
107	97.7	100.0
108	91.7	90.2
109	99.5	100.0
111	99.9	99.9
112	99.9	100.0
113	99.9	100.0
114	99.6	99.8
115	99.9	100.0
116	99.0	99.6
117	99.9	100.0
118	99.8	100.0
119	99.5	99.8
121	99.7	99.9
122	99.8	100.0
123	99.7	100.0
124	98.0	99.1
avg.	98.8	99.2

(a) Noise stress test **(b) w/o noise**

Fig. 9. Success rate evaluation of IHR extractor using MIT-BIH arrhythmia and noise database; (a) noise stress test using motion and muscle artifact, and (b) sensitivity (Se) and positive predictivity (+P) of proposed method without noise. The definition of Se is TP / (TP + FN). The definition of the +P is TP / (TP + FP). Then, TP, FN, and FP respectively denote the number of correct QRS complex detection, the number of failures to detect the true QRS complex, and the number of false detection.

method for ECG [3]. The hum-noise and baseline wander are well suppressed using QSW. However, it is difficult to remove these noises only using QSW because it has similar frequency range of the QRS complex.

Figs. 7 and 8 show the algorithm of the IHR extractor. In the first stage, the template data of QRS complex are generated autonomously using the extended version of a coarse-fine short-term autocorrelation (STAC) [4]. Next, template matching is conducted to extract QRS complexes. Whenever the QRS complex is extracted, the IHR and the QRS template are updated by adding the detected QRS complex to the previous template. Then, the time at which the next QRS complex occurs is predicted from the beat-to-beat variation. The prediction result is used to maximize the sleep time of the ADC and IHR extractor. Even if misdetection or false detection occurs because of arrhythmia or intense noise, the IHR extractor can be awake and recover the error because the coefficient of autocorrelation will decrease rapidly when such an error occurs.

The IHR extractor can also suppress muscle artifacts and motion artifact as shown in Fig. 9. In this simulation, the simple implementation of QSW [5], Quad Level Vector (QLV) [6], Continuous Wavelet Transform (CWT) [6], and our

previous STAC [4] are modeled using MATLAB. The simulation result shows the proposed method has state-of-the-art noise tolerance.

IV. IMPLEMENTATION RESULTS

The 3.7×4.3 mm^2 test chip is fabricated using 0.13μm CMOS technology. Fig. 10 shows the chip micrograph and performance summary. The operating voltage is 1.2V for AFE, ADC, 24MHz oscillator, IHR extractor, NVMCU, and other digital blocks. Only the 32kHz oscillator and IO circuits are operated with 3.0V supply voltage.

To demonstrate the test chip performance, we implemented a heart rate logging application. Fig. 11 shows the measurement result of IHR extraction waveforms. Then, the sampling rate of ADC is set to 128Hz and the IHR output is stored to data memory every second. The measurement results show that the IHRs are extracted correctly, even in a noisy condition.

Fig. 12 (a) shows the summary of current consumptions in each block with IHR logging application. The total current consumption is 6.14 μA on average including 1.28-μA non-volatile MCU and 0.7-μA heart rate extractor. As shown in Fig. 12 (b), the proposed heart rate extractor has higher noise tolerance and minimum power overhead compared with previous noise tolerant hardware [4-6].

Table 1 presents a comparison with other recently published ECG monitoring SoCs [5, 7–10]. The proposed SoC
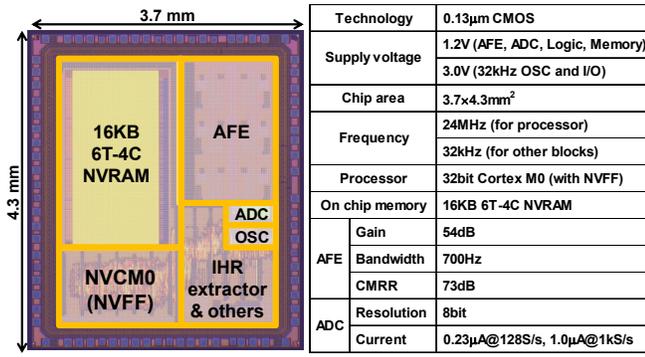
Fig. 10. Chip micrograph and chip specifications.

Technology	0.13μm CMOS	
Supply voltage	1.2V (AFE, ADC, Logic, Memory)	
	3.0V (32kHz OSC and I/O)	
Chip area	3.7×4.3mm²	
Frequency	24MHz (for processor)	
	32kHz (for other blocks)	
Processor	32bit Cortex M0 (with NVFF)	
On chip memory	16KB 6T-4C NVRAM	
AFE	Gain	54dB
	Bandwidth	700Hz
	CMRR	73dB
ADC	Resolution	8bit
	Current	0.23μA@128S/s, 1.0μA@1kS/s
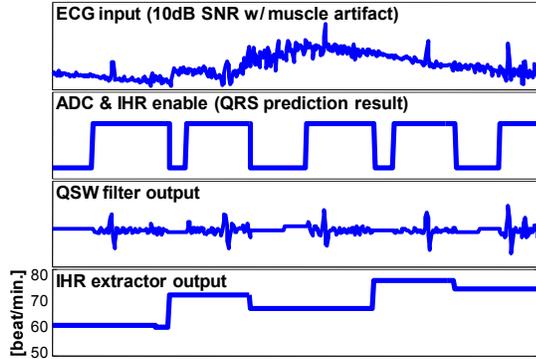
Fig. 11. Input ECG waveform and measurement results of QRS prediction, filter output and extracted IHR.

has the minimum power consumption in fully integrated (with AFE, ADC, Digital filter, Non-volatile MCU, OSC, and communication I/F) ECG sensors.

V. CONCLUSION

We proposed the ECG-SoC using the noise tolerant IHR monitor and NVMCU in 0.13μm CMOS. The IHR monitor uses the short-term autocorrelation and template matching algorithm for noisy conditions in wearable systems. The NVMCU consists of 16Kbyte 6T-4C NVRAM and Cortex M0 core with ferroelectric based nonvolatile FFs. The 3.7×4.3 mm² ASIC consumes 6.14μA for the IHR extraction and logging application. The proposed IHR extractor achieves state-of-the-art noise tolerance and power consumption. This result mitigates the performance requirement for analog front end and electrodes. Although other similar works do not consider the noise contamination in wearable and mobile environments, the proposed chip is evaluated in field test under noisy conditions with 5-cm electrode distance and healthy (but not at rest) subject. The wearable system using the proposed 6.14μA SoC can realize one-week continuous sensing only using a 1-mAh thin-type lithium-ion battery.

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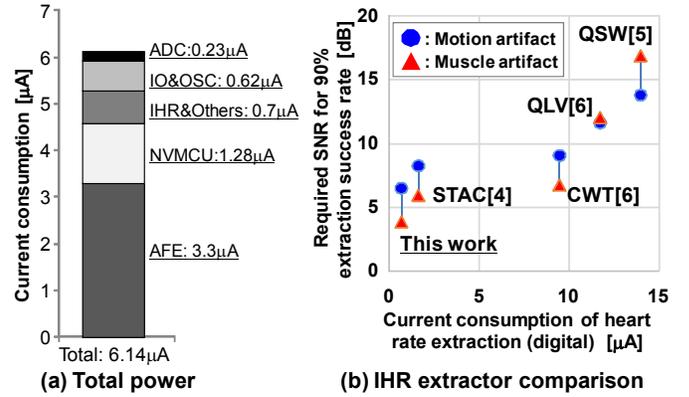
Fig. 12. Summary of current consumption; (a) total power consumption and (b) comparison of heart rate extractor performance with previous studies.

TABLE I.   PERFORMANCE COMPARISON WITH PREVIOUS STUDIES

	This work	A-SSCC'13 [7]	ESSCIRC'13 [8]	VLSI'13 [5]	ISSCC'13 [9]	ISSCC'12 [10]
Technology	0.13μm	0.35μm	0.13μm	0.13μm	0.18μm	0.13μm
Supply voltage	1.2V/3.0V	2.4-3.0V	1.2V/3.0V	0.5-1.0V	1.8/3.2V	0.3-0.7V
Frequency	32.768kHz, 24MHz	32.768kHz	32.768kHz, 24MHz	8-32kHz, 24/40MHz	20kHz	1.7MHz-2kHz
MCU	32b NVCM0	n/a	32b CM0	32b Andes N9	n/a	8b RISC
On-chip memory	16kB NVRAM	n/a	129.75kB	20.5kB	n/a	5.5kB
Total power for 1-ch IHR logging	8.47μW	9.6-12μW	18.24μW	16.1μW	18.7μW	19μW
Total current for 1-ch IHR logging	6.14μA	4.0μA	13.7μA	>16.1μA	10.41μA	>27μA

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