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Design Choice in 45-nm Dual-Port SRAM — 8T, 10T Single End, and 10T Differential

Hiroki Noguchi,[†1] Yusuke Iguchi,[†1]
Hidehiro Fujiwara,[†1] Shunsuke Okumura,[†1]
Koji Nii,[†2] Hiroshi Kawaguchi[†1]
and Masahiko Yoshimoto[†1,†3]

As process technology is scaled down, a large-capacity SRAM will be used. Its power must be lowered. The Vth variation of the deep-submicron process affects the SRAM operation and its power. This paper compares the macro area, readout power, and operating frequency among dual-port SRAMs: an 8T SRAM, 10T single-end SRAM, and 10T differential SRAM considering the multi-media applications. The 8T SRAM has the lowest transistor count, and is the most area efficient. However, the readout power becomes large and the access time increases because of peripheral circuits. The 10T single-end SRAM, in which a dedicated inverter and transmission gate are appended as a single-end read port, can reduce the readout power by 74%. The operating frequency is improved by 195%, over the 8T SRAM. However, the 10T differential SRAM can operate fastest (256% faster than the 8T SRAM) because its small differential voltage of 50 mV achieves high-speed operation. In terms of the power efficiency, however, the readout current is affected by the Vth variation and the timing of sense cannot be optimized singularly among all memory cells in a 45-nm technology. The readout power remains 34% lower than that of the 8T SRAM (33% higher than the 10T single-end SRAM); even its operating voltage is the lowest of the three. The 10T single-end SRAM always consumes less readout power than the 8T or 10T differential SRAM.

1. Introduction

As the ITRS Roadmap predicts, memory area is becoming larger. It is expected to occupy 90% of a system on a chip by 2013 [1]. For example, an H.264 encoder for a high-definition television requires at least a 500-kb memory as a search-window buffer, which consumes 40% of its total power [2]. As multi-media applications have become more complex and memory-demanding, large-capacity SRAMs will be adopted as frame buffers and/or restructured-image memory on a video chip. The large-capacity SRAM potentially dissipates a larger share of its total power, and dominates the circuit speed. Therefore, low-power and high-speed dual-port SRAM is strongly required for video processing. In particular, the power and operating frequency in a read operation is crucial because the readout takes place more frequently than write-in in a video codec. For instance in motion estimation, once picture data are written in memory, full-search algorithms or other motion compensation algorithms read out the data many times.

As process technology is scaled down, the Vth variation of MOS transistors is increased (presented in **Fig. 1**) [1] because the channel area ($L_{\rm eff} \times W_{\rm eff}$) is shrunk as manufacturing processes advance. The readout current on the read bitline (RBL) is easily affected by the Vth variation. **Figure 2** shows the readout operation waveforms of the single-end SRAM of 90-nm and 45-nm technologies. The SS corner, denotes slow nMOS and slow pMOS, is one of the process corners, which represent the extremes of fabrication-parameter variations within which a circuit that has been etched onto the wafer must function correctly. Designers examine the expected process range by using "worst case" analysis to verify that circuits will operate correctly under the Vth variation. The classic worst

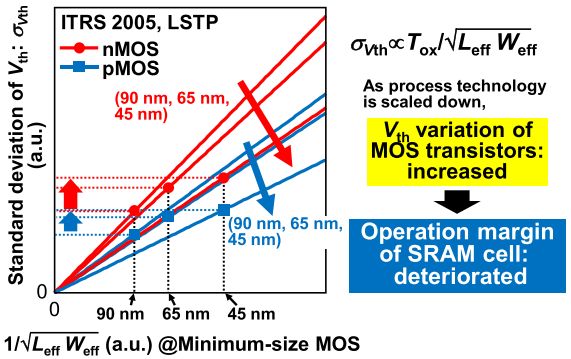

Fig. 1 Pelgrom plots in different processes. The standard deviation of Vth becomes larger as process technology is scaled down.

†1 Graduate School of Engineering, Kobe University
†2 Renesas Electronics Corporation
†3 JST, CREST

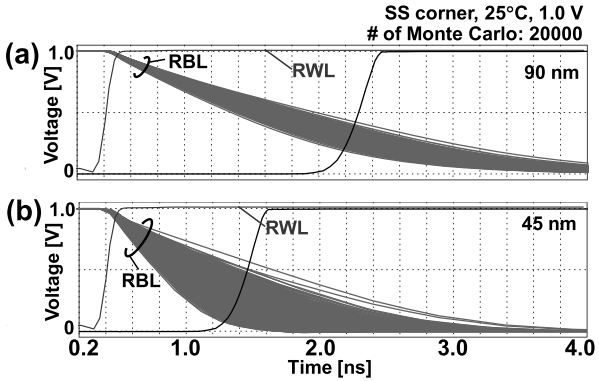

Fig. 2 RBL operation waveforms of (a) 90-nm and (b) 45-nm technologies at the SS corner (temperature = 25°C).

case situation is the asymmetrical assignment of the Vth variation to nMOS and pMOS, which worsens the charge speed or discharge speed. However such worst case involves impossible situation in terms of probability. Monte Carlo simulation with a statistical die average model gives much more realistic results of how the circuits and especially how a SRAM will operate over the expected die average process variations. In the deep submicron era, it is important to design the SRAM read-port while remaining cognizant of the Vth variation tolerance [3]. The Monte Carlo simulation reveals the readout timing variation and sense timing difficulties. To try to be more accurate modeling of how the circuits will operate, not only the Vth variation but also other device deviations, such as the channel length or a serious problem of a gate-induced drain leakage (GIDL), need to be considered. In this paper, we assume that the Vth variation includes every device deviation and it distributes with Gaussian profile.

This paper describes a comparison of dual-port SRAMs of three kinds in a 45-nm process technology. A dual-port SRAM is very useful for video processing because read and write accesses are possible simultaneously. The dual-port SRAMs are of three kinds, we handle the 8T SRAM, 10T SRAM with a single-end read port, and 10T SRAM with differential read ports.

The remainder of this paper is organized as follows. The next section compares

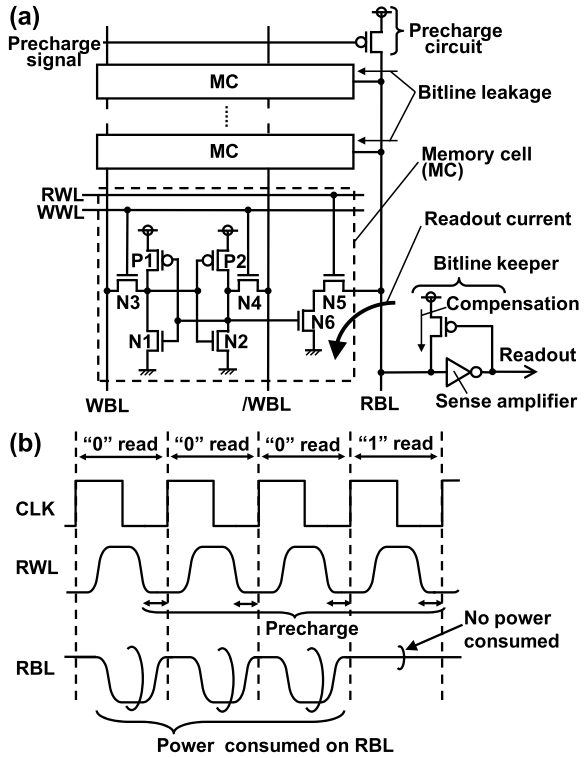

Fig. 3 8T dual-port SRAM: (a) a schematic and (b) waveforms in read operation.

their cell topologies in a 45-nm process technology. In Section 3, simulation results including their areas, operation voltages, and powers will be described. Section 4 summarizes this paper.

2. Cell Topologies

2.1 8T SRAM

The dual-port SRAM cell, which includes eight transistors (8T SRAM) [4], is depicted in **Fig. 3** (a). The 8T SRAM is a read-static-noise-margin-free SRAM in a read operation because it has a separate read port. Meanwhile, a certain power is dissipated by precharging (see Fig. 3 (b)). And the readout time becomes larger as

the supply voltage (VDD) decreases because of the bitline keeper on the RBL [5].

In the 8T SRAM, an inverter circuit is used as a sense amplifier connecting to an RBL. When a datum "1" is read out, the sense amplifier inverter need not pay a delay overhead. In contrast, when a datum "0" is read out, the sense amplifier inverter takes a certain access time by discharging the readout node. The access time in the read operation is therefore determined by the "0" readout. In other words, the logical threshold voltage of the sense amplifier inverter should be adjusted higher to minimize the discharge time.

2.2 10T Single-End SRAM (10T-S SRAM)

To improve the 8T SRAM, we have proposed a 10T non-precharge SRAM with a single-end read bitline [6)–8)], as depicted in **Fig. 4** (a) (hereinafter, "10T-S SRAM"). Two pMOS transistors are appended to the 8T SRAM cell. The additional signal (/RWL) is an inversion signal of a read wordline (RWL); it controls the additional pMOS transistor (P4) at the transmission gate. While the RWL and /RWL are asserted, a stored node is connected to an RBL through the inverter.

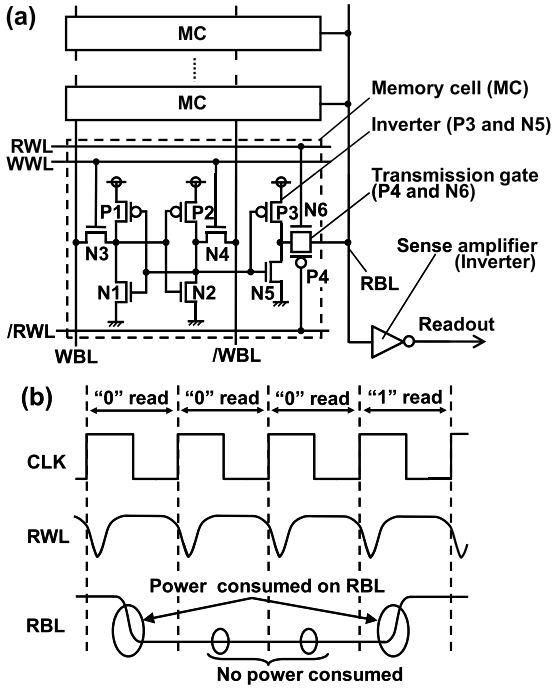

Fig. 4 10T SRAM with a single-end read bitline (10T-S SRAM): (a) a schematic and (b) waveforms in read operation.

Figure 4 (b) depicts operation waveforms in the 10T-S SRAM in read cycles. A charge–discharge power on the RBL is consumed only when the RBL is changed. Consequently, no power is dissipated on the RBL if an upcoming datum is the same as the previous state. The 10T-S SRAM is suitable for a real-time video image that has statistical similarity [6)–8)].

In the 10T-S SRAM, an inverter is connected to an RBL as a sense amplifier, just as with the 8T SRAM. The logical threshold voltage of the sense amplifier inverter should be adjusted in the middle, considering charge–discharge on an RBL and maintaining their balance. **Figure 5** shows the charging–discharging times on the RBL in the 10T-S SRAM when the drive transistor (nMOS) width in the sense amplifier inverter is changed. In the figure, the load transistor (pMOS) width in the sense amplifier is set to the minimum size—0.1 μm for the middle logical threshold voltage—because in the 10T-S SRAM, the drive power of the nMOS transistor N5 (see Fig. 4 (a)) is stronger than that of the pMOS transistor

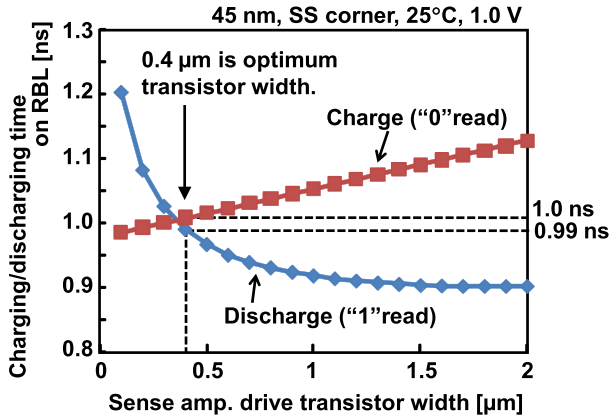

Fig. 5 Charging–discharging times on an RBL in a 10T-S SRAM when a sense amplifier drive transistor width is changed at the SS corner (temperature = 25°C).

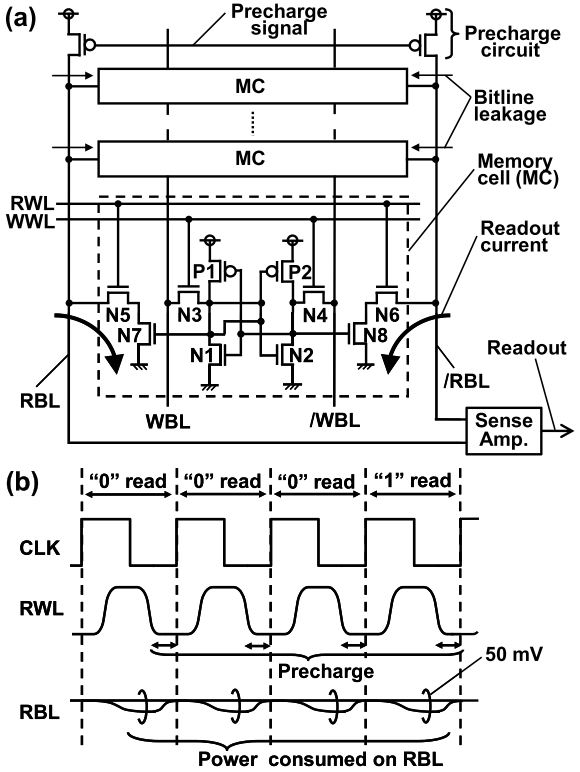

Fig. 6 10T SRAM with differential read bitlines (10T-D SRAM): (a) a schematic and (b) waveforms in read operation.

P3 (see Fig. 4 (a)) when the transistor sizes are the same. Therefore, the charging time is longer than the discharging one on the RBL. When the drive transistor width in the sense amplifier inverter is 0.4 μm, the propagation delay of the sense amplifier inverter becomes the shortest. Thus, Fig. 5 indicates that the optimum ratio of the transistor widths between nMOS and pMOS in the sense amplifier inverter is four. In this paper, we utilized 0.4-μm nMOS and 0.1-μm pMOS for the sense amplifier inverter of 10T-S SRAM. For large-capacity SRAM, in terms of reducing the Vth variation, the minimum size transistor should be avoided to employ as a sense amplifier, because the deterioration on a sense amplifier has influence on access time for all memory cells connected to it.

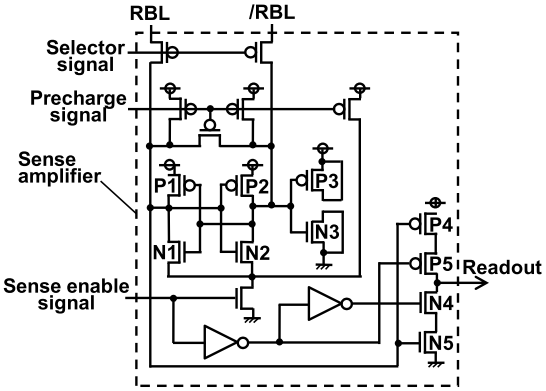

Fig. 7 Circuit schematic of a sense amplifier in the 10T-D SRAM.

2.3 10T Differential SRAM (10T-D SRAM)

Figure 6 (a) presents a schematic of a 10T SRAM with differential read bitlines (RBL and /RBL) [9]. Two nMOS transistors (N5 and N7) for the RBL and the other additional nMOS transistors (N6 and N8) for /RBL are appended to the traditional 6T SRAM. As is true also for the 8T SRAM, precharge circuits must be implemented on the RBL and /RBL.

Figure 6 (b) depicts operation waveforms in the 10T-D SRAM in read cycles. The differential bitlines must be precharged to VDD by the start time of a clock cycle. To sense a difference voltage between the RBL and /RBL correctly, the difference voltage must be, at least, more than 50 mV [10)–12)].

Figure 7 presents an illustration of a sense amplifier circuit for the 10T-D SRAM. This is a commonly used latch type sense amplifier. The use of low-threshold-voltage transistors (P3-P5 and N3-N5) enables sensing of the differential voltage faster, although the precise control of the sense enable signal is needed [13], because timing generator circuits are easily affected by the Vth variation. Consequently, the differential voltage when the sense enabled signal is enabled is varied, which varies the readout power as well.

3. Simulation Results

3.1 Cell and Macro Layouts

Figure 8 portrays the layouts of the dual-port SRAMs of three kinds in a 45-nm process technology. Schematics are shown in the previous figures. The areas of the 8T, 10T-S, and 10T-D SRAM cells are, respectively, $1.55 \times 0.41\,\mu m^2$, $1.97 \times 0.41\,\mu m^2$, and $1.95 \times 0.41\,\mu m^2$. In 8T and 10T-D SRAMs, we utilize 0.2-μm nMOS drive transistors in read port, because the drive current of 0.2-μm nMOS is larger than that of 0.1-μm nMOS. Furthermore, for these additional read ports, poly-space rule restricts the memory cell width whether we utilize 0.2-μm nMOS or not.

In Fig. 8, our memory cell design is based on a logic-design rule. When considering an SRAM-design rule, we can employ a shared contact to an inverter couple and this saves the height of the memory cell, which leads to shorter RBL and faster read operation. The effects by adopting the SRAM-design rule are absolutely same for three kinds of cells and the tendency of performance comparison is not varying whether with the logic-design rule or with the SRAM-design rule.

We also designed 64-kb SRAM macros in the 45-nm process technology for macro-level area comparison. **Figure 9** shows the macro layouts. The core sizes of the 8T, 10T-S, and 10T-D SRAM macros are, respectively, $260 \times 443\,\mu m^2$, $255 \times 550\,\mu m^2$, and $261 \times 547\,\mu m^2$. Each macro is 64 kb (128 b × 512 b). The 8T and 10T-S SRAM macros have 16 memory cell blocks (64 b × 64 b), and the divided factor between local RBL and global RBL is eight, which has been optimized by using Elmore delay model [8]. The 10T-D SRAM macro has four memory cell blocks (64 b × 256 b) and the divided factor between local RBL and global RBL is two. The 8T SRAM macro is the most area-efficient because of its lowest transistor count. The 10T-D SRAM macro has, compared to the 10T-S SRAM, a 2% area overhead that is attributable to differential sense amplifiers and precharge circuits.

3.2 Operating Frequency versus Supply Voltage

To obtain an operating frequency, we conducted Monte Carlo simulations considering threshold voltage variation of each transistor. The number of Monte

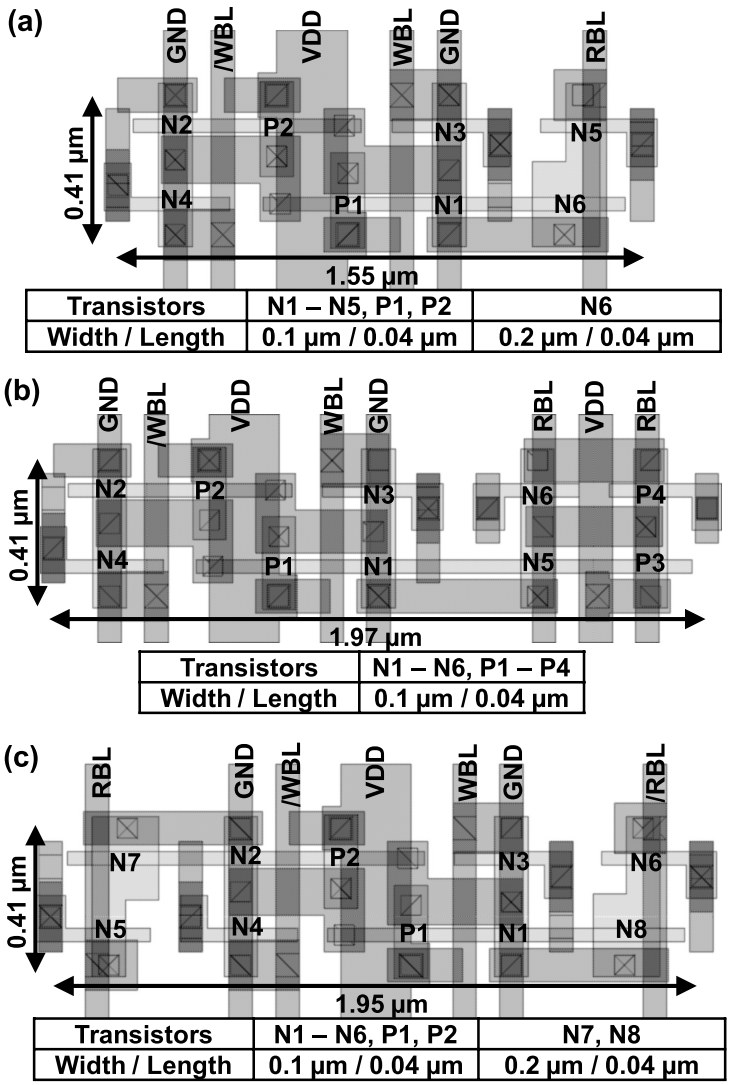

Fig. 8 Cell layouts of (a) 8T, (b) 10T-S, and (c) 10T-D SRAMs, in a 45-nm process technology.

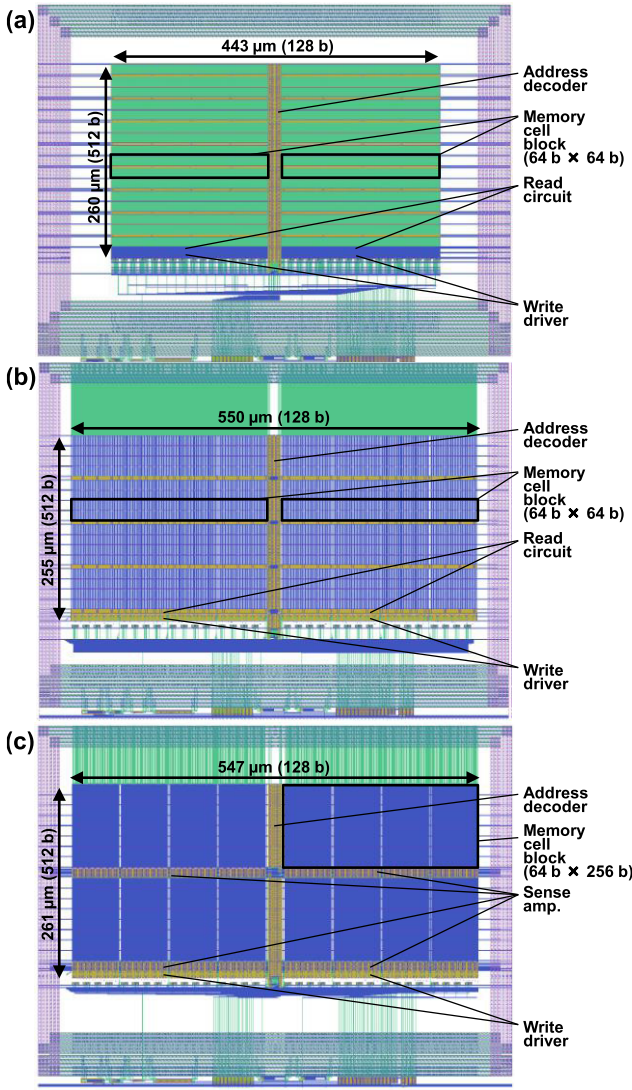

Fig. 9 Macro layouts of (a) 8T, (b) 10T-S, and (c) 10T-D SRAMs, in a 45-nm process technology. The total memory capacity of each macro is 64 kb.

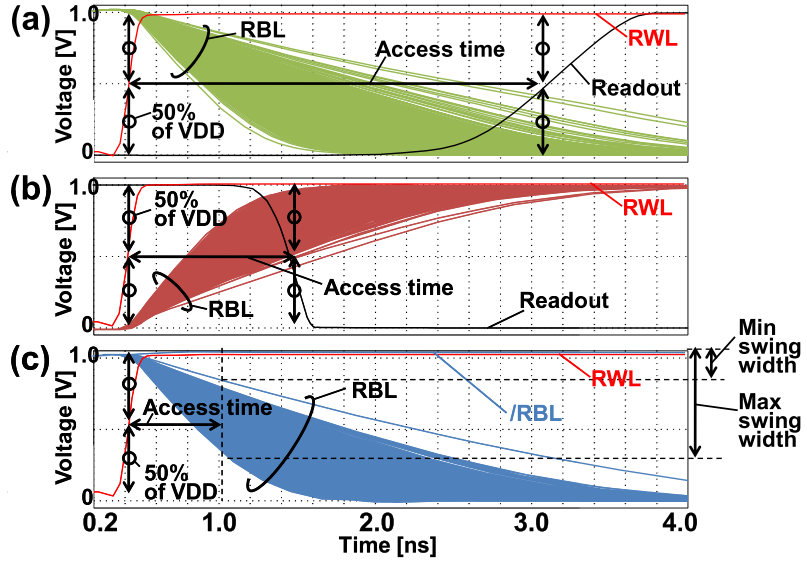

Fig. 10 Operation waveforms of (a) 8T, (b) 10T-S, and (c) 10T-D SRAMs at the SS corner (temperature = 25°C).

Carlo samples was 20,000, which is sufficient for the local variation with 20-kb SRAM. When considered more than 20-kb capacity SRAM, the Monte-Carlo samples need to be increased according to the capacity. The standard deviation σ for Vth variation of nMOS and pMOS are, respectively, $\sigma\,[\mathrm{V}] = 3.6/\sqrt{L_{\mathrm{eff}}\,[\mathrm{nm}] \cdot W_{\mathrm{eff}}\,[\mathrm{nm}]}$ and $\sigma\,[\mathrm{V}] = 2.7/\sqrt{L_{\mathrm{eff}}\,[\mathrm{nm}] \cdot W_{\mathrm{eff}}\,[\mathrm{nm}]}$, which are obtained from the Pelgrom plots based on ITRS 2005 [1]. In the Monte Carlo simulation, all transistors of an accessed memory cell and sense amplifier inverter are given Vth variation according to their L_{eff} and W_{eff}.

Figure 10 shows operating waveforms for the SRAMs of three kinds. In the figure, we adopt the SS corner model to simulate the worst-case delay. As it is shown in the Section 2.2, in the 10T-S SRAM, the sense-amplifier circuit optimization shows that charging time on RBL is 1.0 ns and discharging time on RBL is 0.99 ns. Thus, "1" readout is 0.01 ns longer than "0" readout and for 10T-S SRAM the worst case in a read operation is "1" readout (Fig. 10 (b)).

The following are the criteria used to calculate the access times:

- In the 8T SRAM, an access time is a period from a time at which an RWL rises to VDD/2 to a time at which an output of the sense amplifier is charged up to VDD/2.
- In the 10T-S SRAM, the access time is a longer one: periods from a time at which an RWL rises to VDD/2 to a time at which an output of the sense amplifier is charged up to 50% of VDD, or a period from a time at which an RWL rises up to VDD/2 to a time that an output of the sense amplifier is discharged down to VDD/2.
- In the 10T-D SRAM, the access time is a period from a time at which an RWL rises to VDD/2 to a time at which a differential voltage between an RBL and /RBL is expanded to 50 mV, 100 mV, or 200 mV.

In all SRAMs, the worst cell with the worst threshold-voltage combination determines the critical-path delay and operating frequency. **Figure 11** shows characteristics of the operating frequency when VDD is changed. The operating frequency is calculated as an inverse of a cycle time, which is a sum of a bitline charge–discharge time plus propagation delays in decoder circuits, a wordline, and sense amplifier circuits. The propagation delays in decoder circuits and a wordline are set to entirely same for all SRAMs. In this simulation of the operating

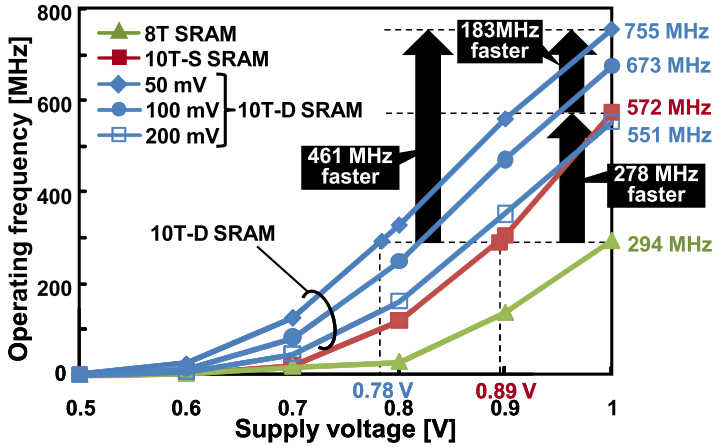

Fig. 11 Operating frequencies when a supply voltage is changed at the SS corner (temperature = 25°C).

frequency, the precharge periods in the 8T and 10T-D SRAMs are not considered because they can be overlapped completely with the decoder operation. The numbers of memory cells connected to a local RBL and a sense amplifier circuits are set to 64 for 8T and 10T-S SRAM and 256 for 10T-D SRAM. The sense amplifier circuits connected to a global RBL. In the simulation, the stored datum of accessed memory cell and the other memory cells are set to opposite, in order to consider worst cell leakage from un-accessed memory cells to the local RBL. The metal capacitances, according to the wire length, are appended to the local RBL and the global RBL. In the simulation, all transistors of an accessed memory cell and sense amplifier inverter are given the worst Vth combination according to 20,000-sampled Monte-Carlo simulation.

At supply voltages of 1.0 V, the 8T, 10T-S, and 10T-D SRAMs can run at 294 MHz, 572 MHz, and 755 MHz, respectively. The maximum 755 MHz is achieved in the 10T-D SRAM at a differential voltage of 50 mV. Consequently, probably the small differential voltage of 50 mV achieves high-speed operation. However, as described in Section 2.3, in the 10T-D SRAM, even if the sense point is targeted to 50 mV, most cells sink more than 50 mV on the bitline. Eventually, the differential voltage results in a large value at a low-voltage operation. Although the additional transistor (P4) is appended in the 10T-S SRAM (see Fig. 4 (a)) and increases an RBL capacitance, the 10T-S SRAM is faster than the 8T SRAM because neither the precharge circuit nor the keeper circuit is needed.

3.3 Power

Figure 12 presents a comparison in leakage power in a 45-nm process technology when stored data of 64 kb are random. The 8T SRAM cell has the lowest leakage power of the three because it has the fewest transistors. The 10T-S SRAM consumes the highest leakage power.

Figure 13 shows a density function of discharging period of 10T-D SRAM from a time at which an RWL rises to VDD/2 to a time at which a differential voltage between RBL and /RBL is expanded to 50 mV when the number of Monte-Carlo samples is set to 20,000. The figure indicates that for 10T-D SRAM discharging time variation deteriorates as the supply voltage is decreased. To ensure the statistically weak cell operation, the sense enable signal becomes to step away from mean timing as the supply voltage is decreased. For example at 0.7-V

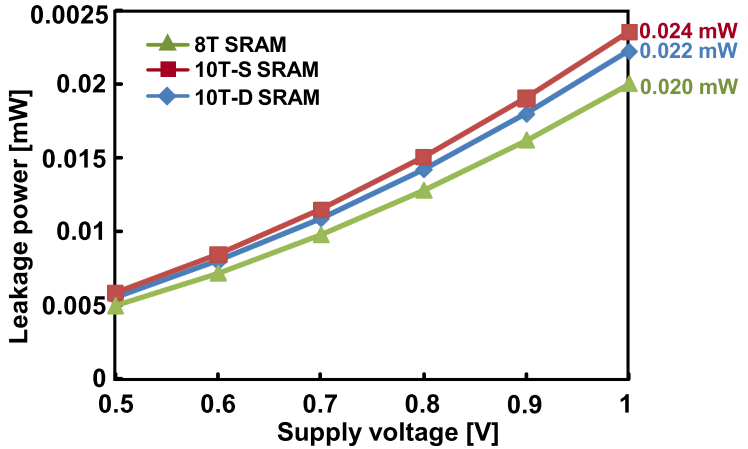

Fig. 12 Leakage power comparison in the 8T, 10T-S, and 10T-D SRAMs at the CC corner (temperature = 25°C).

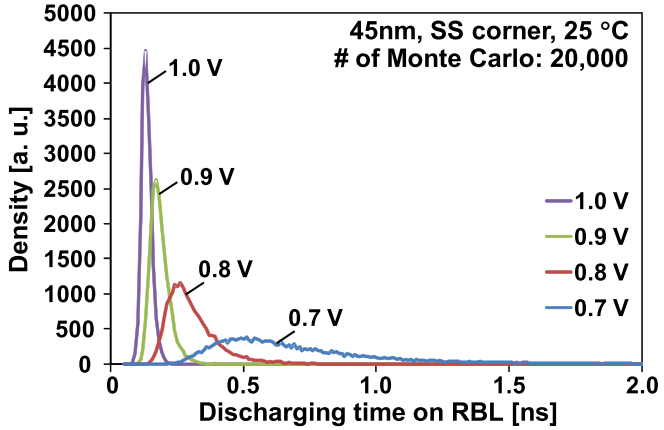

Fig. 13 Density function of discharging time on RBL variation of 10T-D SRAMs.

operation, the worst cell needs 5.98 ns for getting 50-mV differential voltage, although the mean discharging time is 0.717 ns. This is 5.98 − 0.717 = 5.263 ns mismatch, and it leads to much larger bitline amplitudes than 50 mV. For 10T-D SRAM, this sense enable timing mismatch becomes marked as the supply

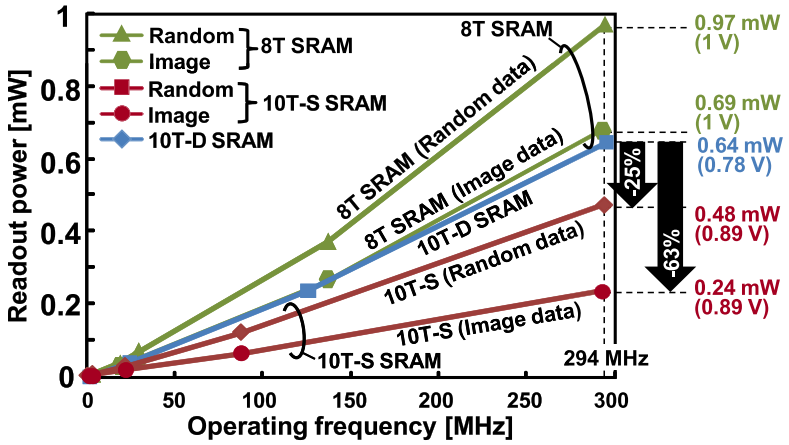

Fig. 14 Readout power versus operating frequencies in a 45-nm process technology at the CC corner (temperature = 25°C).

voltage is decreased, because the σ value of this density function is expanding as the supply voltage is decreased. We conducted the cyclopedic simulation and statistical analysis at several operation voltages, 0.78 V, 0.7 V, 0.6 V, and 0.5 V, in order to obtain the mean bitline amplitudes and readout power. The results are 576.4 mV, 662.3 mV, 599.8 mV, and 499.9 mV at 0.78 V, 0.7 V, 0.6 V, and 0.5 V, respectively. These results indicate that at low voltage operation the 10T-D SRAM needs almost full-swing readout in spite of its differential operation mechanism.

Figure 14 presents a comparison of the readout powers in the 8T, 10T-S, and 10T-D SRAMs. Actually, VDD is changed in the lines, according to Fig. 11. The 10T-S SRAM uses the least power because the transition possibility of the RBL is 50% when a sequence of random data is considered. However, in the 10T-D SRAM, as the supply voltage is decreased, the average voltage differential between the RBL and /RBL becomes more than 80% of VDD, as described above, even if the sense point is set to 50 mV. The readout power in the 10T-S SRAM is 25% lower than that of the 10T-D SRAM at the operating frequency of 294 MHz when random data are considered. The saving factor is maximized to 63% if the readout data have statistical similarity to H.264 reconstructed image data [5]. For

8T SRAM, the power saving scheme has been proposed with majority logic and data-bit reordering [14]. This scheme can save 28% readout power when image data are considered.

4. Conclusion

As described in this paper, we examined dual-port SRAM design in terms of its area, speed, and readout power in a 45-nm process technology. Although the 8T SRAM has the lowest transistor count, and is the most area efficient, the readout power is large and the cycle time increases because of peripheral circuits. The 10T differential-port SRAM would operate fastest if the differential voltage were set to 50 mV. The 10T SRAM with a single-end read port consumes the least power.

Acknowledgments This work was supported by Renesas Electronics Corporation.

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Hiroki Noguchi received his B.E. and M.E. degrees in Computer and Systems Engineering in 2006 and 2008, respectively from Kobe University, Hyogo, Japan, where he is currently earning a Ph.D. degree. His research interests are low-power SRAM designs, multimedia/ubiquitous systems and digital signal processing architectures, which include speech-recognition for handheld, image-recognition for wearable computing, and mixed integer programming for real-time robotics controlling, and their low-power hardware implementation. He is a student member of IEICE and IEEE.

Yusuke Iguchi received his B.E. and M.E. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2007 and 2009, respectively. He is currently working at OSAKA GAS Corporation. His current research is ultra-low-power techniques in digital LSIs and memories, and high reliable SRAM designs for severe operating environments.

Hidehiro Fujiwara received his B.E., M.E. and Ph.D. degrees in Electrical Engineering from Kobe University, Kobe, Japan, in 2005, 2006, and 2009, respectively. He joined an internship program at Takumi Technology B.V., Eindhoven, the Netherlands in 2008. In 2009, he joined Renesas Technology Corporation, Tokyo, Japan. In 2010, he was transferred to Renesas Electronics Corporation, where he has been working on designing embedded SRAM for advanced CMOS logic process. He is a member of IEICE and IEEE.

Shunsuke Okumura was born on August 17, 1984. He received his B.E. and M.E. degrees in Computer and Systems Engineering in 2008 and 2010, respectively from Kobe University, Hyogo, Japan, where he is currently working in the doctoral course. His current research is high-performance, low-power SRAM designs, dependable SRAM designs, and error correcting codes implementation. He is a student member of IPSJ, IEICE and IEEE.

Koji Nii received his B.E. and M.E. degrees in Electrical Engineering from Tokushima University, Tokushima, Japan, in 1988 and 1990, respectively, and Ph.D. degree in Informatics and Electronics Engineering from Kobe University, Hyogo, Japan, in 2008. In 1990, he joined the ASIC Design Engineering Center, Mitsubishi Electric Corporation, Itami, Japan, where he has been working on designing embedded SRAMs for CMOS ASICs. In 2003, he was transferred to Renesas Technology Corporation, Itami, Japan, which is a joint company of Mitsubishi Electric Corporation and Hitachi Ltd. in the semiconductor field. He transferred his work location to Kodaira, Tokyo from Itami, Hyogo on April 2009, and his current responsibility is Section Manager. He holds over 70 issued US Patents. He currently works on the research and development of deep-submicron embedded SRAM in the Embedded SRAM Development Department of Renesas Electronics Corporation, Kodaira, Tokyo, Japan. Dr. Nii received the Best Paper Awards at IEEE International Conference on Microelectronic Test Structures (ICMTS) in 2007. He is a Technical Program Committee of the IEEE CICC. He is a member of the IEEE Solid-State Circuits Society and the IEEE Electron Devices Society.

Hiroshi Kawaguchi received his B.E. and M.E. degrees in Electronic Engineering from Chiba University, Chiba, Japan, in 1991 and 1993, respectively, and earned a Ph.D. degree in Engineering from The University of Tokyo, Tokyo, Japan, in 2006. He joined Konami Corporation, Kobe, Japan, in 1993, where he developed arcade entertainment systems. He moved to the Institute of Industrial Science, The University of Tokyo, as a Technical Associate in 1996, and was appointed as a Research Associate in 2003. In 2005, he moved to Kobe University, Kobe, Japan. Since 2007, he has been an Associate Professor with the Department of Information Science at that university. He is also a Collaborative Researcher with the Institute of Industrial Science, The University of Tokyo. His current research interests include low-voltage SRAM, RF circuits, and ubiquitous sensor networks. Dr. Kawaguchi was a recipient of the IEEE ISSCC 2004 Takuo Sugano Outstanding Paper Award and the IEEE Kansai Section 2006 Gold Award. He has served as a Design and Implementation of Signal Processing Systems (DISPS) Technical Committee Member for IEEE Signal Processing Society, as a Program Committee Member for IEEE Custom Integrated Circuits Conference (CICC) and IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), and as a Guest Associate Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences and IPSJ Transactions on System LSI Design Methodology (TSLDM). He is a member of the IEEE, ACM, IEICE, and IPSJ.

Masahiko Yoshimoto earned his B.S. degree in Electronic Engineering from Nagoya Institute of Technology, Nagoya, Japan, in 1975, and M.S. degree in Electronic Engineering from Nagoya University, Nagoya, Japan, in 1977. He earned a Ph.D. degree in Electrical Engineering from Nagoya University, Nagoya, Japan in 1998. He joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan, in April 1977. During 1978–1983 he was engaged in the design of NMOS and CMOS static RAM including a 64K full CMOS RAM with the world's first divided-wordline structure. From 1984, he was involved in research and development of multimedia ULSI systems for digital broadcasting and digital communication systems based on MPEG2 and MPEG4 Codec LSI core technology. Since 2000, he has been a Professor of the Department of Electrical and Electronic Systems Engineering at Kanazawa University, Japan. Since 2004, he has been a Professor of the Department of Computer and Systems Engineering at Kobe University, Japan. His current activities are focused on research and development of multimedia and ubiquitous media VLSI systems including an ultra-low-power image compression processor and a low-power wireless interface circuit. He holds 70 registered patents. He served on the Program Committee of the IEEE International Solid State Circuit Conference from 1991 to 1993. Additionally, he served as a Guest Editor for special issues on Low-Power System LSI, IP, and Related Technologies of IEICE Transactions in 2004. He received R&D100 awards in 1990 and 1996 from R&D Magazine for development of the DISP and development of a real-time MPEG2 video encoder chipset, respectively.