A 14 µA ECG Processor with Robust Heart Rate Monitor for a Wearable Healthcare System

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***Abstract*— This report describes an electrocardiograph (ECG) processor for use with a wearable healthcare system. It comprises an analog front end, a 12-bit ADC, a robust Instantaneous Heart Rate (IHR) monitor, a 32-bit Cortex-M0 core, and 64 Kbyte Ferroelectric Random Access Memory (FeRAM). The IHR monitor uses a short-term autocorrelation (STAC) algorithm to improve the heart-rate detection accuracy despite its use in noisy conditions. The ECG processor chip consumes 13.7 µA for heart rate logging application.**

I. Introduction

Because of the advent of an aging society in Japan, mobile health plays an ever more prominent role [1]. Daily-life monitoring is especially important in preventing lifestyle diseases, which have rapidly increased the number of patients and elderly people requiring nursing care. Our goal is the monitoring and display of vital signals and physical activity in daily life to improve users' quality of life and realize a smart society.

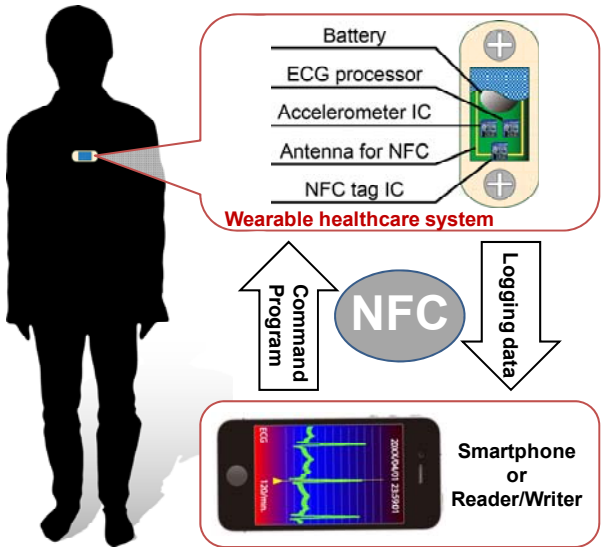

Figure 1. Wearable healthcare system overview.

We propose an Instantaneous Heart Rate (IHR) monitoring and electrocardiograph (ECG) processor for use in a wearable healthcare system. The IHR is an important bio-signal used for heart disease detection, heart rate variation analysis [2], and exercise intensity estimation [3].

Key factors affecting wearable system usability are miniaturization and weight reduction. However, a wearable ECG monitor is sensitive to extraneous noise because its electrodes are close together. The SNR of ECG signals will be especially degraded if a user is not at rest. Consequently, a sophisticated and costly analog front end is usually required. However, the feature and purpose of our approach is digital signal processing to reduce the performance requirements of the analog portion and to minimize the overall system power consumption. The battery weight is a dominant characteristic of the wearable system. Therefore, the battery capacity and power consumption must be limited as much as possible.

II. System Description and Processor Architecture

Fig. 1 presents an overview of the wearable healthcare system, comprising the proposed ECG processor, Near Field Communication (NFC) tag IC, and accelerometer IC. The NFC is used for program loading, individual optimization, and data retrieval from the ECG processor. Compared with Bluetooth Low Energy or ZigBee, the standby power of NFC is extremely small. The active communication energy is also consumed by a reader/writer side when using a passive NFC tag. Therefore, the proposed system uses NFC to cooperate with a Smartphone (or reader/writer).

Fig. 2 presents a block diagram showing the proposed ECG processor, which consists of an ECG sensing block, Ferroelectric Random Access Memory (FeRAM), 32-bit Coretex-M0 core, and extra interfaces. Because the frequency range of vital signals is low (less than 1 kHz), both the standby power reduction and sleep time maximization are important to minimize the total power consumption. The 64-Kbyte FeRAM is integrated as a data buffer for daily life monitoring because

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the leakage current of the data buffer is dominant in the standby state.

The ECG sensing block has an analog front end (AFE), a 12-bit SAR ADC, and a robust IHR monitor. The AFE includes a 34-dB gain instrumental amplifier and a 20-dB gain amplifier. The ADC sampling rate can be set to 1 kSamples/s for ECG processing mode and 128 Samples/s for IHR monitoring mode. The robust IHR monitor is the main contribution of this study.

The operating frequency of the Cortex M0 core, which is used for an on-node vital signal processing, is 24 MHz, whereas the operating frequency of other digital blocks is 32 kHz. The slow signals in the 32-kHz domain are synchronized at the low-speed bus to the 24-MHz domain. When the Cortex M0 core is in a deep sleep state, the on-chip 24-MHz oscillator is also stopped.

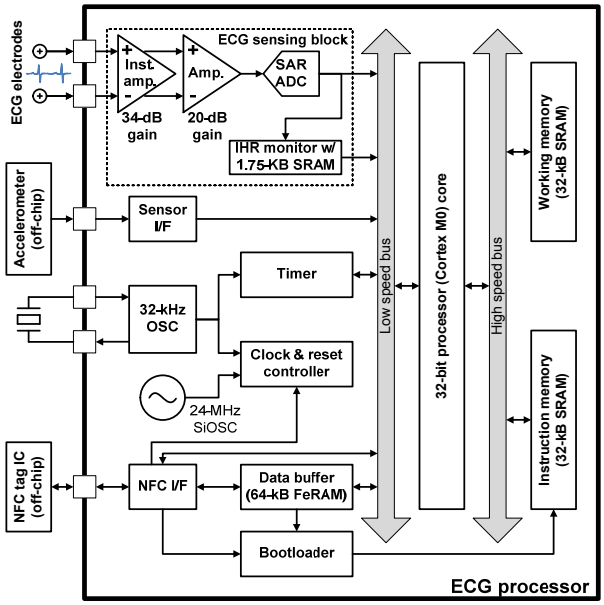


Figure 2. Block diagram of ECG processor.

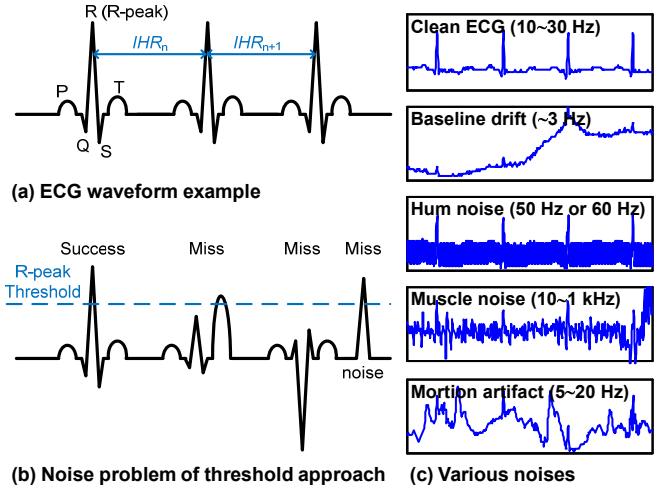


Figure 3. Threshold based R-wave detection and its noise problems in wearable healthcare systems.

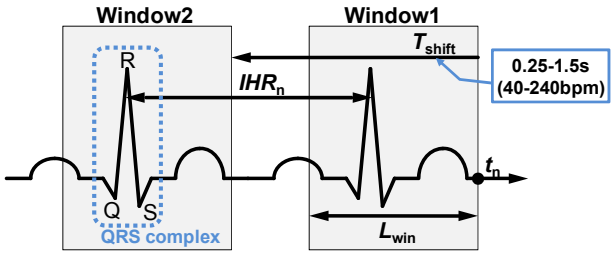


Figure 4. IHR extraction with short-term autocorrelation (STAC).

III. Robust Instantaneous Heart Rate Monitor

A. *Heart rate extraction algorithm in wearable healthcare*

Extracting R-waves (see Fig. 3(a)) with threshold determination is a general approach. Recently, various statistical approaches have been proposed for noise-tolerant threshold calculation such as using root-mean-squares (RMS) [4], standard deviations (SD), and mean deviations (MD) [5]. However, as depicted in Fig. 3, both misdetection and false detection are increased in the wearable healthcare system by noise from various sources such as myoelectric signals from muscle and electrode movement because the power consumption and electrode distance of the wearable sensor are strictly limited to reduce its size and weight.

Autocorrelation [6, 7] and template matching [8] are more robust approaches to prevent incorrect detection because these algorithms use the similarity of QRS complex waveforms and have no threshold calculation process. Autocorrelation has been used in a non-invasive monitoring system [7]. However, the method necessitates numerous computations because it calculates the average heart-rate over a long duration (30 s). In our previous work, a short-term autocorrelation (STAC) technique was proposed for IHR detection [9].

Fig. 4 portrays IHR extraction using STAC. As depicted in Fig. 4 and (1–4), the IHR at time t_n (IHR_n) is obtained as a window shift length (T_{shift}) that maximizes the correlation coefficient between the template window and the search window (CC_n). The STAC method can improve the noise tolerance about 5.6 dB with a 95% success rate.

$$CC_n[T_{shift}] = w_1 \cdot \sum_{i=0}^{L_{win}-1} Q_w[t_n - i] \cdot Q_w[(t_n - T_{shift}) - i] \quad (1)$$

$$IHR_n = \arg_{0.25\times F_s \le T_{shift} \le 1.5\times F_s} \max \{CC_n[T_{shift}]\} \quad (2)$$

$$L_{win} = 1.5 \times F_s \quad (3)$$

$$w_1 = \begin{cases} 1 & (T_{shift} \le 0.546 \times F_s) \\ 0.75 & (0.546 \times F_s < T_{shift} \le 0.983 \times F_s) \\ 0.5 & (0.983 \times F_s < T_{shift}) \end{cases} \quad (4)$$

In the equations presented above, F_s, L_{win}, and w_1 respectively denote the sampling rate (samples/s), the window length, and the weight coefficient. The value of T_{shift} is set as 0.25 s to 1.5 s because the heart rate of a healthy subject is 40 bpm to 240 bpm. The L_{win} is updated according to the estimated IHR to reduce the computational amount and to improve the IHR estimation accuracy. Then, the range of L_{win} and w_1 is

determined by the maximum rate of the beat-to-beat variation, which is generally 20% in a healthy subject [10].

B. Hardware implementation of the heart rate monitor

In this work, we introduce a robust IHR monitor, which employs two-step noise reduction technique. In the first stage, a quadratic spline wavelet transform (QSWT) [11] is used to mitigate the baseline wander and hum noise. The QSWT requires few calculations and low hardware cost because it can be implemented using only adders and shift operators. Fig. 5 presents a block diagram and frequency characteristics of the QSWT with 128-Hz sampling rate. The base-line wander and hum noise can be removed easily using QSWT. Unfortunately, it is difficult to remove the myoelectric noise and electrode motion artifacts only using QSWT because these frequency ranges are similar to the desired ECG signal.

Therefore, in the second stage, the IHR is extracted using the STAC method. The STAC is also implemented as dedicated hardware to minimize the power overhead. Fig. 6 presents the block diagram of the IHR monitor and STAC processing core. Each STAC core has CC buffer to store the intermediate value of $CC_n[T_{shift}]$ in (1). The CC buffer is updated in synchronization with ADC output (see Fig. 7). Since the L_{win} is 1.5 s and because IHR is updated every second, two STAC cores alternately calculate IHR with 0.5 s overlap.

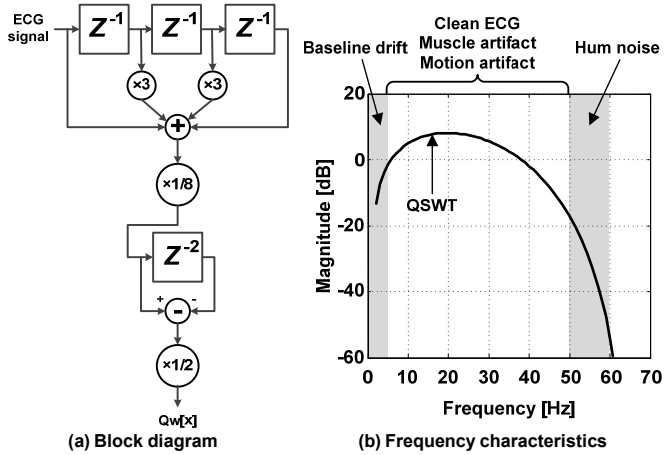


Figure 5. Block diagram and frequency characteristics of QSWT.

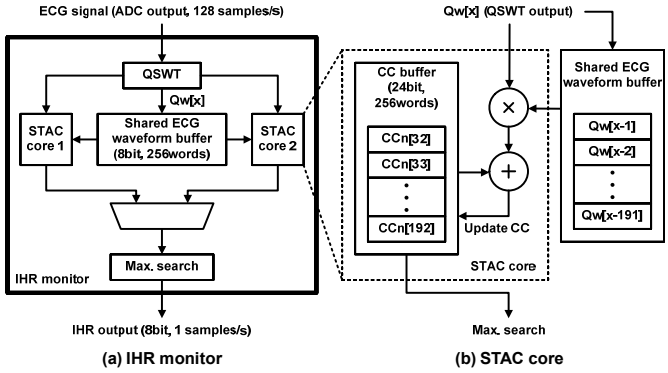


Figure 6. Block diagram of robust IHR monitor.

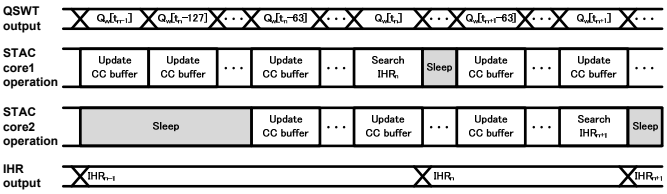


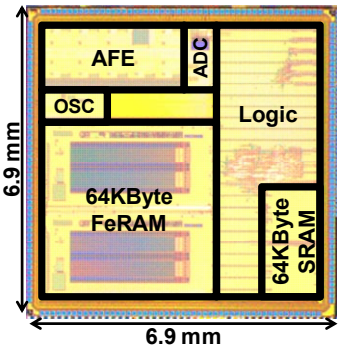
Figure 7. Timing chart of IHR extraction.

The gate level simulation result shows the IHR monitor block, which contains QSWT, two STAC cores, and SRAMs, consumes 1.21 μA. The digital logic and SRAMs respectively consume 0.26 μA and 0.95 μA.

IV. Implementation Result

The test chip is fabricated using 130-nm CMOS technology. Fig. 8 presents a chip photograph and a performance summary. The operating voltage is 1.2 V for AFE, ADC, SRAM, 24-MHz oscillator, and digital blocks. The FeRAM, 32-KHz oscillator, and IO circuits are operated with 3.0 V supply voltage.

To demonstrate the test chip performance, we implemented a heart rate logging application. The experimental environment is presented in Fig. 9. In this experiment, an Android™ smartphone is used for program loading and logging data retrieval. As portrayed in Fig. 10, the IHR is extracted correctly in a noisy condition.



Technology		130-nm CMOS
Supply voltage		1.2V (Digital, SRAM, ADC, AFE)
		3.0V (FeRAM, 32kHz OSC, I/O)
Chip area		6.9 mm x 6.9 mm
Frequency		24 MHz (for MCU)
		32 kHz (for other blocks)
MCU		32-bit Cortex M0
On chip memory		64-KB FeRAM (for logging data)
		64-KB SRAM (for MCU)
		1.75-KB SRAM (for IHR detector)
ADC	Resolution	12 bit
	Current	0.5 μA@128 S/s, 1.4 μA@1 kS/s
AFE	Gain	54 dB
	Bandwidth	0-100 Hz
	Current	3.4 μA
Total current		12.7 μA (for heart rate logging)

Figure 8. Chip photograph and chip specifications.

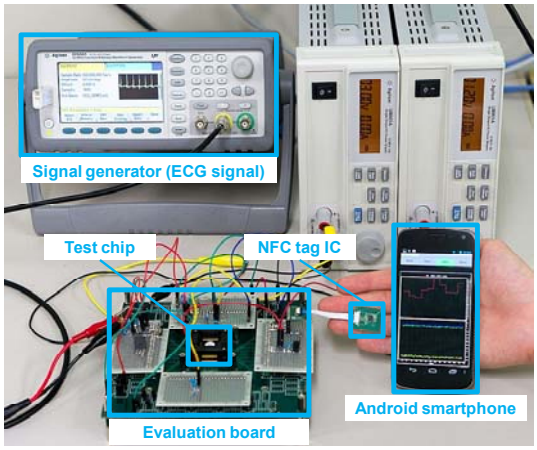


Figure 9. Experimental environment.

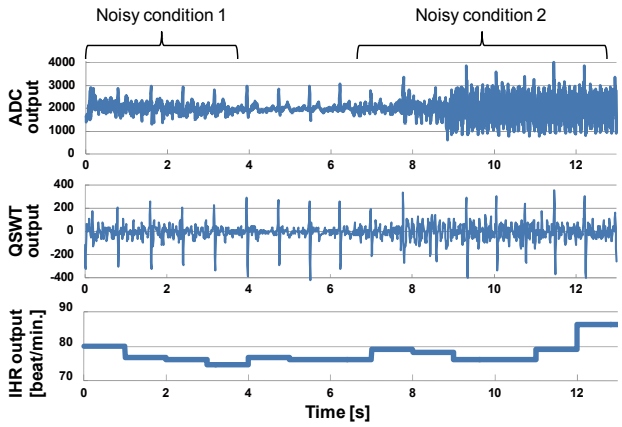


Figure 10. Measured waveform of IHR monitor in a noisy condition.

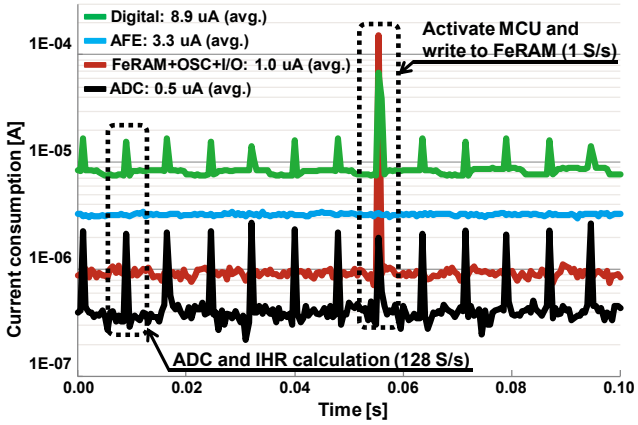


Figure 11. Measurement result of current consumption with a heart rate logging application.

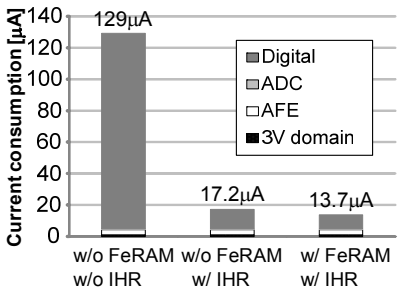


Figure 12. Contribution of dedicated IHR monitor and FeRAM.

Fig. 11 portrays the current consumption with a heart rate logging application. In this experiment, the ADC sampling rate and the logging interval of IHR are set respectively to 128 Samples/s and 1 Sample/s. Then the AFE, 32-kHz OSC, and Timer block are always activated. The measurement results show that the test chip consumes 13.7 µA on average for the heart rate logging application. The peak current, which is consumed when the Cortex and FeRAM are activated to store the logging IHR data every second, is less than 1 mA.

As presented in Fig. 12, the IHR monitor and FeRAM respectively contribute to active ratio reduction and sleep power reduction. Table 1 presents a performance comparison of the ECG processor. Compared with earlier ECG processors, the proposed processor has lower power and grater memory capacity for daily-life monitoring.

V. Conclusion

As described in this paper, we proposed a low-power ECG processor with a robust heart rate monitor. The robust heart rate monitor can correctly extract a heart rate from noisy environments using the STAC algorithm. The measured total current consumption is 13.7 µA at 1.2V and 3.0V power supply for the heart rate logging application.

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TABLE I. Performance Comparison with Previous Studies

	This work	ISSCC'12 [12]	VLSI'11 [13]
Technology	130 nm	130 nm	180 nm
Supply voltage	1.2V/3.0V	0.3-0.7V	1.2V
Frequency	24 MHz/32 kHz	1.7 MHz-2 kHz	1 MHz
MCU	Cortex M0 (32 bit)	8b RISC	n/a
On chip memory	129.75 kB	5.5 kB	46 kB
Total power for heart rate extraction	18.24 µW	19 µW	31.1 µW
Total current for heart rate extraction	13.7 µA	>27 µA	25.9 µA