0.42-V 576-kb 0.15-µm FD-SOI SRAM with 7T/14T Bit Cells and Substrate Bias Control Circuits for Intra-Die and Inter-Die Variability Compensation

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1. Abstract

We propose 7T/14T FD-SOI SRAM with a substrate bias control mechanism. The 14T configuration suppresses intra-die variation in a bit cell. The substrate bias control circuits detect a threshold voltage and automatically change it with the substrate bias. Thereby, the inter-die variation is suppressed. By combining these two schemes, we confirmed that a 576-kb SRAM test chip in a 0.15-µm FD-SOI works at 0.42 V.

2. Introduction

In an SoC (system on a chip), SRAM occupies an area of 90% or more of a silicon die [1], meaning that SRAM is the most sensitive device to process variation. To make matters worse, read and write margins in a 6T bit cell are decreased with lowering a supply voltage. Fig. 1 (so-called Yamaoka plot [2]) illustrates it by relations between read/write limit lines and process corners. At an FS (SF) corner, SRAM has the least read (write) margin.

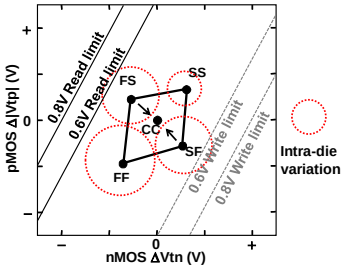

Fig. 1: *Yamaoka plot.*

3. 7T/14T SRAM with Substrate bias

To maximize the operating margin in SRAM, both of the inter-die and intra-die variations must be suppressed. As shown in Fig. 2, the FS/SF corner can be converged on the CC corner with an FD-SOI substrate bias [3], which means the suppression of the inter-die variation. In this paper, we apply this FD-SOI substrate bias control to a 7T/14T bit cell [4] in order to suppress the other component: the intra-die variation.

Fig. 3 portrays the 7T/14T bit cell that has two operating modes: normal mode and dependable mode. In the normal mode, a 7T bit cell stores one-bit information. In the dependable mode, a 14T bit cell combining a pair of 7T bit cells does so, too; however, it can suppress the intra-die variation. This is because a β ratio is doubled in a read operation, and a conductance of access gates are averaged in a write operation. The normal and dependable modes are switched by activating and deactivating two connecting transistors.

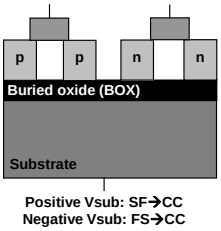

Fig. 2: *FD-SOI substrate bias control.*

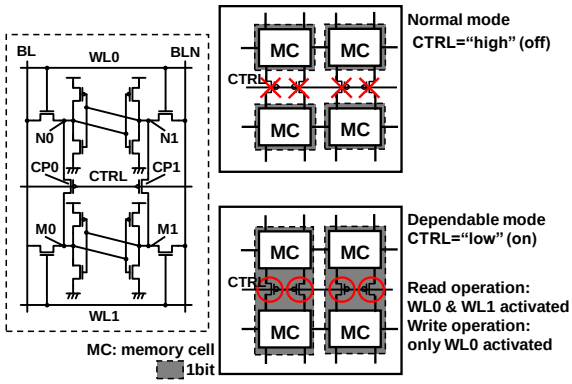

Fig. 3: *7T/14T bit cell.*

4. Circuit Implementation and Results

Fig. 5 is a micrograph of a 576-kb (512 rows × 8 columns × 16 bits/word × 9 blocks) 7T/14T SRAM test chip in a 0.15-um FD-SOI process with the substrate bias control circuits.

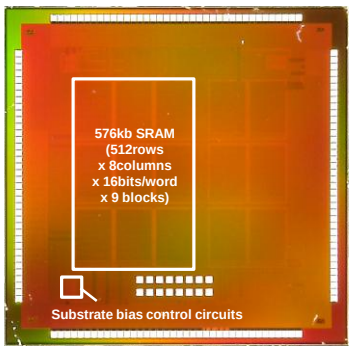

Fig. 4: *Test chip (FS corner).*

Fig. 5(a) shows a block diagram of the proposed substrate bias control circuits. Fig. 5(b) shows a Vt detector. "Detect" is an analog signal that changes from Vdd to the ground according to a process condition. Fig. 5(c) shows a half-Vdd generator using body-tie transistors. Respective "Ref+" and "Ref–" are set to slightly higher and lower voltages than a half Vdd, regardless of the process condition. The substrate bias (Vsub) is controlled so that "Detect" is always kept between "Ref+" and "Ref–". In this way, the FS/SF corners converge on the CC corner.

Fig. 6(a) expresses simulated output voltages of the Vt detector and half-Vdd generator when the process condition is varied. Fig. 6(b) depicts measured data obtained from the test chip around the SF corner. In this case, the proposed control circuits outputs a substrate bias of 3.4 V to suppress the inter-die variation.

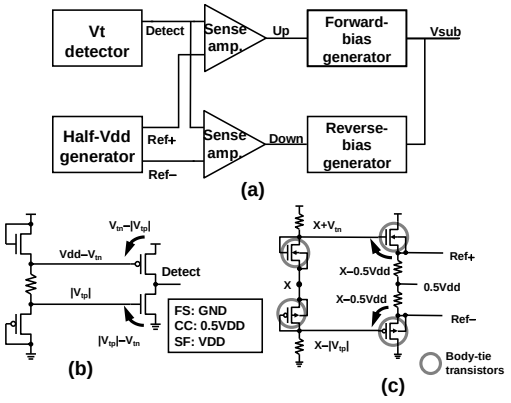

Fig. 5: *Proposed substrate bias control circuits: (a) block diagram, (b) Vt detector, and (c) half-Vdd generator.*

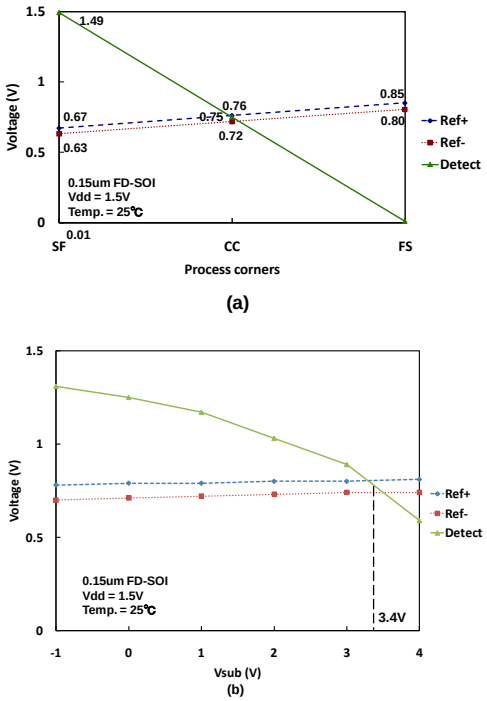

Fig. 6: *(a) Simulated and (b) Measured output voltages of Vt detector and half-Vdd generator.*

Fig.7 illustrates the bit error rates (BER) of the test chip around the FS corner. Although the retention voltage on the test chip is 0.43 V without the 14T configuration or substrate bias control, it can be lowered to 0.28 V with the two schemes (Fig. 7(a)). The operating voltage is also improved from 0.74 V to 0.42 V in the case where the intra-die and inter-die variability compensation is both treated (Fig. 7(b)).

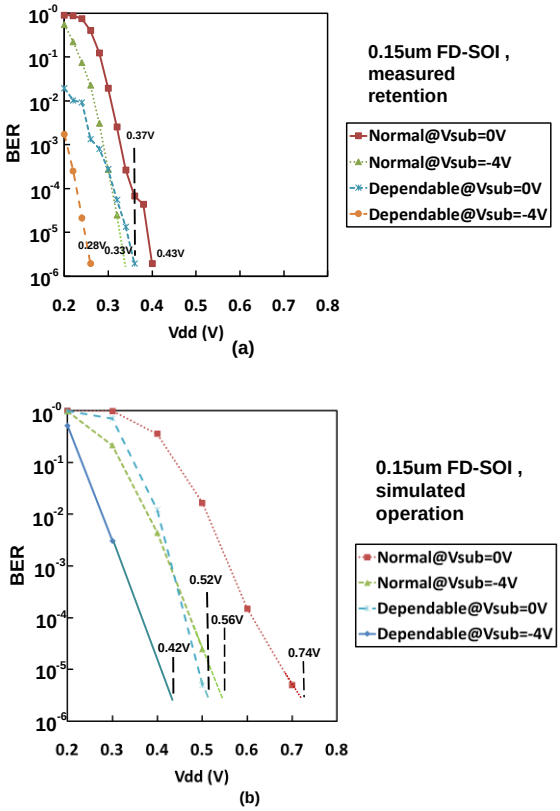

Fig. 7: *Bit error rates (BERs) in: (a) retention and (b) operation (read/write) on the test chip.*

6. Summary

We proposed 7T/14T FD-SOI SRAM with substrate bias control circuits. We confirmed that the 0.15-µm SRAM test chip can reduce the minimum retention and operating voltage to 0.28 V and 0.42 V, respectively.

Acknowledgments

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References

[1] International Technology Roadmap for Semiconductors (ITRS) Report.
[2] M. Yamaoka, et al., IEEE JSSC, vol. 41, no. 3, pp. 705-711, 2006.
[3] H. Fujiwara, et al., IEEE SOI Conf., pp. 93-94, 2008.
[4] H. Fujiwara, et al., ISQED, pp. 98-102, 2008.