An 8-bit I/O-Sized ADC with Second-Order TDC and MOM Capacitor Voltage-to-Time Converter

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***Abstract*— We present an I/O-sized second-order analog to digital converter (ADC) combined with a time-to-digital converter (TDC) and a voltage-to-time converter (VTC). Our proposed VTC is optimized for metal–oxide–metal (MOM) capacitances, and is charged to the MOM capacitances by an input voltage. In a standard 65-nm CMOS process, an SNR of 50 dB (8 bits) is achievable at an input signal frequency of 78 kHz and a sampling rate of 20 MHz, where the respective area and power are 6468 mm^2 and 509 µW. The active area of the proposed ADC is smaller than an I/O buffer. The proposed ADC is useful as an ADC I/O.**

I. Introduction

Various techniques have been developed to realize ubiquitous computing for sensors. With implementation of more sensors, more analog-to-digital converters (ADCs) are required by the many sensors to digitize the many channel signals [1]. To date, the ADCs on an LSI chip have been limited numerically by the chip area. To achieve high accuracy, for instance, an SAR ADC requires large capacitors for which the area cannot be scaled down with process scaling.

Fig. 1 presents the points of emphasis of this work. We propose a smaller ADC than an I/O buffer size. We adopt a time-to-digital converter (TDC) suited to multiple-channel applications because it can be configured by digital circuits and because it can be extended easily to advanced CMOS process node. However, the small-area TDC, which can be realized within performance constraints at a low cost, needs an external circuit to convert an analog signal to a time-domain signal. As described in this paper, we propose a voltage-to-time converter (VTC) using metal–oxide–metal (MOM) capacitance, which achieves linearity that is as good as that of the TDC.

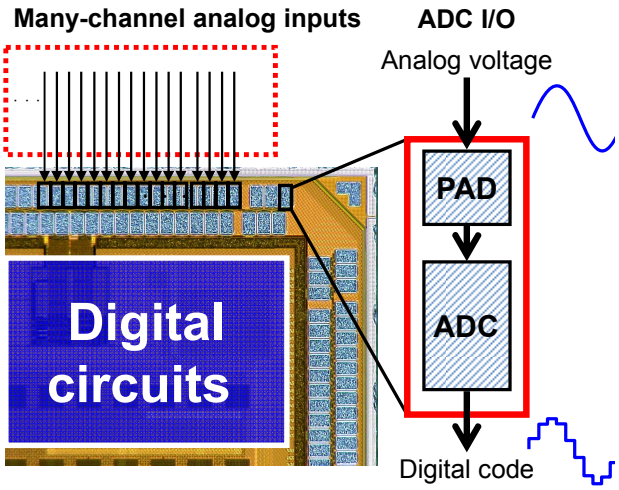

Fig. 1. ADC I/Os for multiple-channel analog inputs.

II. Proposed Voltage-To-Time Converter Core Circuit

A schematic of our proposed VTC core is depicted in Fig. 2. Our proposed VTC circuit, which consists of two MOM capacitances, converts an analog voltage (V_{IN}) to a time interval. The circuit changes a discharging charge by V_{IN}. The two MOM capacitances, C_1 and C_2, are connected with the supply voltage (*VDD*) and a V_{IN} switch circuit. The V_{IN} switch circuit propagates a V_{IN} analog voltage or the ground (*VSS*) to C_2. Therefore the charge amount of C_2 is changed by V_{IN}. A tristate buffer includes a current source. The non-overlap signals (*DCG* and *PCG*) control the C_1 and C_2 charges and discharges.

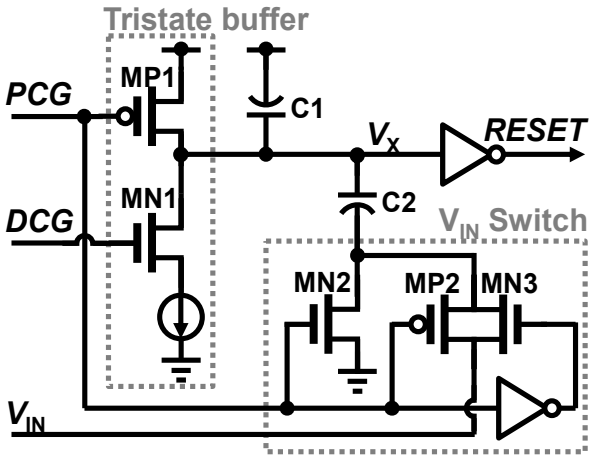

Fig. 2. Schematic of the proposed voltage-to-time converter.

Fig. 3 shows the mechanism and the timing diagram of proposed VTC core circuit. First, while *DCG* and *PCG* are

'low', the pMOS transistor (MP1) charges V_X to *VDD*; the charge on V_X is a sum of the charges of C_1 and C_2 represented as

$$Q_1 + Q_2 = 0 + C_2 \cdot (VDD - V_{IN}), \quad (1)$$

where Q_1 and Q_2 are charges of C_1 and C_2. Next, when the *PCG* becomes 'high', the V_{IN} switch is flipped from V_{IN} to *VSS*. The charges of C_1 and C_2 are shared at V_X. Therefore, its voltage is controlled by V_{IN} as

$$Q_1' + Q_2' = C_1 \cdot (V_{XN} - VDD) + C_2 \cdot (V_{XN} - VSS), \quad (2)$$

where V_{XN} is a stable voltage after *PCG* becomes 'high'. Eventually, from (1) and (2), V_{XN} can be given as

$$V_{XN} = VDD - \frac{C_2}{C_1 + C_2} \cdot V_{IN}. \quad (3)$$

The charge amount is defined by the capacitances of C_1 and C_2, and the voltage of V_{IN}. Next, *DCG* becomes 'high', and the nMOS transistor (MN1) and a current source discharges the charge. When V_X becomes lower than a threshold voltage (V_{TH})

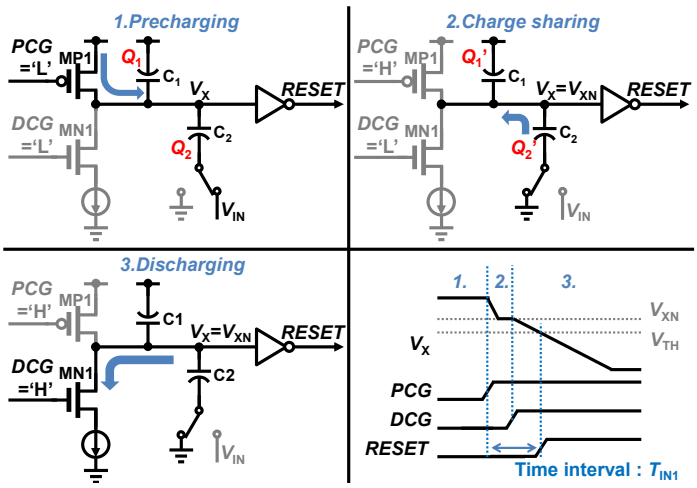

Fig. 3. Operation of the proposed VTC core circuit.

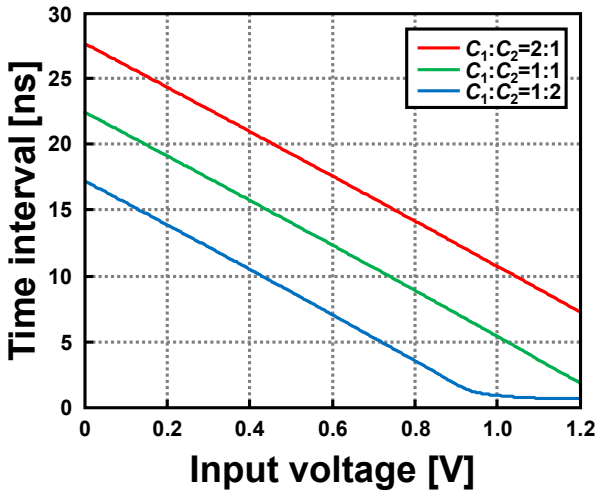

Fig. 4. Simulation result of the VTC core.

of the inverter, *RESET* becomes 'high'. From (3), the interval in which V_X becomes lower than V_{TH} depends on V_{XN} and depends on the time at which the rising edge of *RESET* is changed. Therefore, this VTC core circuit can convert the voltage domain to the time domain.

Fig. 4 presents the SPICE simulation result of the proposed VTC core circuit. The vertical axis is the time interval from the rising edge of *PCG* to the rising edge of *RESET*. The horizontal axis is the analog input voltage V_{IN}. The time interval is varied with the capacitance ratio and the current amount of the current source. The output characteristic is not completely linear because the discharging speed of the current source is not perfectly constant. To eliminate the nonlinearity characteristics, the proposed ADC has a nonlinearity corrector (see the next section).

III. Proposed I/O-Sized ADC

We propose an IO-sized ADC that consists of the small area VTC and a frequency shift oscillator (FSO) TDC [2], as presented in Fig. 5. The VTC generates non-overlap signals, *DCG* and *PCG*, using a clock signal (*CLK*) to control the VTC core circuit. An SR Latch connected to the VTC core circuit outputs the time interval, T_{IN1} (time from the rising edge of *CLK* (≈ *PCG*) to the rising edge of *RESET*), as explained in the previous section. The VTC core circuit is precharged again by its own *RESET*. In doing so, it is possible to make the circuit operation fast and to prepare for the next *CLK* pulse.

In [2], timing jitters affect the TDC performance. To improve it, we adopt an FSO comprised of the Schmitt trigger inverter oscillator instead of normal inverters (Fig. 6). It can absorb noise from the power supply and reduce jitters on the output. After converting an analog voltage to a digital code, the ADC can correct its nonlinearity using digital signal processing (DSP) because the VTC characteristic is monotonic. The DSP coefficients for the nonlinearity correction are obtained by DC sweep in Fig. 5 at the initial calibration phase.

Fig. 7 shows the operating waveforms of the proposed ADC. When *CLK* becomes 'high', the DFF outputs 'high' for *PCG* and *DCG*. After *DCG* enables 'high', V_X begins to be

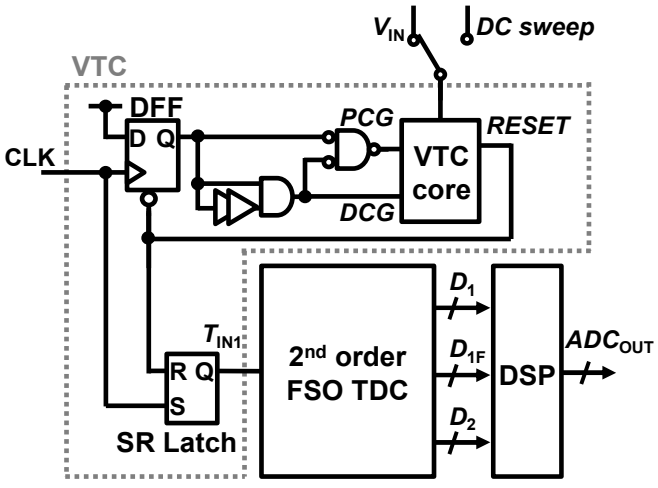

Fig. 5. Proposed I/O-sized ADC architecture.

discharged toward *VSS*; V_X is, however, precharged on the way again by a trigger of *RESET* pulse when V_X crosses V_{TH}. Then, T_{IN1} becomes 'low'. That is, the SR latch generates the output pulse (T_{IN1}: time from the rising edge of *CLK* to the rising edge of *RESET*). The T_{IN1} width is defined by V_{IN}. After the VTC converts V_{IN} to T_{IN1}, the FSO TDC converts T_{IN1} to a digital code using a frequency difference. After converting the digital code, the DSP corrects the nonlinearity and suppresses harmonic noises.

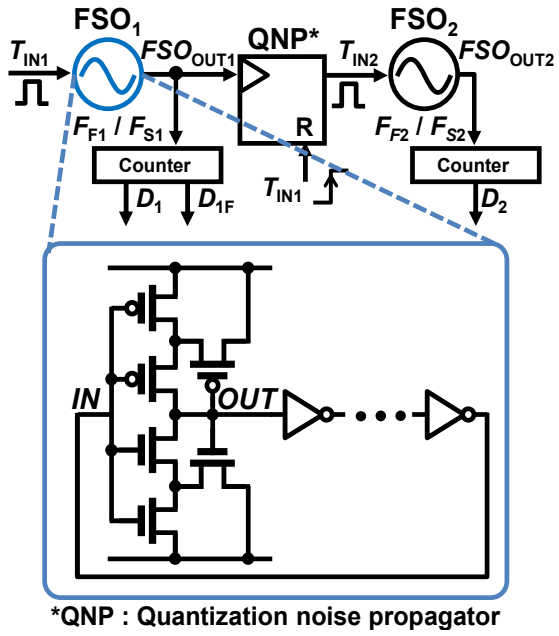

Fig. 6. Schematic of FSO and Schmitt trigger inverter ring.

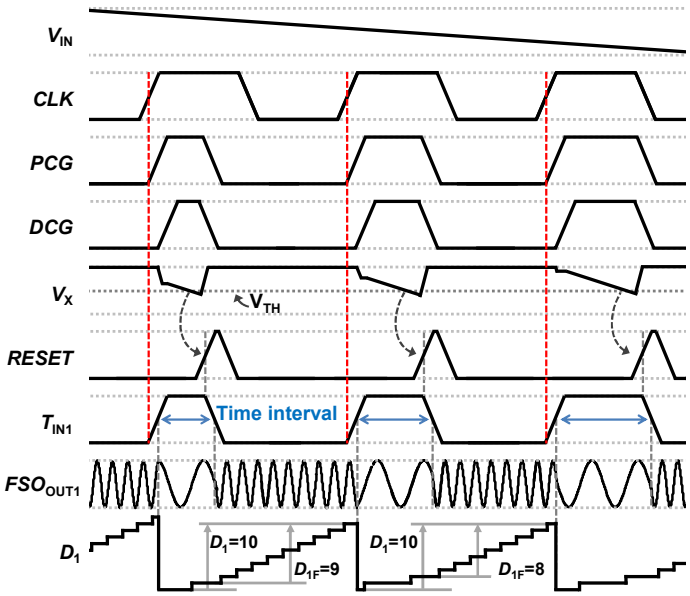

Fig. 7. Proposed ADC operating waveforms.

IV. Measurement Results

Fig. 8 shows the measured output spectra of the proposed ADC. In the spectra, the input signal frequency is 78 kHz at a 20-MHz sampling rate. The original SNDR in Fig. 8(a) is 43 dB at a bandwidth of 500 kHz and the SFDR is 45 dB. The harmonics of ADC are produced by the nonlinearity of the VTC. After making the nonlinearity correction, the SFDR is improved to 58 dB in Fig. 8(b).

A test chip was made using a 65-nm CMOS process (Fig. 9). The VTC occupies 6468 μm^2 as an active area. The MOM capacitance consists of higher metal to put in the FSO TDC under the VTC. The MOM capacitance needs somehow large area; however the ADC needs no additional area without the VTC because the MOM capacitance consists of the higher metals. A digital input I/O in a 65 nm occupies 6800 μm^2. The proposed ADC is 95.1% of the digital I/O, and is useful as an ADC I/O to convert a signal from analog to digital. The total power consumption is 509 µW. The test chip performance is summarized in TABLE I and Fig. 10. Our purpose is the area

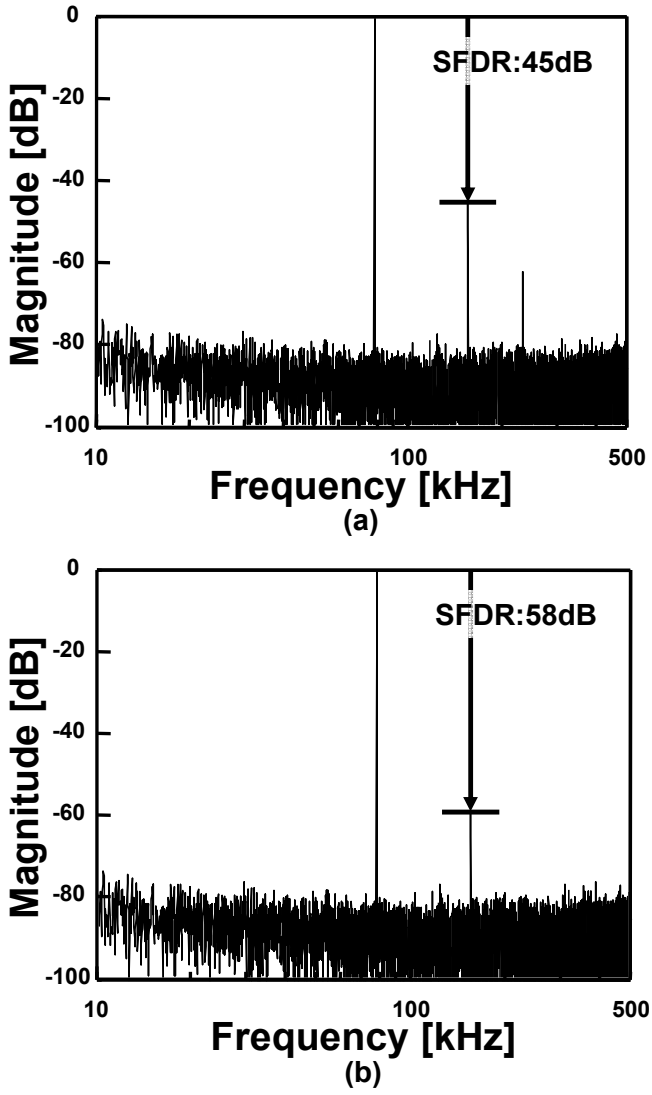

Fig. 8. Output spectra of IO-sized ADC (a) w/o calibration and (b) w/calibration.

reduction of the ADC. Therefore, we compare area-FoMs of other state-of-the-art ADCs [3]. Our proposed ADC exhibits better area-FoM among the near-bandwidth ADCs.

V. SUMMARY

We described a 50-dB I/O-sized second-order ADC. The proposed architecture obviates analog circuits such as opamps and switched capacitors. The proposed ADC thereby maintains scalability with future advanced processes. As process technology advances, the ring oscillator frequency is expected to increase, which will be beneficial for the proposed ADC. A three-order or multiple-order ADC will be possible in our proposed ADC architecture.

ACKNOWLEDGMENT

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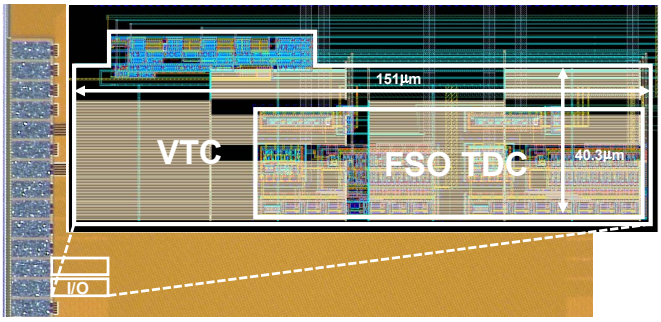

Fig. 9. Micrograph of the proposed ADC chip.

TABLE I.
COMPARISON WITH STATE-OF-THE-ART ADCS

Item	This work		[8]	[9]
Technology (nm)	65		90	40
Band width (kHz)	500		500	550
Sampling rate (MS/s)	20		96	1.1
Power (mW)	VTC	0.228	2.6	0.0012
	TDC	0.281		
	Total	0.509		
SFDR (dB)	58		N/A	N/A
SNDR (dB)	50		76	46.8
ENOB (bits)	8.0		12.3	7.5
Active area (mm^2)	0.0065		0.4	0.012
Power-FoM (fJ/conv.step)*	1970		504	6
Area-FoM (mm^2·ps/conv.step)**	23		78	49

$$*Power-FoM = \frac{Power}{2 \cdot BW \cdot 2^{ENOB}} \quad **Area-FoM = \frac{Area}{2 \cdot BW \cdot 2^{ENOB}}$$

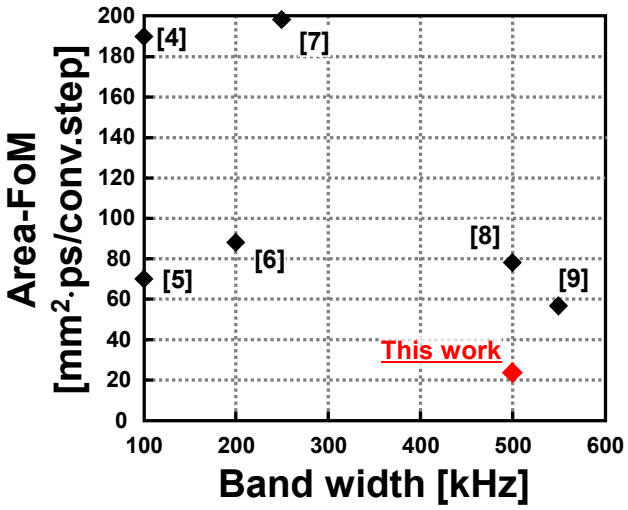

Fig. 10. Comparison with other state-of-the-art ADCs.