A 2.23 ps RMS Jitter 3 μs Fast Settling ADPLL using Temperature Compensation PLL Controller

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***Abstract*— This report describes an all-digital phase-locked loop (ADPLL) with temperature-compensated settling time reduction. The novelty of this work is autonomous oscillation control word estimation without a look-up table or memory circuits. The proposed ADPLL includes a multi-phase oscillator as a digitally controlled oscillator (DCO). Digital timing error correction circuits are integrated to minimize the settling time that is degraded by phase conversion error. The ADPLL is fabricated using a 65 nm CMOS process. The test chip occupies 0.27 × 0.36 mm^2. It achieves 2.23 ps RMS jitter and -224 dB FoM at 2.4 GHz output frequency with 8.85 mW power dissipation. Measurement results show that the 47% settling time is reduced by the proposed estimation block. The average settling time at 25 °C is 3 μs.**

I. INTRODUCTION

Because of their implementation without difficulty, their low power consumption, and their small area, all-digital phase-locked loops (ADPLLs) have attracted attention [1]. We used a digitally controlled oscillator (DCO) because it has a small footprint and low power consumption. An important shortcoming of the ring-oscillator-based ADPLL is that it has larger jitter than one with LC oscillators. A jitter reduction technique using an injection lock has been proposed [2]. In an earlier study [3], the ring oscillator contributes both to power reduction and the settling time reduction.

We specifically examine the settling time of the ADPLL in this report. The settling time of the ADPLL directly affects the system level power consumption in a modern wireless communication application such as a sensor network because the periodical wake-up technique is used to minimize power consumption in these applications [4]. For example, when the system has a very low active ratio (less than 0.1%), a carrier sense operation dissipates the dominant power consumption, although only several bits of data are received in this operation.

In the conventional settling-time reduction method, a foreground calibration block estimates the oscillator tuning word (*OTW*). To estimate the optimum *OTW*, the conventional method calibrates DCO characteristic [5]. However, the settling time lengthens under the temperature variation because the DCO characteristic is changed in another temperature.

Therefore, as described herein, we propose a fast-settling and low-jitter ADPLL using a digital error correction circuit and a digital calibration block to compensate the temperature variation.

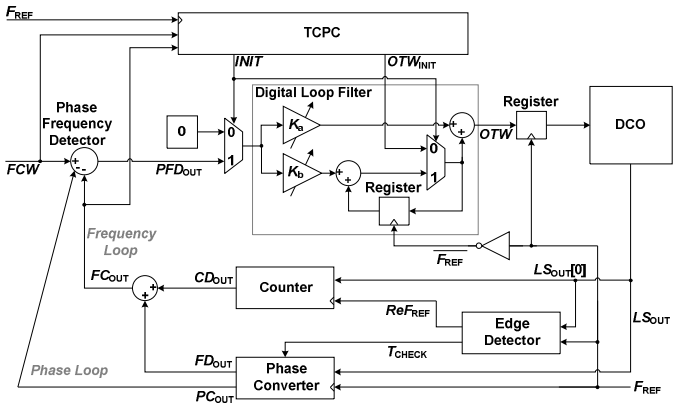

Fig. 1. Block diagram of proposed ADPLL.

II. ADPLL WITH DIGITAL ERROR CORRECTION CIRCUITS

This section introduces the architecture of the ADPLL with the proposed digital timing error correction circuits and the OTW estimation block. Fig. 1 portrays the architecture of the proposed ADPLL, which is based on a divider-less ADPLL architecture [1]. The feedback loop consists of a counter, a phase converter (PC), a phase frequency detector (PFD), a register, and a digital loop filter (DLF).

Our ADPLL uses a multi-phase output oscillator to detect oscillator phase. We choose a multi-phase oscillator (MPOSC) with phase couplers [6]. As presented in Fig. 2, the DCO consists of the MPOSC, a 16-bit-resolution current source circuit, and level shifters (LSs). The LSs contribute to improvement of the phase detection accuracy. The output signals of LSs (LS_{OUT}) are connected to both the counter and the PC. The PFD compares a frequency control word (*FCW*) and the sum of the counter output and the PFD output. The

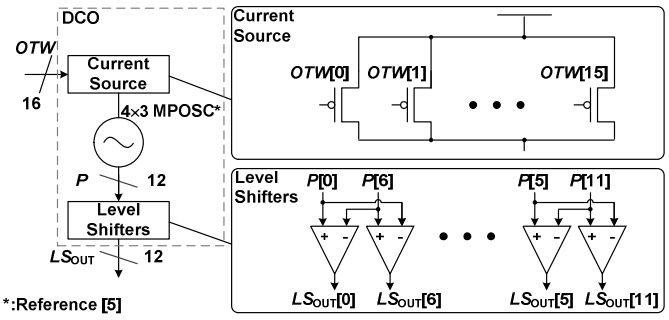

Fig. 2 Block diagram of DCO with MPOSC.

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FCW determines the ADPLL output frequency. A DLF switches the filter gain coefficients dynamically according to the PFD output. The digitized phase and frequency error (PFD_{OUT}) are filtered by the DLF.

The DLF and the PFD operate at the falling edge of the reference clock F_{REF}. Then, the registers in front of DCO latch the OTW from DLF output at the rising edge of F_{REF}. Therefore the setup and hold errors in DFFs are predicted. Although the maximum delay between DFFs with falling edge and DFFs with rising edge is a half cycle of F_{REF}, the critical path in the feedback loop is sufficiently smaller than the maximum delay.

A. Edge Detector

The coarse DCO frequency is detected by the counter. And the PC detects the fine DCO frequency and the phase error. The counter and the PC have a strict timing constraint because the DCO output is connected directly to these circuits. To prevent the timing error, an edge detector (ED) is introduced to generate latch timing and a phase error check signal.

Fig. 3 shows the block diagram and the timing diagram of the ED. The counter output is synchronized by $LS_{OUT}[0]$. It has higher frequency. Unfortunately, the LS_{OUT} and F_{REF} are asynchronous. Therefore, if the counter uses the rising edge of F_{REF}, then the timing error will occur. To eliminate this error, the ED outputs the gated LS_{OUT} clock (ReF_{REF}), which is kept away from the rising edge of F_{REF} as depicted in Fig. 3. The ReF_{REF} is used to latch the counter value without metastability. The ED also outputs a correction signal T_{CHECK}, which is determined by sampling $LS_{OUT}[0]$ at the rising edge of F_{REF} to prevent phase detection errors. The T_{CHECK} is used to determine the range of phase. The phase error is compensated in the PC by T_{CHECK}.

B. Phase Converter

The PC detects the fine frequency and the phase error. In other words, the PC operates as a time-to-digital converter. As

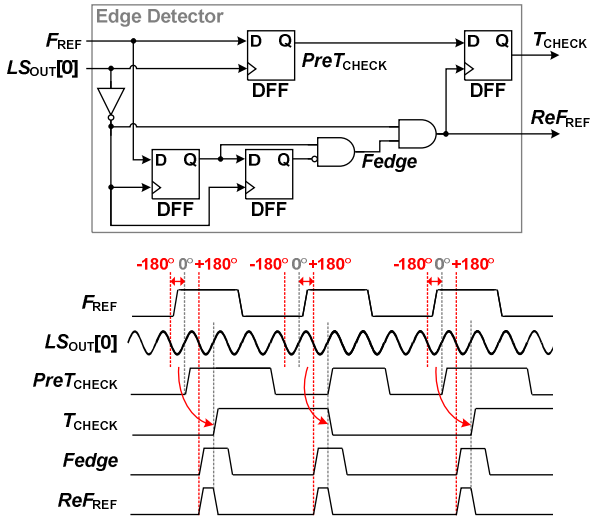

Fig. 3. Architecture and timing diagram of the edge detector (ED).

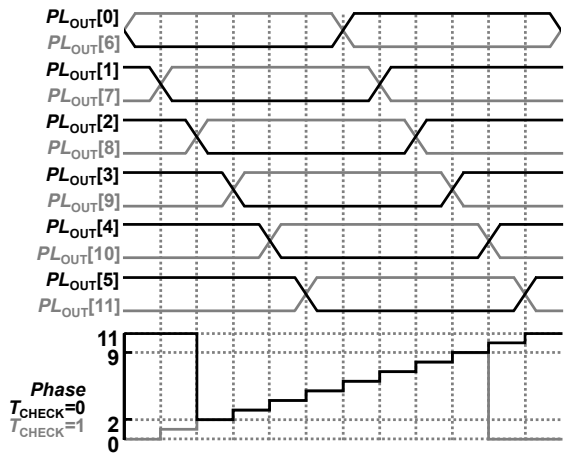

Fig. 4. Timing diagram of the phase converter.

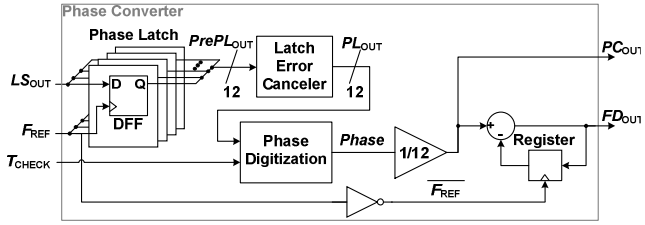

Fig. 5. Block diagram of the phase converter

portrayed in Fig. 4, the PC controls the fine frequency tuning and phase locking by converting the LS_{OUT} to phase data. All DCO output signals are latched by phase latch DFFs at the rising edge of F_{REF}. The DCO outputs and F_{REF} are asynchronous. Therefore, the phase latch output $PrePL_{OUT}$ includes latch errors. The latch error can be canceled by adjusting phase signals in the next block. Next, the corrected signal PL_{OUT} is digitalized to 4-bit signals, called *Phase*. The range of *Phase* depends on the number of the DCO output phases, which is 12 phases in this report. Finally, to eliminate the latch timing error, *Phase* is corrected using T_{CHECK}. T_{CHECK} shows the $LS_{OUT}[0]$ state at the rising edge of F_{REF}. Therefore, the latch error can be determined. The phase digitization corrects the converted data if the value of *Phase* is outside of the phase range. In the same manner of the counter output, the error checker output is latched at the falling edge of F_{REF}.

III. Temperature Compensation PLL Controller

This section presents a description of a settling-time reduction technique using a temperature compensation PLL controller (TCPC). The TCPC uses a digital calibration algorithm based on the temperature characteristic of DCO, and it outputs an optimum *OTW*, called OTW_{EST}. Fig. 6 (a) shows the DCO nonlinearity temperature characteristics of the test chip. Because of this characteristics, the optimum OTW is changed by temperature. Although the DCO frequency is changed by the temperature fluctuation, the normalized frequency is almost identical to that depicted in Fig. 6 (b). Therefore, the relationship between *OTW* and output frequency can always be estimated from one-time calibration.

In this work, we defined the DCO frequency model formula by a rational approximation using this normalized frequency. The model formula is

$$NF = OTNF(OTW) = \frac{a \cdot OTW + b}{c \cdot OTW + d}. \quad (1)$$

Here, *a, b, c,* and *d* are constants. In the test chip, the calculated constraints *a, b, c,* and *d* in (1) are 1.11, 2.613, 1.0, and 31.27, respectively. *NF* denotes the normalized frequency. *OTNF* is the OTW-to-normalized frequency function. Using this *NF* from (1), the estimation accuracy is unaffected by temperature fluctuation. In the system level, the constraints *a*, *b*, *c*, and *d* should be calculated in the calibration at first time of use. Then, the counter and phase converter are used as TDC.

Next, we present an optimum *OTW* estimation algorithm, as presented in Fig. 7. To estimate OTW_{EST}, the estimation algorithm requires the previous locked *OTW*, OTW_{LOCK}, and the previous frequency code, FC_{OUT}. From (1), the previous *NF*, NF_{LOCK}, is expressed as

$$NF_{LOCK} = \frac{a \cdot OTW_{LOCK} + b}{c \cdot OTW_{LOCK} + d}. \quad (2)$$

NF_{LOCK} is directly proportionate to FC_{OUT} because the FC_{OUT} expresses the DCO output frequency. The target normalized frequency, NF_{EST}, is also directly proportionate to *FCW*. Therefore, the ratio of NF_{LOCK} to NF_{EST} is given as

$$NF_{LOCK} : NF_{EST} = FC_{OUT} : FCW. \quad (3)$$

From (3), NF_{EST} can be derived as (4)

$$NF_{EST} = \frac{FCW}{FC_{OUT}} \cdot NF_{LOCK}. \quad (4)$$

The OTW_{EST} is calculable using the inverse function of (2), $OTNF^{-1}$. Therefore, the OTW_{EST} is represented as

$$OTW_{EST} = OTNF^{-1}(NF_{EST}) = \frac{d \cdot NF_{EST} - b}{-c \cdot NF_{EST} + a}. \quad (5)$$

Eventually, from (3), (5) and (6), the OTW_{EST} can be given as

$$OTW_{EST} = \frac{d \cdot FCW \cdot A - b \cdot FC_{OUT} \cdot B}{-c \cdot FCW \cdot A + a \cdot FC_{OUT} \cdot B}, \quad (6)$$

where *A* is $a \cdot OTW_{LOCK} + b$, and *B* is $c \cdot OTW_{LOCK} + d$.

The block diagram of TCPC is presented in Fig. 8. The TCPC inputs are *FCW*, FC_{OUT}, and *OTW*. The TCPC outputs two control signals, the OTW_{INIT} to control the DCO frequency directly and the *INIT* to switch the ADPLL operation. An estimation block in the TCPC calculates (6). The outputs of a TCPC controller $FLAG_{OTW}$ and $FLAG_{EST}$ respectively control the output signals and the estimation block.

Fig. 9 portrays a timing diagram of the TCPC operation. When *FCW* is changed, a TCPC controller makes $FLAG_{EST}$ to calculate OTW_{EST}. The OTW_{EST} calculation process takes two reference cycles. After the calculation, $FLAG_{OTW}$ becomes high to output OTW_{EST}. The total cycles of the TCPC correction are seven cycles. Whenever *FCW* is changed, this estimation operation is repeated. The settling time is reduced in any case.

IV. Measurement Result

The test chip is fabricated in a 65 nm CMOS process. Fig.

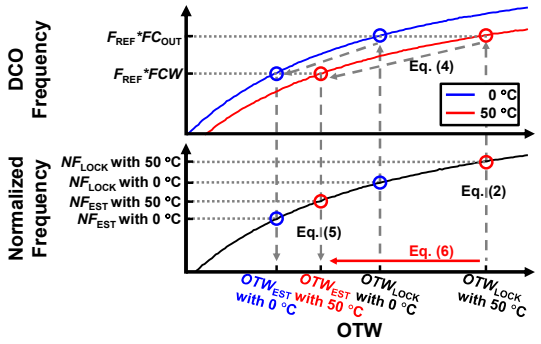

Fig. 7. TCPC algorithm to estimate an optimum OTW.

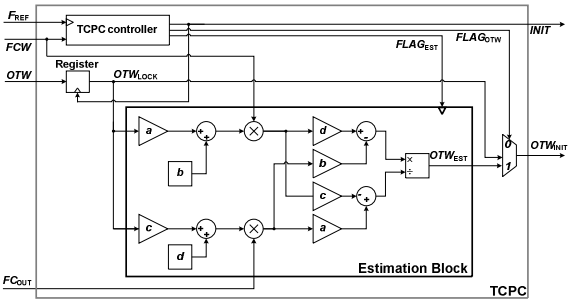

Fig. 8. Block diagram of a TCPC.

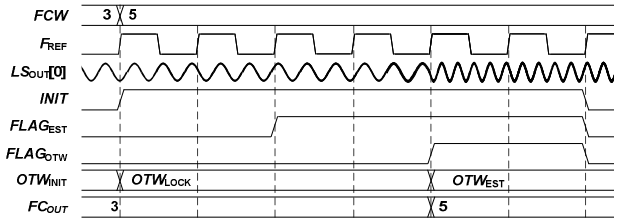

Fig. 9. Timing diagram of a TCPC block.

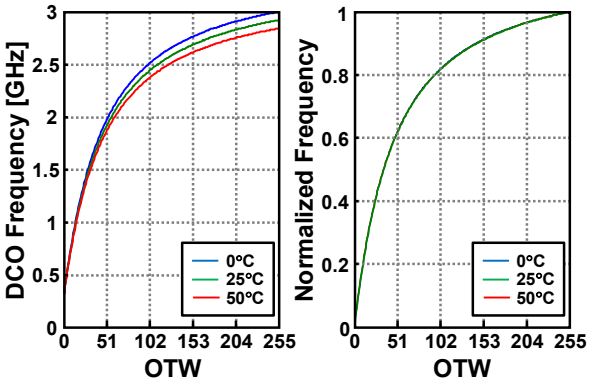

Fig. 6. Temperature characteristics of normalized DCO frequency.

10 exhibits a microphotograph and a layout plot. The total power consumption is 8.85 mW. Then, the DCO and LSs consume 2.48 mW and other circuits consume 6.37 mW. In this evaluation, the TCPC block is implemented using an FPGA. The estimated area and power estimations of the TCPC are 0.2×0.1 mm^2 and 813 µW in a 65-nm process.

Fig. 11 presents a measurement result of the frequency transient with 15 MHz F_{REF}. As presented in Fig. 12, although the *FCW* is changed continuously, the TCPC can maintain a fast settling time. The blue line represents the average of five samples. The grey area shows the standard deviation. The settling time of the ADPLL with the TCPC is 3 µs (45 cycles)

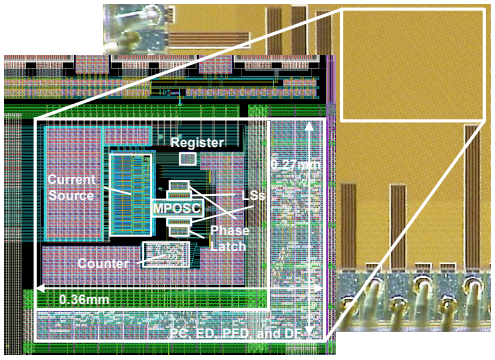

Fig. 10. Chip micrograph and layout of the proposed 65 nm ADPLL.

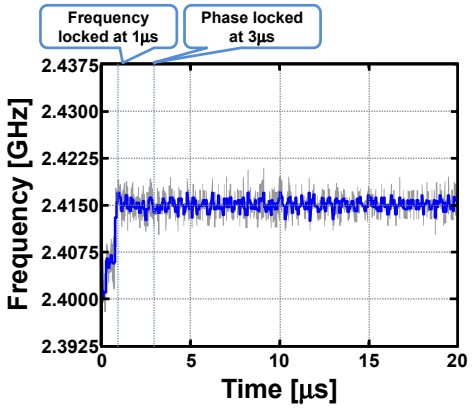

Fig. 11. Measurement results of settling time at 25 °C.

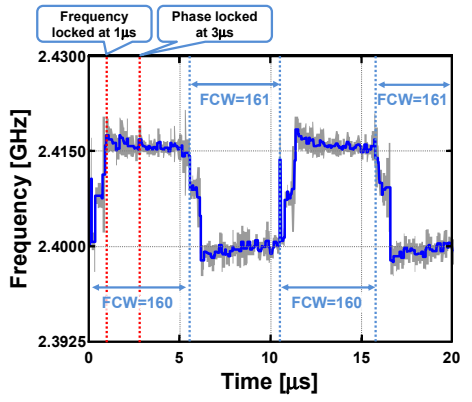

Fig. 12. Measurement results of settling time with continuous FCW change.

when the *FCW* is changed from 2.4 GHz to 2.415 GHz at 25 °C. As presented in Fig. 12, although the *FCW* is changed continuously, the TCPC can maintain a fast settling time. TABLE I presents settling times at several temperatures. At least 47% settling time is reduced by the TCPC. The measured RMS jitter is 2.23 ps and the phase noise is -71 dBc/Hz at 100 kHz offset frequency. The figure of merit (FoM) is -224 dB at 2.4 GHz output frequency. TABLE II presents a performance comparison with previously published fast settling ADPLLs using a ring-oscillator DCO. This work presents the best settling time and FoM.

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TABLE I. SETTLING TIME COMPARISON

	Settling time [µs]		Reduction[%]
Temp.[°C]	w/ TCPC	w/o TCPC	
10	3.13	5.86	47
20	3.33	6.60	50
25	3.00	7.33	59
30	3.33	7.40	55
40	3.40	7.87	57
50	3.53	7.87	55

TABLE II. PERFORMANCE SUMMARY AND COMPARISON

	This work	[2]	[3]	[7]
Process [nm]	65	65	22	180
Ref. Freq. [MHz]	20	32	100	5
Freq. range[GHz]	1.50-2.80	N/A	0.3-3.20	2.39-2.65
Carrier Freq. [GHz]	2.40	0.58	3.20	2.49
Area [mm^2]	0.0972	0.1600	0.0170	1.7810
Settling time [µs]	3.0	N/A	<3.0	5.0
RMS Jitter [ps]	2.23	4.23	6.00	1.92
Power [mW]	8.85	10.50	3.40	18.60
FoM* [dB]	-224	-217	-219	-221

$* \; FoM = 10\log[(Jitter/1s)^2 \cdot (Power/1mW)]$