Multiple-Bit-Upset and Single-Bit-Upset Resilient 8T SRAM Bitcell Layout with Divided Wordline Structure

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***Abstract*—This paper presents a new 8T (8-transistor) SRAM cell layout mitigating multiple-bit upset (MBU) in a divided wordline structure. Because bitlines along unselected columns are not activated, the divided wordline structure eliminates a half-select problem and achieves low-power operation, which is often preferred for low-power / low-voltage applications. However, the conventional 8T SRAM with the divided wordline structure engenders MBUs because all bits in the same word are physically adjoining. Consequently, error correction coding (ECC) techniques are difficult to apply. This paper presents a new 8T cell layout pattern that separates internal latches in SRAM cells using both an n-well and a p-substrate. We investigated an SEU cross section of nMOS that is 3.5–4.5 times higher than that of pMOS. Using an iRoC TFIT simulator, we confirmed that the proposed 8T cell has better neutron-induced MBU tolerance. The MBU in the proposed 8T SRAM is improved by 90.70% and the MBU soft error rate (SER) is decreased to 3.46 FIT at 0.9 V when ECC is implemented. Additionally, we conducted Synopsys 3-D TCAD simulation, which indicates that the LET threshold (LETth) in single-event upset (SEU) is also improved by 66.47% in the proposed 8T SRAM by a common-mode effect.**

***Index Terms*—SRAM, soft error, multiple-bit upset (MBU), single-event upset (SEU), error correction coding (ECC), alpha particle, neutron particle**

I. Introduction

The minimum feature size in transistors continues to decrease with the advance of process technology. Process scaling realizes higher density and lower cost. In a deep sub-micron era, the threshold voltage (Vt) deviation in transistors is nevertheless increasing to more than 100 mV as $3\sigma_{Vt}$ [1–2]. Consequently, designing a 6T SRAM cell, presented in Fig. 1, has become increasingly difficult: both read and write margins must be considered [3]. The 8T SRAM cell presented in Fig. 2(a) was proposed to eliminate read failures caused by the dedicated read port (comprising NRA and NRD). Therefore, in the 8T cell, only the write margin must be considered, which can make the layout smaller and less expensive than that of 6T cell in future processes [4].

Figs. 3(a) and 3(b) portray a general bit-interleaving SRAM structure and a divided wordline structure [5]. In write operations in the general structure, all access gates (NA0 and NA1 in Fig. 2) from one end's cell to the other are activated. Then selected BLs are discharged or charged by write drivers. Consequently, the other BLs, which are unselected, incur the half-select problem [6] and consume large amounts of active power. The general structure includes disadvantages related to low-power and low-voltage operation.

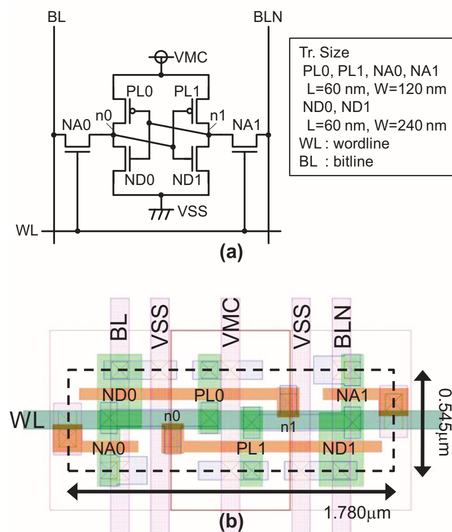

Fig. 1. (a) Schematic and (b) layout of a 6T cell in 65-nm CMOS process (logic rule basis).

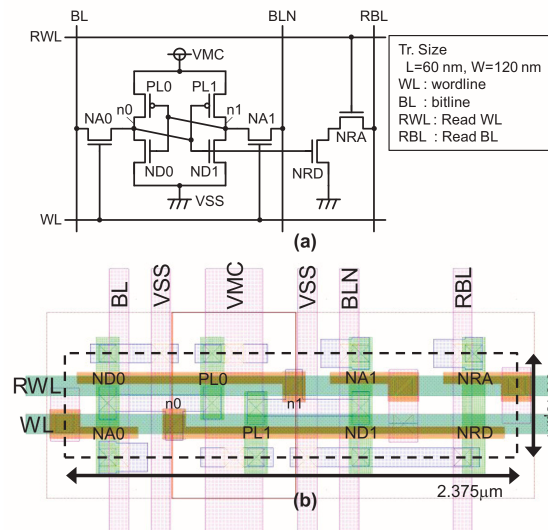

Fig. 2. (a) Schematic and (b) layout of conventional 8T cell in 65-nm CMOS process (logic rule basis).

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The divided wordline structure separates one word from others, and a large multiplexer (MUX) outputs a selected word. Only the BLs in the selected columns are only discharged, which can obviate the half-select problem and achieve low power operation. However, a conventional 8T SRAM with a divided wordline structure retains the MBU problem in a word. Fig. 3(c) presents the conventional 8T cell layout and alignment pattern. The conventional bilaterally symmetric allocation produces two adjacent latches (Latch-0 and Latch-1). Therefore, two-bit upset in the horizontal direction can easily occur from a heavy-ion strike. Furthermore, the two adjoining nodes (n00 and n10) are n-diffusions, for which the critical linear energy transfer (LET_{crit}) is a quarter or less than that of p-diffusion [7]; avoiding the MBU in a word is difficult in a conventional 8T cell.

As described herein, we propose a novel MBU-tolerant 8T SRAM cell layout and its alignment pattern. As presented in Fig. 4, a pMOS (PL0), nMOSes (ND0, NA0, ND1, NA1), pMOS (PL1), and nMOSes (NRA and NRD) form p-n-p-n diffusions. The internal latches are separated and not adjoining. The sensitive nMOSes (ND0 and ND1) are adjacent in a single cell, thereby, enhancement of a SER tolerance can be expected using a common-mode effect [8]. Results show that the proposed 8T cell layout achieves MBU tolerance, even in the divided wordline structure.

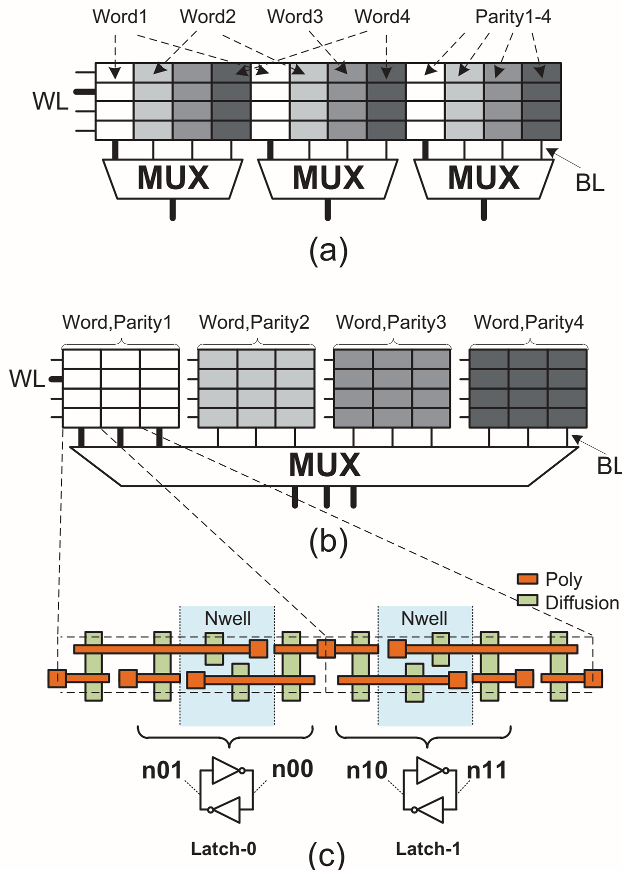

Fig. 3. (a) General structure, (b) divided wordline structure, and (c) conventional 8T SRAM cell layout pattern. ECC requires extra parity bits.

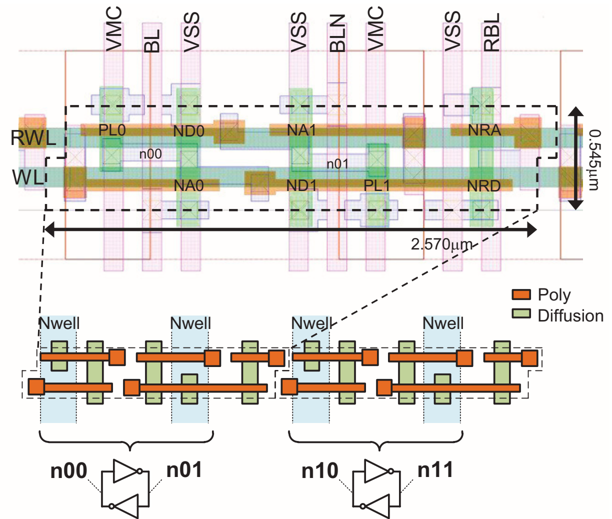

Fig. 4. Proposed 8T cell layout and alignment pattern.

II. Soft-Error Simulation Results

A. TFIT simulation

For simulating soft errors caused by heavy ions and neutrons on semiconductor devices, iRoC TFIT is an useful tool [9]. Fig. 5 presents the TFIT simulation flow diagram. In reality, TFIT has a database of disturb currents and soft-error behaviors extracted from the Synopsys TCAD simulator, which is fitted to measurement data. In the TFIT simulation flow, we used a 65-nm generic CMOS database and a 65-nm PTM model for SPICE simulations.

Figs. 6 and 7 respectively present SEU cross sections of nMOSes (ND1 = ND2 = ND and NA1 = NA2 = NA) and pMOS (PL1 = PL2 = PL) in a latch. The cross section is defined by an area in which a heavy ion strikes and a cell is flipped. The LET of a heavy ion was varied from 10 to 90 fC/μm. The cross section area was set from the center of the drain diffusion. We observed that the cross sections at 0.9 V are 70–75% larger than at 1.3 V. Fig. 8 presents that the SEU cross section ratios of nMOS to pMOS are 3.5–4.5. The proposed cell layout has nMOSes in the middle and because the sensitive n-diffusions are separated in two adjoining cells. Therefore, it can decrease the horizontal MBUs.

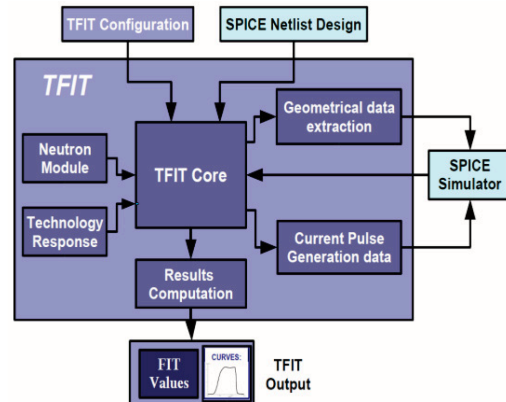

Fig. 5. TFIT simulation flow diagram [9].

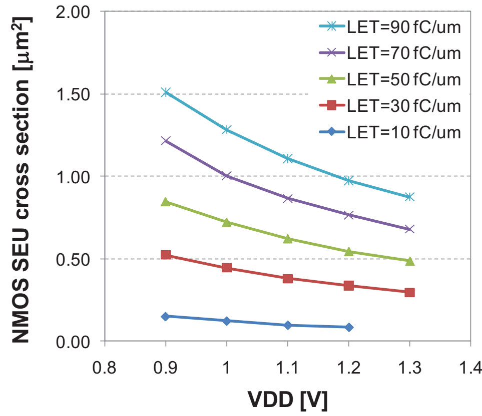

Fig. 6. SEU cross section in nMOSes (shared drain diffusion of ND and NA).

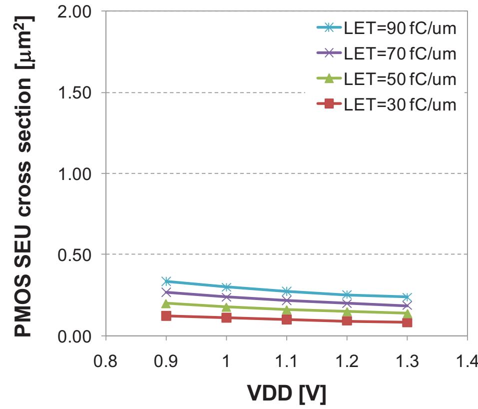

Fig. 7. SEU cross section in pMOS (drain diffusion of PL).

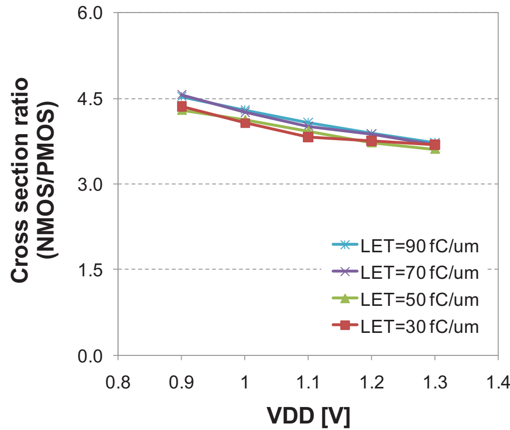

Fig. 8. Cross section ratio of nMOS to pMOS.

We also investigated neutron-induced MBU SER considering both horizontal and vertical directions, and compared the conventional and proposed 8T layout patterns. The TFIT has a neutron-induced SER database fitted to sea level in New York. The SRAM data pattern was set as random and the memory capacity was assumed as 1 Mb. Fig. 9 portrays the MBU FIT and the error patterns in the conventional 8T cell at 0.9 V. The MBUs in the vertical direction can be corrected by ECC, but the two-bit or more upsets in the horizontal direction are not, which might cause important problems such as system failure.

TABLE I
NEUTRON-INDUCED MBU AT 0.9-1.3 V

Type	VDD [V]	w/o ECC [FIT]	w/ ECC [FIT]	MBU Reduction
Conv. 8T	0.9	111.92	37.20	-66.76%
	1.0	85.87	27.85	-67.56%
	1.1	64.68	20.77	-67.89%
	1.2	43.79	13.60	-68.95%
	1.3	37.12	11.50	-69.02%
Prop. 8T	0.9	92.78	3.46	-96.27%
	1.0	68.49	2.57	-96.24%
	1.1	50.04	1.82	-96.36%
	1.2	32.68	1.06	-96.74%
	1.3	26.79	0.85	-96.81%

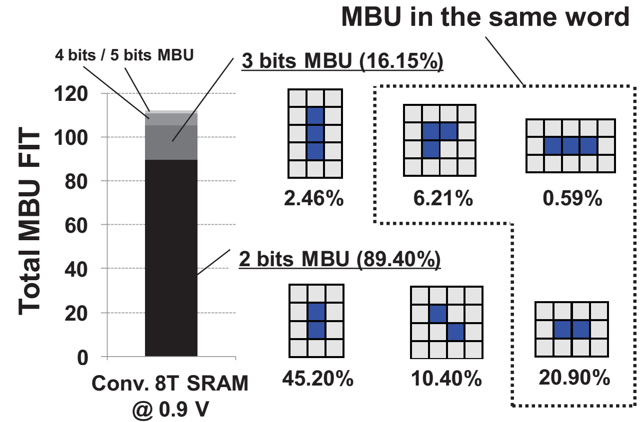

Fig. 9. MBU pattern in conventional 8T SRAM at 0.9 V.

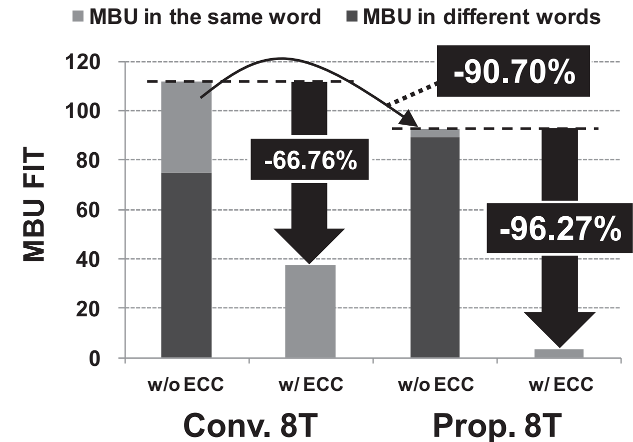

Fig. 10. Neutron-induced MBU improvement at 0.9 V in a divided wordline structure: conventional and proposed 8T SRAMs.

TABLE I presents neutron simulation results obtained at 0.9–1.3 V. Fig. 10 shows that, in the divided wordline structure with the conventional 8T cell, the MBU reduction by ECC is 66.76% at 0.9 V. It is 96.27% in the proposed 8T cell because the internal latches are separated by the n-well and p-substrate. The MBU in the same word is improved by 90.70%. The MBU SER is calculated as 3.46 FIT in ECC.

B. Synopsys 3-D TCAD simulation

We investigated an SEU tolerance in the proposed 8T SRAM layout using Synopsys 3-D TCAD simulation [10].

The proposed 8T cell has two internal nodes (N1 and N0) of nMOSes (ND and NA) in the middle. The distance between the nodes is 0.46 μm. When a heavy ion strikes an area around them, these nodes are pulled down; in this case, the SEU tolerance is expected to be improved because of the common-mode effect. However, the conventional 8T cell has nMOSes separated by n-wells and has no common-mode effect. In this simulation, two nMOSes (ND0 and ND1) in the proposed 8T cell and one nMOS (ND1) in the conventional 8T cell were made with 65-nm 3-D device models [11]. The other transistors were based on the PTM 65-nm SPICE model. The gate length and width of the nMOS were set respectively to 60 nm and 120 nm.

Fig. 11 portrays a cross section of an nMOS: Fig. 11(a) shows the case of the conventional 8T cell, Fig. 11(b) shows the proposed 8T cell case. The heavy ion strike occurs at 0.23 μm, which is distant from the edge of the drain node. Fig. 12 presents internal waveforms. The conventional 8T cell was flipped by the impact, although the proposed 8T cell is not flipped by the common-mode effect. Fig. 13 shows an LET threshold (LETth) improvement in the proposed 8T SRAM cell at 0.9 V. The common-mode effect enhances LETth from 1.360 MeV to 2.264 MeV (+66.47%).

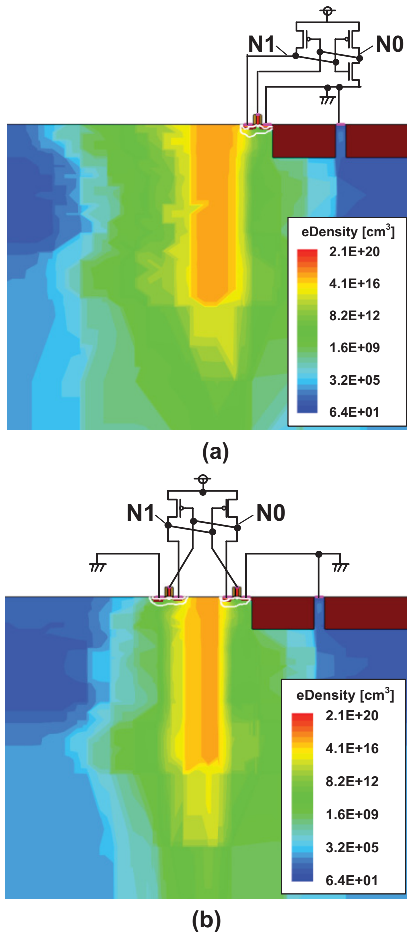

Fig. 11. Cross sections of nMOS in (a) conventional and (b) proposed 8T cells. The LET of the heavy ion is 5.49 MeV.

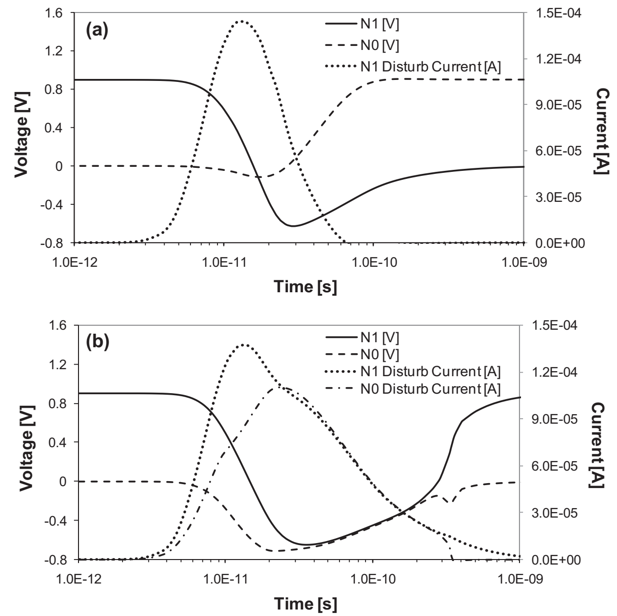

Fig. 12. Waveforms of internal nodes' (N1 and N0) voltages and disturb currents in (a) conventional and (b) proposed 8T cells.

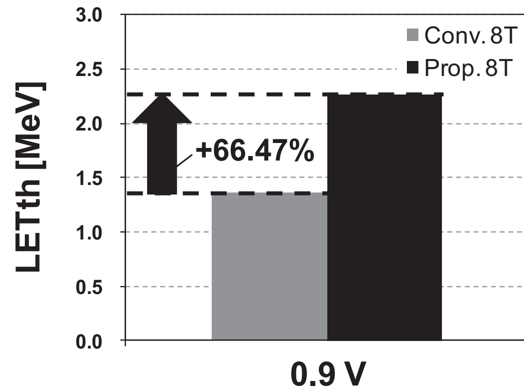

Fig. 13. LETth improvement at a supply voltage of 0.9 V.

III. Area and Power Comparisons

A. Area comparison

The proposed 8T SRAM layout has an area overhead because of its p-n-p-n diffusion. In addition, the divided wordline structure requires an extra AND gate for each word. In this subsection, we mention the overheads in the proposed layout.

TABLE II
SRAM Array features

	Conv. 6T SRAM	Conv. 8T SRAM	Prop. 8T SRAM
Cell area [μm^2] *(ratio to 6T)*	0.9701/cell (× 1.00)	1.294/cell (× 1.33)	1.401/cell (× 1.44)
Array style	Bit interleaving	Divided WL	Divided WL
Configuration	B bits/word × 8 words/row × 256 cells/bitline		
ECC	1-bit correction		

TABLE II shows a cell area comparison (a conventional 6T cell, a conventional 8T cell, and the proposed 8T cell). The cells are all designed in a 65-nm CMOS logic rule, as illustrated in Figs. 1, 2, and 4. The conventional and the proposed 8T cell respectively exhibit cell area overhead values that are 33.43% and 44.38% greater than that of the conventional 6T cell.

Fig. 14 shows area overhead on an SRAM macro level for different bits/word ratios (B in TABLE II). The conventional 6T SRAM macro has the bit-interleaving structure. The conventional and the proposed 8T SRAM macro have a divided wordline structure. The cell arrays consist of eight words/row and 256 cells/bitline. The SRAM macros are equipped with 1-bit correcting ECC. The word width (B) increases concomitantly with decreased array area overheads. The proposed 8T SRAM is 48.45% larger than the conventional 6T SRAM when using 64 bits/word.

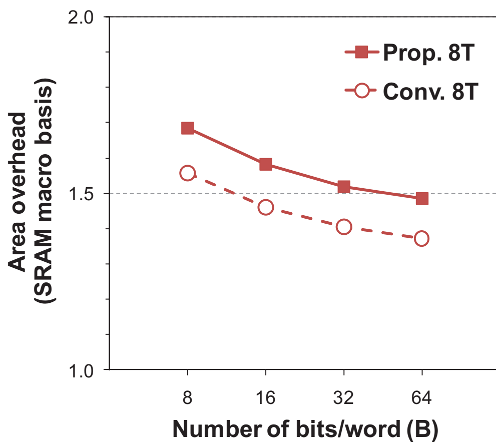

Fig. 14. Area overhead on an SRAM array level for various numbers of bits/word (B in TABLE II).

B. Power comparison

The proposed 8T SRAM layout presents disadvantages in terms of the area overhead. However, it improves the minimum operating voltage.

Fig. 15 portrays bit error rates (BERs) in the 6T SRAM and the proposed 8T SRAM for the worst-case conditions (FS corner and 125°C). A static noise margin (SNM) is used as a metric to evaluate the BERs [12]. The proposed 8T SRAM can eliminate the half-select problem. Therefore, the minimum operating voltage is reduced from 0.88 V to 0.43 V (0.45-V improvement). The minimum operation voltage is defined at a BER of 10^{-6}.

Fig. 16 presents operating powers in the conventional 6T SRAM and the proposed 8T SRAM (when read/write = 50/50 and the power worst corner: the FF corner and 125°C). The memory capacity is 1 Mb, and the clock cycle is set to 10 MHz. Although the proposed 8T SRAM consumes extra power because of its single-ended read port, the operating voltage can be decreased. The power is therefore improved by 77.21%. Consequently, the proposed 8T SRAM achieves low-voltage and low-power operation.

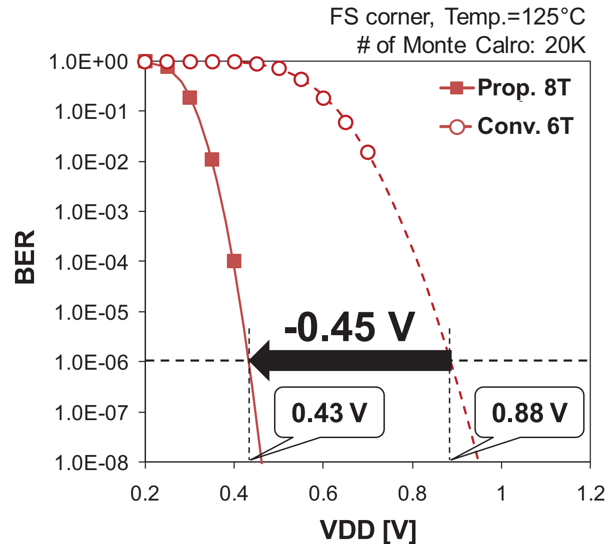

Fig. 15. Bit error rates (BER) in the proposed 8T SRAM and the conventional 6T SRAM. The minimum operation voltage is defined at a BER of 10^{-6}.

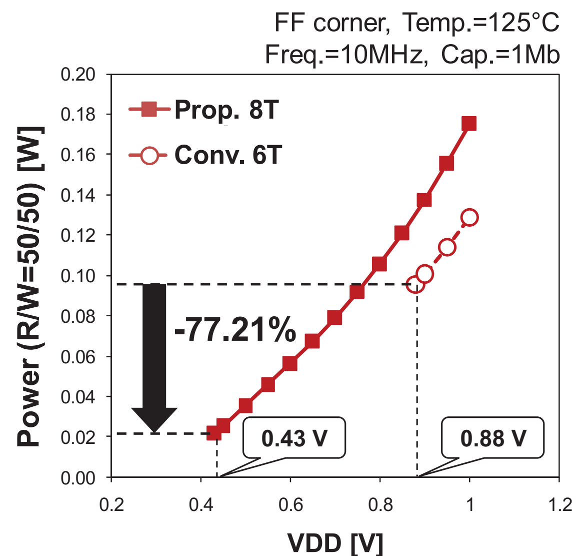

Fig. 16. Operating powers in (a) the conventional 6T SRAM and (b) the proposed 8T SRAM.

IV. Conclusion

We proposed an MBU-tolerant 8T SRAM cell layout with the divided wordline structure. The proposed layout improves MBU in the divided wordline by 90.70%. Moreover, the MBU SER is decreased to 3.46 FIT at a supply voltage of 0.9 V. TCAD simulation of results revealed that the proposed 8T cell layout improves LETth by 66.47% because of the common-mode effect. The proposed 8T SRAM array has 48.38% greater area overhead compared to the conventional 6T SRAM. However, the minimum operation voltage can be improved by 0.45 V. Therefore, the operation power is decreased by 77.21%. Results show that the proposed 8T cell layout enhances soft-error reliability in the divided wordline structure and that it can achieve low-power and low-voltage operation.

Acknowledgments

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