A 6T-4C Shadow Memory using Plate Line and Word Line Boosting

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***Abstract*—This report describes a high speed 6T-4C shadow memory design using a word line boosting and a plate line driver boosting. The proposed methods utilize a characteristic of ferroelectric capacitor. The word line and the plate line boosting method respectively reduce 21% write time and 33% plate line charging time.**

Keywords—Nonvolatile memory, FeRAM, Shadow memory, High-speed

I. INTRODUCTION

Presently, the non-volatile memory is employed in a system-on-a-chip (SoC) for a lot of applications, such as sensor network, biomedical monitoring, and so on. The common characteristics of these applications are extremely low active ratio. Therefore, the non-volatile memory is suitable because these applications have a strict constraint in its stand-by power consumption to reduce the battery capacity and the size of system module. If a volatile memory (e.g. SRAM: Static Random Access Memory) is used as a data buffer in these applications, the leakage current will be a critical portion in the total power consumption of system

In this research, we focus on Ferroelectric Random Access Memory (FeRAM), which utilizes a ferroelectric capacitor as non-volatile element [1-3]. The benefits of FeRAM are low voltage operation and low power consumption operation [4, 5]. The FeRAM is put into practical use (e.g. noncontact IC card). Its availability is also an advantage compared with other advanced non-volatile memory.

Unfortunately, the non-volatile memory has disadvantages in operating speed, active power, and endurance [6]. To mitigate this problem, a 6T-4C shadow memory has been proposed [7, 8]. At read and write operation, the 6T-4C memory act as 6T SRAM to improve the operating speed and active power. While stand-by state, its data are stored to ferroelectric capacitors. Then the power supply to memory cells can be cut off. In this research, we propose write and plate line charging speed boosting techniques using ferroelectric capacitor (see Fig. 1). The proposed boosting techniques also contribute to system level power reduction because operating speed directly affects the active time.

Research supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy an Industrial Technology Development Organization (NEDO).

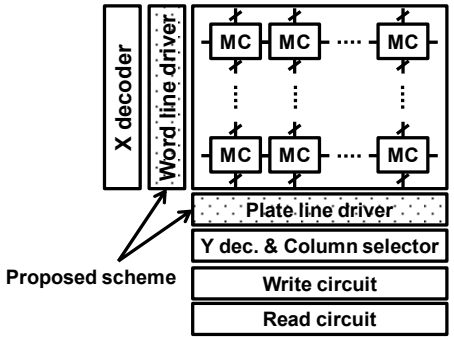

Fig. 1. Block diagram of 6T-4C shadow memory (MC: memory cell).

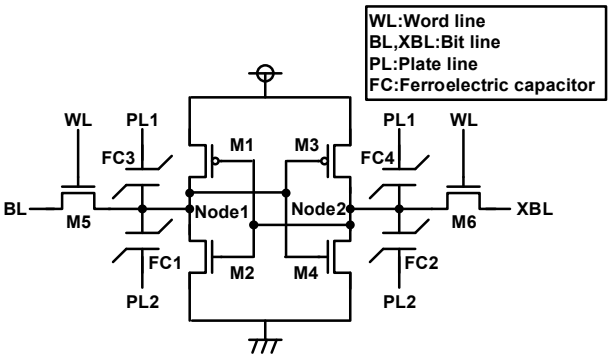

Fig. 2. Schematic of 6T-4C shadow memory cell

II. 6T-4C SHADOW MEMORY

Figure 2 shows the schematic of 6T-4C shadow memory cell. The memory cell consists of drive transistors (M2, M4), load transistors (M1, M3), access transistors (M5, M6), and ferroelectric capacitors (FC1-4). Internal nodes 1 and 2 are storage nodes of the flip-flop to store logical data "0" or "1". A pair of bit lines (BL, XBL) is connect to access transistor as I/O port. The two access transistors are also connected to a word line (WL). Two plate lines (PL1, PL2) are connected to ferroelectric capacitors to control direction of polarization.

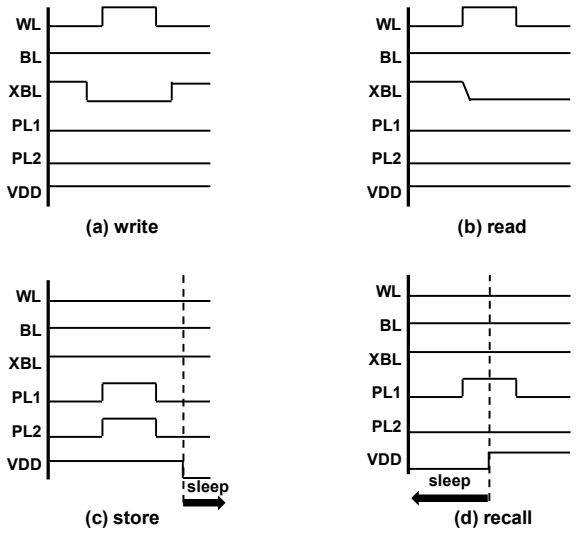

Fig. 3. Timing diagram of write, read, store, and recall operations.

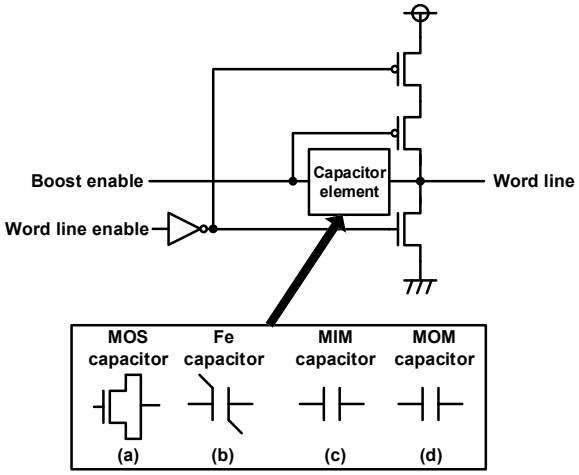

Fig. 4. Schematic of word line driver with boosting capacitor.

Figure 3 shows the timing diagram of 6T-4C shadow memory. Read and write operations are the same as 6T SRAM. The store operation, which transfers the data from internal nodes to ferroelectric capacitors, is required before cutting off the power supply of memory cells. The recall operation restores the internal nodes to previously stored condition.

III. PROPOSED METHODS

A. *Word line boosting*

The 6T-4C shadow memory has a write time overhead compared with 6T SRAM because four ferroelectric capacitors are connected to the internal nodes. To improve write latency, we employed the word line boosting technique, which has been proposed for SRAM [9, 10]. Figure 4 shows word line boosting circuit. Generally, a MOS capacitor is used as a capacitor element.

TABLE I. AREA COMPARISON OF WORD LINE DRIVER.

	Area of WL driver [um^2]	Area of 16Kb memory [um^2]
w/o capacitor	20.1	213202
Fe capacitor	20.2	213215
MOS capacitor	31.3	214636
MIM capacitor	112.1	224978
MOM capacitor	151.1	229970

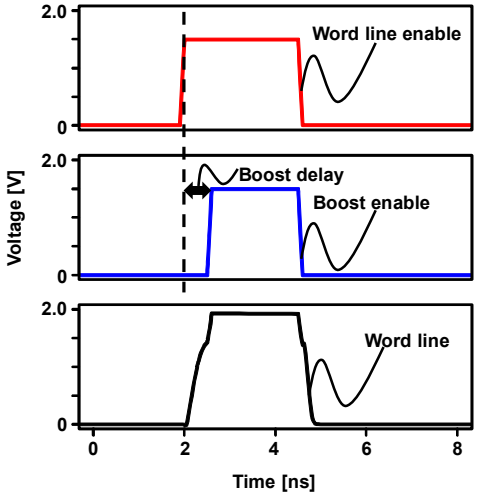

Fig. 5. Waveforms of word line boosting.

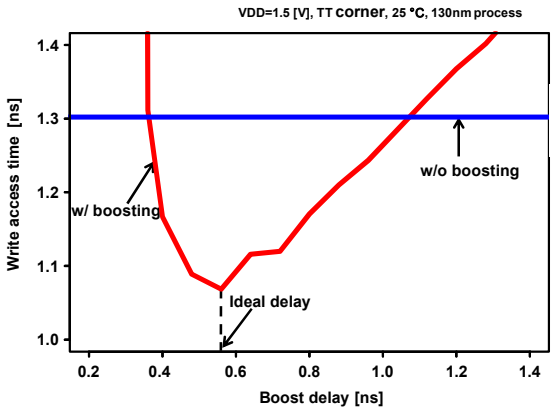

Fig. 6. Boost delay versus write access time.

In our design, the ferroelectric capacitor is used instead of MOS, Metal-Insulator-Metal (MIM), and Metal-Oxide-Metal (MOM) capacitors because it has larger capacitance in same occupied area. TABLE I shows the circuit area comparison of word line driver and 16-Kbit memory macro block.

Figure 5 shows the waveform of write operation using word line boosting. First, the word line enable is charged to drive word line. When word line is reached to nominal voltage, the boost enable will be charged and word line will be boosted.

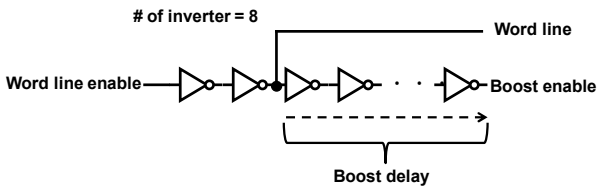

Fig. 7. Boost timing generator using inverter chain.

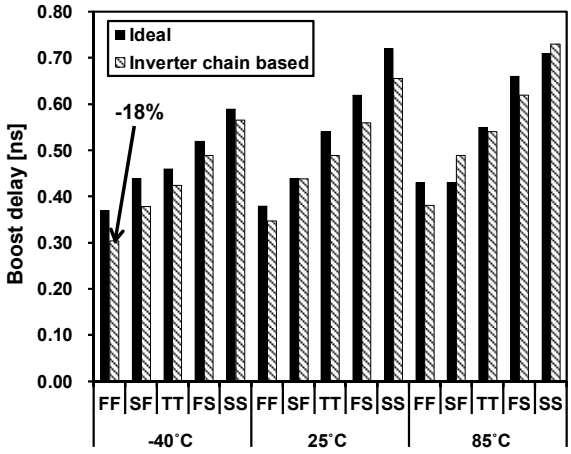

Fig. 8. Simulation results of inverter chain.

The boost delay, which is the time duration between the rising edges of word line enable and boost enable, affect the write access time as shown in Fig. 6. Unfortunately, the ideal length of boost delay is depends on the process variation. To minimize the write access time at any process corner, we designed adoptive timing generator using inverter chain (see Fig. 7). The delay of inverter chain is adjusted to ideal boost delay at TT corner with room temperature. As shown in Fig. 8, the delays of inverter chain much the same as ideal boost delay at any process corner. The maximum mismatch between ideal and inverter chain delays is 18% at FF corner with -40 °C.

B. Plate line driver boosting

The 6T-4C shadow memory requires store and recall operations before cutting off and power on. The plate lines are charged by plate line driver in these operations. However, driving plate lines takes a long time because ferroelectric capacitors, which are connected to plate line, have large capacitance. To reduce the plate line charging time, we propose the boosting technique using ferroelectric capacitor. Figure 9 shows the proposed plate line driver circuit.

Figure 10 explain the waveform of plate line charging using plate line driver boosting for store and recall operations. At first, the plate line enable is charged to drive plate line. Next, the boost enable is charged when boosting node is reached 0V. Then, the on-state current of plate line driving transistor will be increased because the voltage of boosting node will be negative voltage. Therefore the charge time of plate line can be improved.

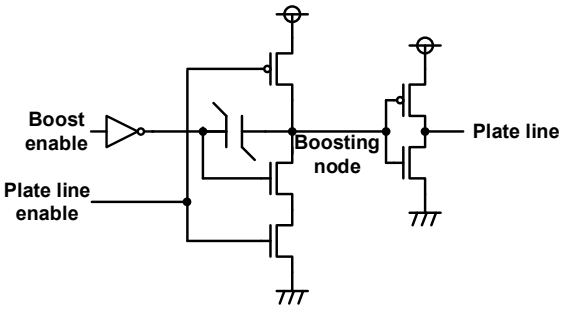

Fig. 9. Schematic of plate line driver with capacitor boosting.

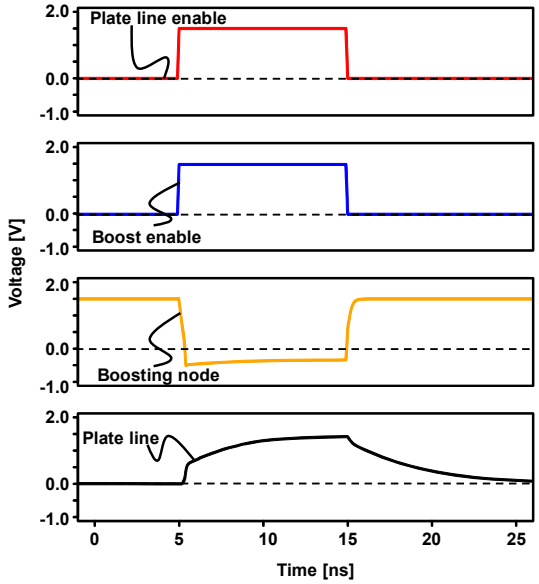

Fig. 10. Waveforms of plate line boosting.

IV. PERFORMANCE EVALUATION

To evaluate the proposed methods, we conducted SPICE simulation. TABLE II shows the simulation conditions.

Figure 11 shows the comparison of write access time. The simulation result shows the worst case of write access time is improved 21%. As shown in TABLE III, although the power overhead of word line driver is 47.8%, power overhead of 16-Kbit memory macro block is only 1.3% at TT corner. TABLE IV shows the simulation result of plate line boosting. In this condition, about 33% of plate line charge time is reduced only dissipating 0.43% power overhead and 0.0061% area overhead.

Finally, a system level processing time reduction using proposed methods is evaluated. In this estimation, we assumed a periodically wake-up application such as sensor network for environmental monitoring. Figure 12 shows the memory operation example of this application. The MCU in the sensor read and write 160-bit sensing data in every second. After the processing, the power supply of sensor will be cut off. As shown in Figure 12 and TABLE V, the word line boosting and the plate line driver boosting methods

respectively reduce 4% and 25% processing time. The total processing time reduction is 29% with up to 1.3% active power dissipation.

TABLE II. SIMULATION CONDITIONS.

Process	130nm
Temperature	25°C
Power supply	1.5V
Macro configuration	16bits/word
# of cells/WL	256
# of cells/BL	256

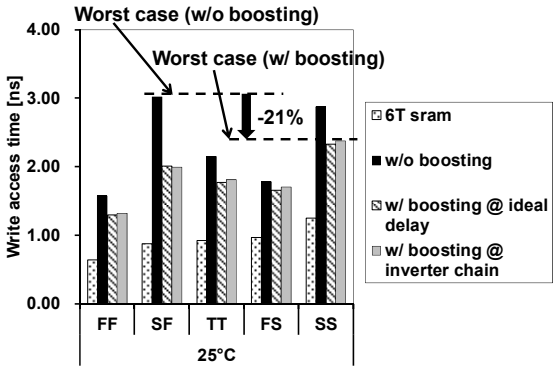

Fig. 11. Write access time comparison.

TABLE III. SIMULATION RESULT OF WORD LINE BOOSTING.

	Write access time [ns]	Energy of WL driver [pJ]	Energy of 16Kb memory [pJ]
w/o boosting	2.15	0.436	16.3
w/ boosting	1.81	0.644	16.5

TT corner, 25°C

TABLE IV. SIMULATION RESULT OF PLATE LINE BOOSTING.

	PL charge time [ns]	Energy of PL driver [pJ]
w/o boosting	10.47	46.3
w/ boosting	6.99	46.5

TT corner, 25°C

V. CONCLUSION

In this research, we proposed two boosting techniques using ferroelectric capacitor to mitigate the speed overhead of 6T-4C shadow memory. The word line boosting method achieves 21% write access time reduction with 1.3% power dissipation. The plate line driver boosting method also achieves 33% plate line charging time reduction with 0.43% power dissipation. The system level analysis using periodically wake-up sensing application example shows the proposed memory can reduce up to 29% processing time.

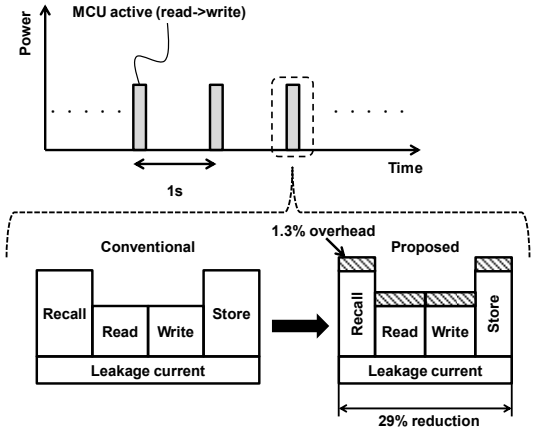

Fig. 12. Example of periodicaly wake-up sensing application.

TABLE V. PROCESSING TIME COMPARISON.

	Active time [ns]
w/o boosting	400
w/ WL boosting	385
w/ WL boosting & PL driver boosting	286

-29%

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