A Low Power 6T-4C Non-volatile Memory using Charge Sharing and Non-precharge Techniques

Tomoki Nakagawa[1], Shintaro Izumi[1], Koji Yanagida[1], Yuki Kitahara[1], Shusuke Yoshimoto[1]
Yohei Umeki[1], Haruki Mori[1], Hiroto Kitahara[1], Hiroshi Kawaguchi[1], Hiromitsu Kimura[2]
Kyoji Marumoto[2], Takaaki Fuchikami[2], Yoshikazu Fujimori[2], and Masahiko Yoshimoto[1]

[1] Kobe University, Kobe, Japan, E-mail: nakagawa@cs28.cs.kobe-u.ac.jp
[2]Rohm Co. Ltd., Kyoto, Japan

Abstract—**This report describes a low power 6T-4C non-volatile memory design using a bit-line non-precharge and plate-line charge-share techniques. Two proposed techniques contribute to decrease energy consumption. The bit-line non-precharge technique can reduce 73% of write energy consumption and 76% of read energy consumption. The plate-line charge-share technique can reduce 22% of store energy consumption and 11% of recall energy consumption.**

Keywords—Nonvolatile memory, FeRAM, Low power

I. INTRODUCTION

Recently, a lot of system-on-a-chip (SoC) has a non-volatile memory. The SoC with non-volatile memory is suitable for low active ratio applications, such as sensor network and biomedical monitoring. Non-volatile memory can keep the data during cutting off the power to reduce stand-by power consumption. Stand-by power reduction contributes to reduce the battery capacity and to minimize the size of system module. If a volatile memory (e.g. SRAM: Static Random Access Memory) is used as a data buffer in these applications, the leakage current will occupy critical portion in the total power consumption of system.

In this research, we focus on Ferroelectric Random Access Memory (FeRAM), which utilizes a ferroelectric capacitor as non-volatile element [1-4]. The benefits of FeRAM are low voltage operation and low power consumption operation [5, 6]. The FeRAM is put into practical use (e.g. noncontact IC card) [7]. The FeRAM has better availability compared with other advanced non-volatile memory.

Unfortunately, the non-volatile memory has disadvantages in operating speed, active power, and endurance [8]. To mitigate these problems, a 6T-4C non-volatile memory has been proposed [9, 10]. The 6T-4C non-volatile memory consists of 6T SRAM and four ferroelectric capacitors. Because the 6T-4C non-volatile memory act as 6T SRAM at read and write operation, it can improve the operating speed and active power. The data are stored to ferroelectric capacitors while stand-by state. Then the power supply to memory cells can be cut off. In this research, we propose bit-line non-precharge technique and plate-line charge-share technique to improve the active power consumption (see Fig. 1).Moreover, we produce test chip to measure the effectiveness of proposed techniques.

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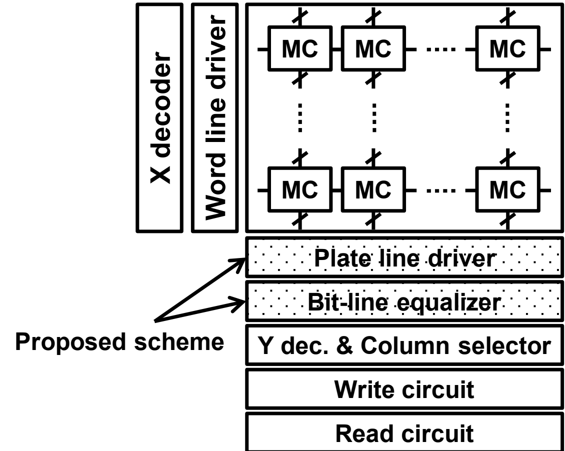


Fig. 1. Block diagram of 6T-4C non-volatile memory (MC: memory cell).

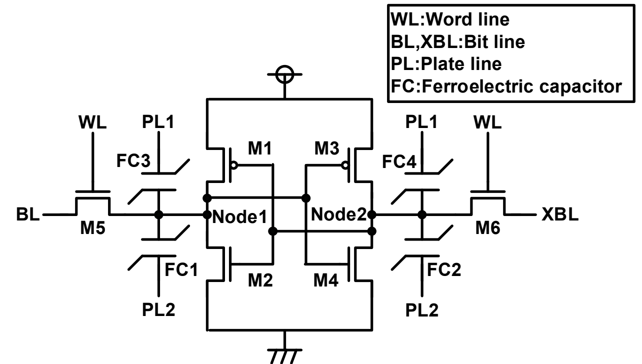


Fig. 2. Schematic of 6T-4C memory cell.

II. 6T-4C NON-VOLATILE MEMORY

Fig. 2 shows the schematic of 6T-4C memory cell. The memory cell consists of two drive transistors (M2, M4), two load transistors (M1, M3), two access transistors (M5, M6), and four ferroelectric capacitors (FC1-4). Internal nodes 1 and 2 are storage nodes of the flip-flop. A pair of bit-lines (BL, XBL) is connected to access transistors as I/O port. The two access transistors are also connected to a word-line (WL). Two plate-lines (PL1, PL2) are connected to ferroelectric capacitors to control direction of polarization.

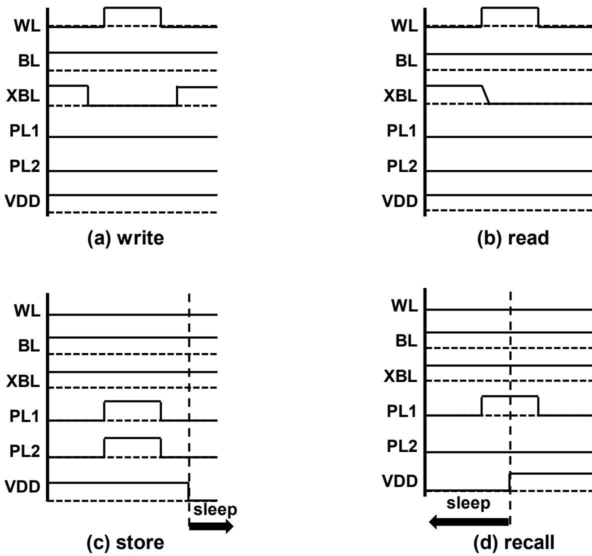


Fig. 3. Timing diagram of write, read, store, and recall operations.

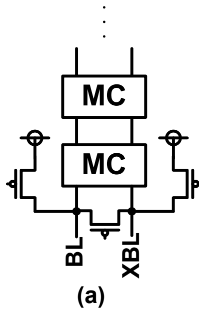


Fig. 4. Schematic of bit-line with (a) precharger, (b) equalizer.

Fig. 3 shows the timing diagram. Read and write operations are the same as 6T SRAM. The store operation, which transfers the data from internal nodes to ferroelectric capacitors, is required before cutting off the power supply of memory cells. The recall operation restores the internal nodes to previously stored condition.

III. Proposed Techniques

A. Bit-line non-precharge technique

Unfortunately, the 6T-4C non-volatile memory has a power overhead during write and read operations compared with 6T SRAM, because four ferroelectric capacitors connected to the internal nodes. To mitigate write and read power overhead, we employed the bit-line non-precharge technique. Fig. 4 shows the schematic of bit-line using pre-charger and using equalizer.

Fig. 5 (a) shows the waveforms of read operation using bit-line pre-charge. First, bit-lines are charged and forced to VDD. Next, the word-line is charged. Then bit-line, which is connected to low internal node, is discharged. Finally, the difference of bit-line's voltage is read as logical data. The conventional 6T-4C memory requires charging bit-line before charging word line to prepare read operation and to stabilize the status of half-selected cell. Half-selected cell is selected by X decoder, although it is not selected by Y decoder during read and write operations.

In conventional 6T SRAM, bit-line precharge is necessary to disturbs half-selected cells. On the other hand, the internal nods of 6T-4C memory cell are connected to four ferroelectric capacitors, and it has enough tolerance for disturbance. Therefore, the disturbance can be avoided only equalizing the bit-lines before charging word-line. Fig. 5 (b) shows the waveforms of bit-line non-precharge operation. Then, bit-lines are equalized to force same voltage. After that, it is operated as same as using bit-line pre-charger. Therefore the pre-charging power can be omitted in write and read operations.

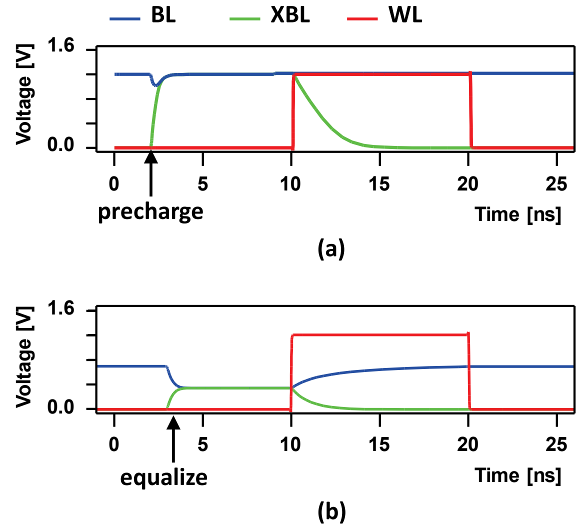


Fig. 5. Waveforms of read operation using (a) bit-line precharge (b) bit-line non-precharge.

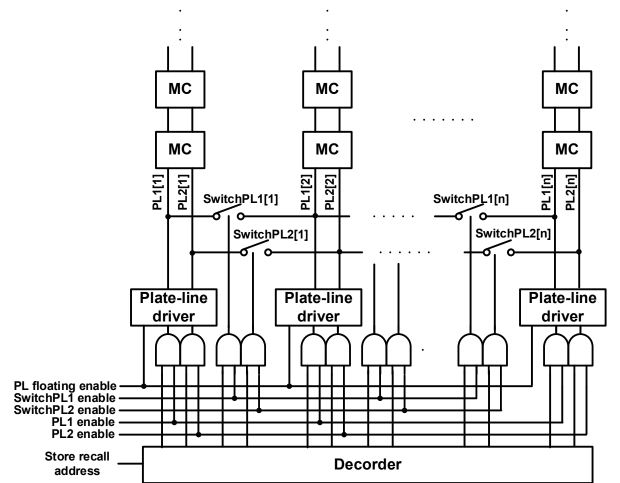


Fig. 6. Schematic of plate-lines with switches.

B. Plate-line charge-share technique

The 6T-4C non-volatile memory requires store and recall operations before cutting off and power on. The plate-lines are charged by plate line driver in these operations. However, driving plate lines needs large power because ferroelectric capacitors, which are connected to plate-line, have large capacitance. To decrease the plate line charging power, we propose the plate-line charge-share technique. Fig. 6 shows the proposed plate-line circuit with charge-sharing switches. Each two adjacent plate-lines have switches to reuse its charge. Here, switchPL1[n] denotes the switch between PL1[n] and PL1[n+1] .

Fig. 7 (a) shows the waveform of plate-line charging without charge-sharing technique. PL1[1] and PL1[2] are charged and discharged in series. In this operation, plate-line driver needs charging plate-lines from 0V to VDD. Thus the 6T-4C memory consumes large power for store and recall operations.

Fig 7 (b) explain the waveform of proposed plate-line charging using charge-sharing switches. Additional switches between plate-lines are used to share the charge used for store and recall operations. The switchPL1[1] is connected after the PL1[1] is charged, and the charging of PL1[1] is shared with the PL1[2]. The PL1[2] is charged after cutting the switchPL1[1]. Other plate-lines are charged in same manner, and the charge is transported sequentially. Thus, the proposed technique can decrease store and recall power.

Required time for store and recall can be reduced by charging plate-lines in parallel. However, when multiple plate-lines are charged at the same time, rush current is increased. The number of plate-lines, which is driven simultaneously, is limited by the characteristics of power source. Fig. 8 shows the relationship between the rush current and the number of driven plate-lines.

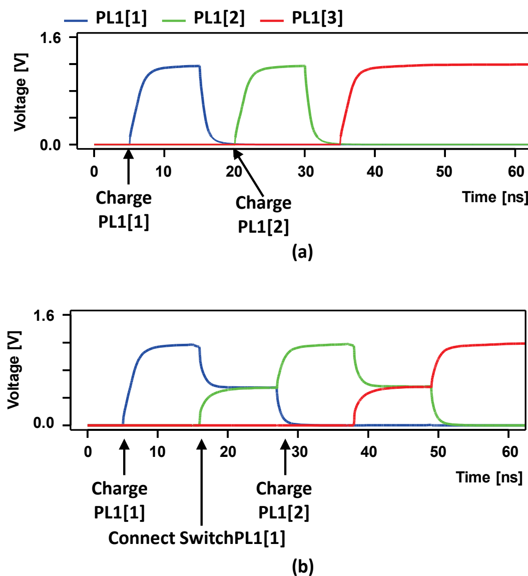


Fig. 7. Waveforms of charging plate-lines
(a) without plate-line charge-share technique,
(b) with plate-line charge-share technique.

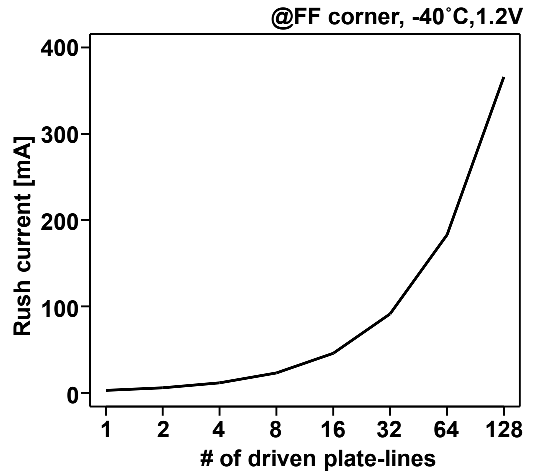
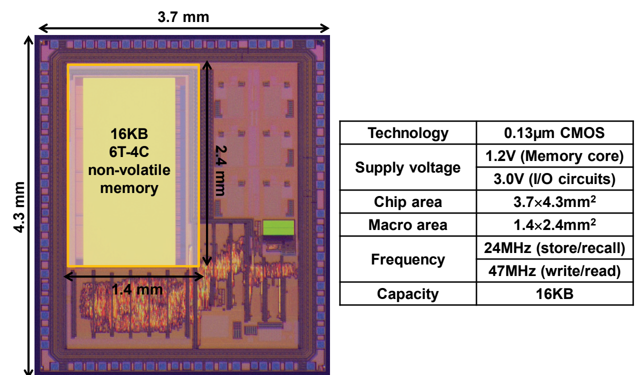


Fig. 8. The number of driven plate-lines versus rush current in store operation.



Technology	0.13µm CMOS
Supply voltage	1.2V (Memory core)
	3.0V (I/O circuits)
Chip area	3.7×4.3mm²
Macro area	1.4×2.4mm²
Frequency	24MHz (store/recall)
	47MHz (write/read)
Capacity	16KB

Fig. 9. Chip micrograph and chip specifications.

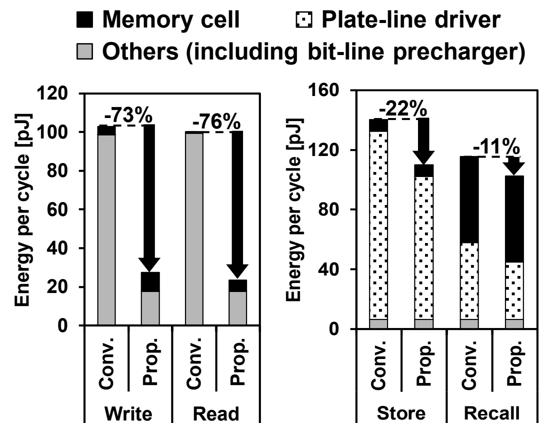


Fig. 10. Measured energy consumption
of conventional and proposed 6T-4C non-volatile memory.

IV. Chip Implementation and Mesurement Results

The 3.7×4.3 mm^2 test chip is fabricated using 0.13 µm CMOS technology. Fig. 9 shows the chip micrograph and

performance summary. The operating voltage of memory core is 1.2V. IO circuits are operated with 3.0V supply voltage. The area of the memory macro is 1.4×2.4 mm^2. The memory capacity is 16KB. Maximum operating frequency is 24MHz during store and recall operations. During write and read operations, maximum operating frequency is 47MHz.

Fig. 10 shows the measurement results of power consumption. The energy consumptions of write and read operations are respectively reduced by 73% and 76% using bit-line non-precharge technique. When bit-line is pre-charged, the current from memory cell to bit-line is reduced. However, peripheral circuits including bit-line pre-charger consumes large energy for pre-charging bit-lines. On the other hand, when using bit-line non-precharge technique, bit-lines are equalized to about half-VDD. Therefore, the current from memory cell to bit-lines is increased compared with using bit-line pre-charger. However, the total energy consumption of peripheral circuits is reduced because the energy for bit-line pre-charge is dominant.

The energy consumptions in store and recall operations are respectively reduced by 22% and 11% using plate-line charge-share technique. Then, the energy consumption of plate-line driver is reduced compared with conventional circuits. In store operation, both of two plate-lines are charged. However, in recall operation, only one plate-line is charged. Therefore the energy reduction ratio in store operation is twice as large as recall operation.

Fig. 11 shows the shmoo plot of the test chip in store and recall operations. The minimum cycle time with 1.2V supply voltage is 41 ns. Fig. 12 shows the shmoo plot in write and read operations. The test chip can operate at a cycle time of 21ns.

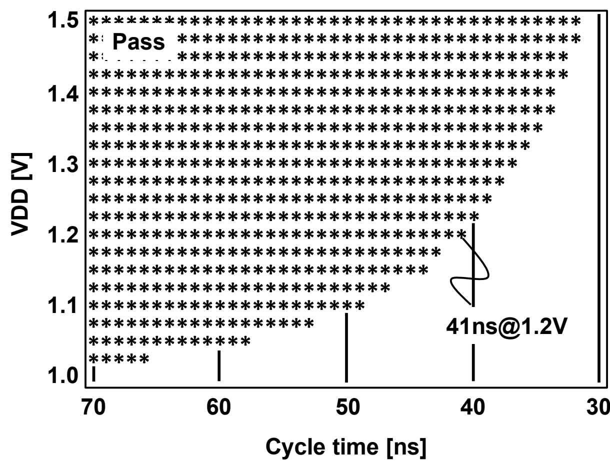


Fig. 11. Shmoo plot of store and recall operations.

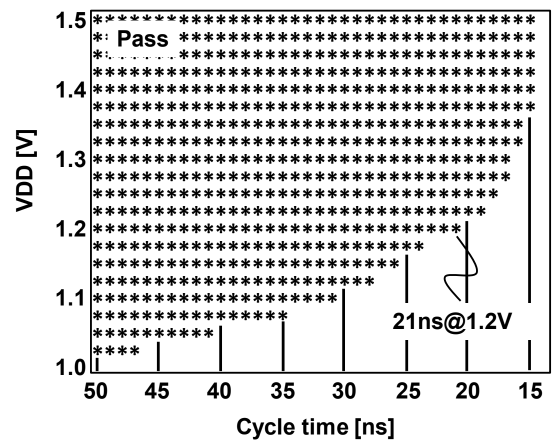


Fig. 12. Shmoo plot of write and read operations.

V. CONCLUSION

In this research, we proposed two techniques to decrease operating power of 6T-4C non-volatile memory. The bit-line non-precharge technique achieves 73% write energy reduction and 76% read energy reduction. The plate-line charge-share technique also achieves 22% store energy reduction and 11% recall energy reduction.

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