A 40-nm Resilient Cache Memory for Dynamic Variation Tolerance with Bit-Enhancing Memory and On-Chip Diagnosis Structures Delivering ×91 Failure Rate Improvement

Yohei Nakata[1], Yuta Kimi[1*], Shunsuke Okumura[1], Jinwook Jung[1], Takuya Sawada[1], Taku Toshikawa[1], Makoto Nagata[1, 5], Hirofumi Nakano[2], Makoto Yabuuchi[3], Hidehiro Fujiwara[3], Koji Nii[3], Hiroyuki Kawai[4], Hiroshi Kawaguchi[1] and Masahiko Yoshimoto[1, 5]
[1]Graduate School of System Informatics, Kobe University, Kobe, 657-8501 Japan
[2]Renesas Electronics Corporation, Itami, 664-0005 Japan
[3]Renesas Electronics Corporation, Kodaira, 187-8588 Japan
[4]Renesas Electronics Corporation, Tokyo, 100-0004 Japan
[5]Japan Science and Technology Agency (JST) CREST, Tokyo, 102-0076 Japan
[*]E-mail: kimi@cs28.cs.kobe-u.ac.jp

Abstract

This paper presents a resilient cache memory for dynamic variation tolerance in a 40-nm CMOS. The cache can perform sustained operations under a large-amplitude voltage droop. To realize sustained operation, the resilient cache exploit 7T/14T bit-enhancing SRAM and on-chip voltage/temperature monitoring circuit. 7T/14T bit-enhancing SRAM can reconfigure itself dynamically to a reliable bit-enhancing mode. An on-chip monitoring circuit can sense a precise supply voltage level of a power rail of the cache. The proposed cache can dynamically change its operation mode using the voltage/temperature monitoring result and can operate reliably under a large-amplitude voltage droop. Experimental result shows that it does not fail with 25% and 30% droop of V_{dd} and it provides 91 times better failure rate with a 35% droop of V_{dd} compared with the conventional design. The processor simulator shows that the proposed cache running in the bit-enhancing mode results in 2.88% IPC loss on average.

Keywords

Design for robustness, Cache, Dynamic variation tolerance, 7T/14T SRAM

1. Introduction

Technology scaling increases the threshold-voltage (V_{th}) variation of MOS transistors mainly because of random dopant fluctuation. The minimum operating voltage (V_{min}) of SRAM cell increases as the V_{th} variation increases with technology scaling. Increase in the V_{min} degrades operating margin of processors. A processor with a shrinking operating margin is more susceptible to power supply noise, IR drops, and temperature fluctuations. Especially, electric control units in electric vehicles suffer large temperature fluctuation and large voltage fluctuation/droop caused by motor noise, EMIs, voltage surges, and sudden interruptions in wiring harness connections. A sudden interruption, for example, can cause disconnection of the ECU to the power supply for several milliseconds. Power supply circuits implemented in the ECU have large capacitors to improve tolerance against sudden interruptions. If the capacitance is hundreds of microfarads, then the voltage droops caused by the sudden interruptions are reduced to less than 20% droop, with droop duration in the milliseconds. However, the use of a large capacitor for the ECU should be avoided for reason of reliability, cost, and size. Consequently, voltage-variation (the voltage droops of 20% V_{dd}) and temperature-variation tolerant processors are needed for ECUs in electric vehicles.

Earlier designs [1]–[3] have addressed timing errors caused by a high-frequency (ca. 100 MHz) voltage droop. A tunable replica scheme [4] can reduce V_{min} of SRAM by 9% under 13% voltage droop. However, they cannot mitigate embedded SRAM margin failures caused by large amplitude (ca. 20% of V_{dd}) voltage droops. An SRAM cache in a processor with high integration and minimum-size transistors determine the V_{min} of the entire processor. Therefore, a fault-tolerant cache is required to realize dynamic variation tolerant processors.

A common fault-tolerant cache architecture uses redundant columns/rows [5]. The architecture requires many redundant columns/rows to accommodate the large number of faults, while the columns/rows are inefficient in low failure rate situation. The PADed cache proposed in [6] uses programmable decoder to remap faulty cache lines to non-faulty ones. As another solution, the error correction code (ECC) has been applied to caches [7], [8]. Two-dimensional ECC proposed in [8] combines vertical error coding and horizontal error coding. However, these techniques are not effective under large amplitude voltage droops that cause a great deal of faults because the fault-tolerance of these techniques depends on the number and locations of erratic bits.

Herein, we present a resilient cache memory that can perform sustained operations under a large-amplitude voltage droop. To realize sustainable operation, the resilient cache exploits 7T/14T bit-enhancing SRAM, which has a more reliable operation mode and on-chip voltage monitoring circuit.

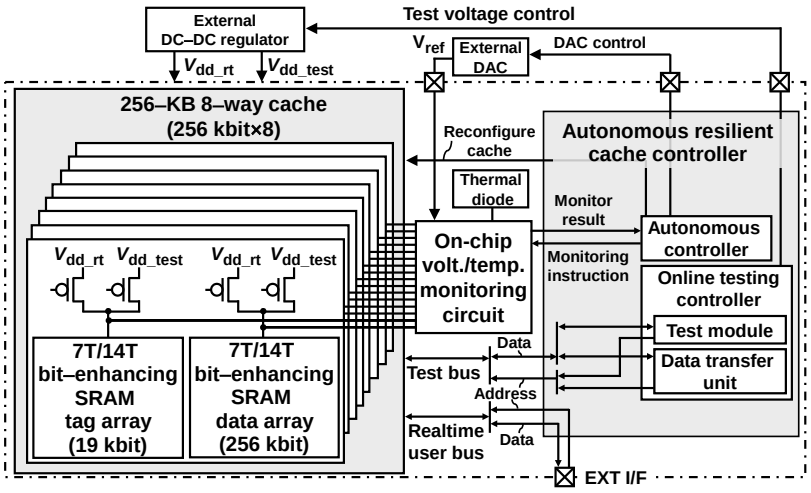


Figure 1: Block diagram of the resilient cache.

2. Proposed Resilient Cache

The resilient cache (Fig. 1) is a 256 KB 8-way cache memory array with 7T/14T bit-enhancing (BE) SRAM bitcell structure [9], voltage and temperature monitoring circuits [11], and an autonomous resilient cache controller. A power supply of each memory block can be switched to the power supply for runtime operation (V_{dd_rt}) or the power supply for testing (V_{dd_test}) individually. The local power rails of the memory blocks are monitored by voltage monitoring circuits, which can obtain a precise supply voltage level at a testing time and monitor a voltage fluctuation during runtime. Furthermore, a temperature monitoring circuit can sense the on-chip temperature. The temperature information recorded at a testing time is used in a temperature correction of the V_{min}. The autonomous resilient cache controller comprises an autonomous controller and an online testing controller with a test module and data transfer unit. The online testing controller can execute memory testing that is completely transparent to user accesses and which can obtain an operation margin and V_{min} of the memory block. The autonomous controller controls a probing point of the voltage monitor and reference voltage (V_{ref}) control using the external DAC. It receives monitoring results from monitoring circuits. The results are used for voltage droop detection and block-basis voltage droop control, as described in the remainder of the paper.

2.1. 7T/14T bit-enhancing SRAM bitcell

Each SRAM cell in the proposed resilient cache comprises 7T/14T BE SRAM cell structure [9]. The 7T/14T BE SRAM cell has a pair of conventional 6T SRAM bitcells. The internal nodes are connected directly by two additional PMOS transistors as presented in Fig. 2. This structure of 7T/14T BE SRAM provides an additional operation mode designated as the enhancing mode along with the normal mode. The two modes of 7T/14T BE SRAM are presented in Table I. Fig. 3 shows bit error rates in 7T/14T BE SRAM and in the other scheme [10]. In enhancing mode, the

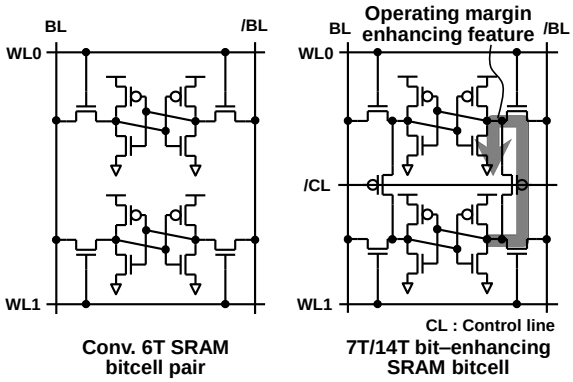


Figure 2: Schematics showing a conventional 6T SRAM bitcell pair and 7T/14T bit-enhancing SRAM bitcell.

Table 1: Two operation modes of 7T/14T bit-enhancing bitcell.

Mode	*# of memory cells comprising 1 bit*	*# of WL drives*	*CL*
Normal	1 (7T/bit)	1	Off (“H”)
Enhancing (read)	2 (14T/bit)	1	On (“L”)
Enhancing (write)	2 (14T/bit)	2	On (“L”)

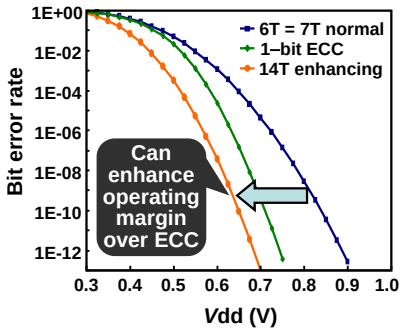


Figure 3: Bit error rates (BERs): “6T”, “1-bit ECC” and “7T normal” and “14T enhancing” using 7T/14T bit-enhancing SRAM.

added transistors are activated and BE SRAM features reliable operations especially at low voltages by combining two bitcells. A 7T cell with insufficient operating margin is covered by the other cell through activating these added transistors.

2.2. On-chip monitoring circuits

On-chip monitoring circuits, presented in Fig. 4, comprise a source follower (SF) and a latch comparator (LC) [11]. Supply voltage monitoring circuits measure the supply voltage fluctuation on power rails of each SRAM array. Temperature monitoring circuits sense thermal diodes placed near the center of the cache macro.

Voltages on the probing point and thermal diode are level-shifted by the SFs. The level-shifted voltage (V_{sfo}) is compared with the reference voltage (V_{ref}) by the LC in synchronization with a sampling clock. The LC outputs "1" or "0" corresponding to the comparison result.

The on-chip monitoring circuits are area-efficient and can sense accurate voltage level of the SRAM array, in addition to the cache temperature. Therefore, they are suitable for use in online built-in self-tests (BISTs) and voltage droop detection.

2.3. Block basis online testing

The online testing controller measures operation margin and V_{min} of the memory blocks with current temperature. The adaptive control using the online testing result can deal with dynamic temperature fluctuation at operating time, but a boot time testing not. Figure 5 shows the block basis online testing scheme for the proposed resilient cache. The online test controller conducts memory testing on each memory block in order of the physical block address. It decreases the supply voltage of the testing block gradually during the testing time. The controller records the testing voltage and temperature from the on-chip monitoring circuits with respect to each operation mode of BE SRAM at which the first failure is detected. The resilient cache still has cache lines to which data can be allocated even if memory testing is working because it is block-basis testing. The memory blocks, except the current memory under test (MUT) block, are still accessible. Thereby they can operate as runtime (RT) blocks.

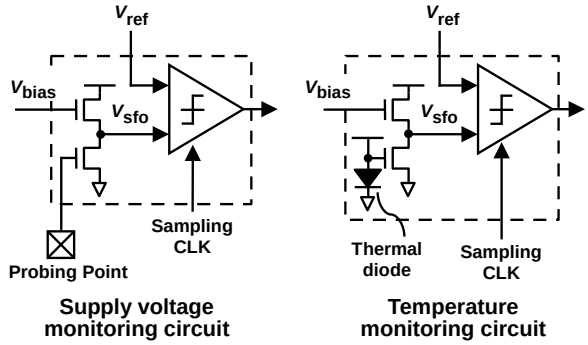


Figure 4: Supply voltage/temperature monitoring circuit.

The proposed testing scheme is transparent to the processor operation because the testing controller uses the test bus separated from the user bus. Although one cache way cannot be used during the testing, processor simulation using gem5 simulator [12] shows the IPC performance degradation in the SPEC 2006 benchmarks [13] is less than 1%. The test is conducted periodically. The testing cycle can be regulated outside the cache (e.g. a cycle responding to a control period of the software). The IPC degradation is 1% at most, although it depends on the testing cycle.

The flowchart in Fig. 6 depicts the online testing flow. At the beginning of memory testing on each block, the data transfer unit transfers data from the MUT block to the previous MUT block. The power supply of the MUT block is switched to testing voltage (V_{dd_test}). After switching, a testing is executed to evaluate whether the failure is detected or not. If not detected, then V_{dd_test} is decreased by one step and the testing is executed again. If detected, then the voltage at that time is recorded with temperature. Having completed the testing on one block, the online test controller sets V_{dd_test} to a nominal V_{dd} and changes next block into MUT. This flow continues until all blocks have been tested.

Operation of the data transfer unit is depicted in Fig. 7. First, physical block 0 is tested. Physical blocks of 1–7 operate as runtime blocks. Next, the data transfer unit transfer data from physical block 1 (next MUT) to physical block 0 (previous MUT). After the transfer, physical block 1 is tested. Physical block 0 and physical blocks 2–7 operate as runtime blocks. In this way, the MUT block moves among 8 blocks without losing the memory contents.

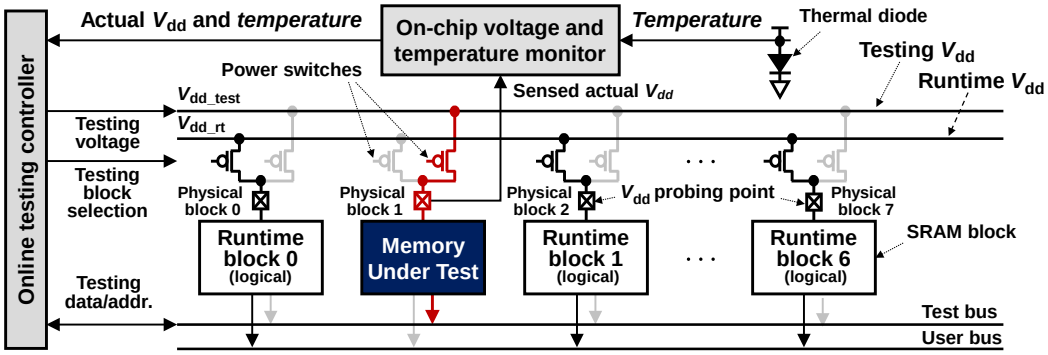


Figure 5: Online testing architecture.

An example of test results is presented in Fig. 8. The online testing controller has a test result table to record V_{min} corresponding to temperature. The recorded testing voltage is actual V_{min} of the memory array because the on-chip voltage monitor probes the local power rail of the memory blocks. The voltage monitor traces the bottom level of the testing voltage (V_{bottom}) during the testing time to record an actual V_{min}. The test result table is used as a reference for the voltage–temperature variation adaptive control described later.

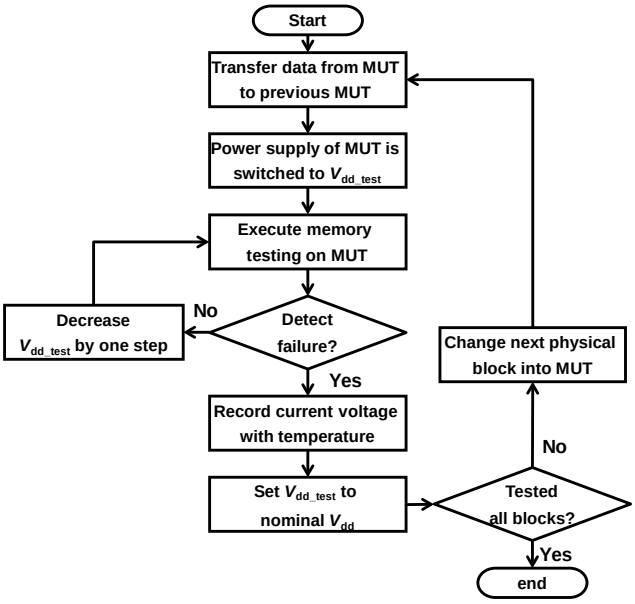


Figure 6: Flowchart of the online testing.

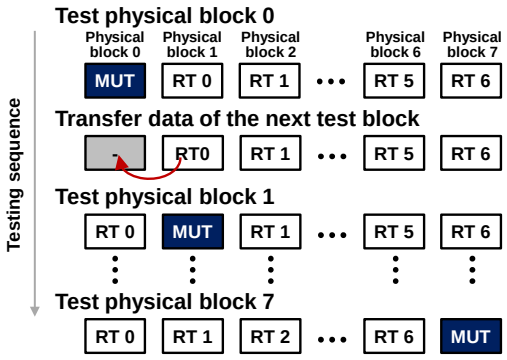


Figure 7: Block basis online testing scheme.

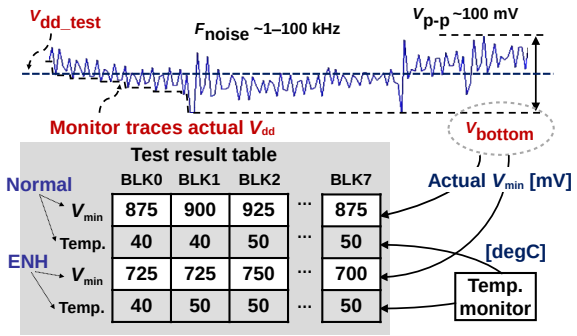


Figure 8: Block basis actual V_{min} and temperature recording.

2.4. Voltage and temperature variation adaptive control

Figures 9, 10 and 11 present a voltage–temperature variation adaptive control scheme. The autonomous controller detects degradation of the operating margin caused by the voltage and temperature fluctuation. If the margin is insufficient for stable operation, the controller changes the operation mode of 7T/14T bit-enhancing SRAM to the 14T enhancing mode. This adaptive control enables maintenance of the required voltage margin in the current operating condition.

To detect the voltage droop, reference voltages "high" (V_{ref_high}) and "low" (V_{ref_low}) are set to the proper level as shown in Fig. 9. V_{dd} is monitored by the monitoring circuit using V_{ref_high} and V_{ref_low}. When V_{dd} falls below V_{ref_high}, a timer starts to count. Then, as V_{dd} falls below V_{ref_low}, the timer stops to count and a gradient of the voltage droop is calculated. The autonomous controller estimates whether the V_{dd} drops below V_{min_normal} or not using the gradient. If the gradient is greater than the threshold value, then the controller estimates that the V_{dd} crosses V_{min_normal}. If not, then the controller estimates that the V_{dd} does not cross V_{min_normal} (shown in Fig. 9 (b)). The resilient cache changes the operation mode to the 14T enhancing mode at the voltage below V_{min_normal}.

This voltage variation adaptive control scheme is performed in a block-basis manner. Only blocks for which the V_{dd} drops below its V_{min_normal} change the operation mode to the 14T enhancing mode as presented in Fig. 10. The other blocks keep the operation mode as the 7T normal mode.

The V_{min} at runtime is corrected in response to the runtime temperature to compensate the temperature fluctuation (shown in Fig. 11). The autonomous controller obtains the current temperature using the on-chip temperature monitor and looks up V_{min} in the test result table. The V_{min} corresponding to the current temperature is

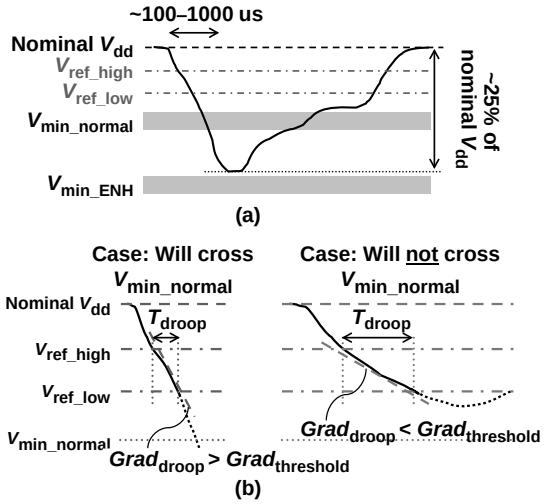


Figure 9: (a) Example of voltage waveform. (b) Voltage droop detection scheme.

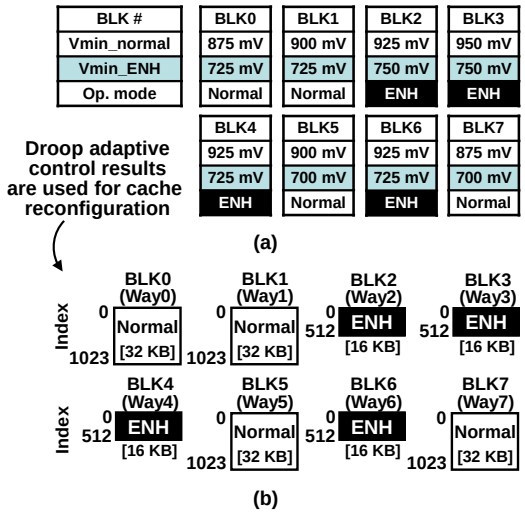


Figure 10: (a) Block basis voltage droop control. (b) Cache configuration during voltage droop.

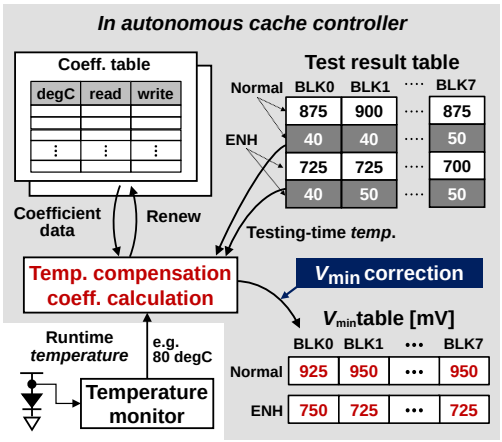


Figure 11: V_{min} correction responding to temperature variation.

calculated using these data. The coefficient data to compensate temperature difference between the testing time and current time are recorded in coefficient tables. The calculated V_{min} are collected in V_{min} tables. The V_{min} tables are used to determine the threshold of the gradient in the droop detection.

When the autonomous controller changes operation mode of the blocks into bit-enhancing mode, dirty cache lines in the blocks must be migrated. The migration process shows in Fig. 12. In this example, a target block of the mode transition is block 7. The controller searches dirty cache lines in the odd index of block 7. Dirty lines in the even index do not need to migrate because these lines are used after the mode transition. If the dirty cache line is detected, then the cache line migrates into the least recently used (LRU) cache line in same set. If the LRU cache line is also dirty, then the LRU line is written back to main memory before the detected dirty line is migrated. If the detected dirty line is LRU line, then the line is written back to main memory.

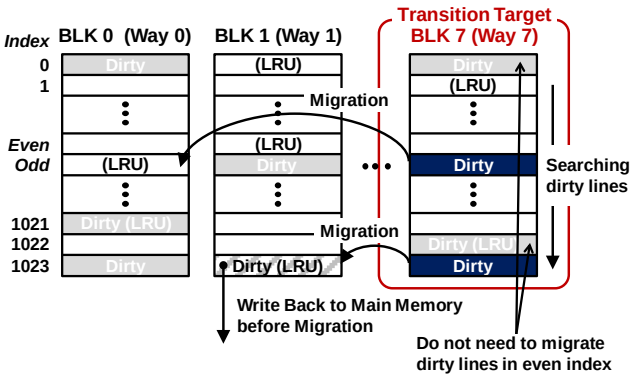


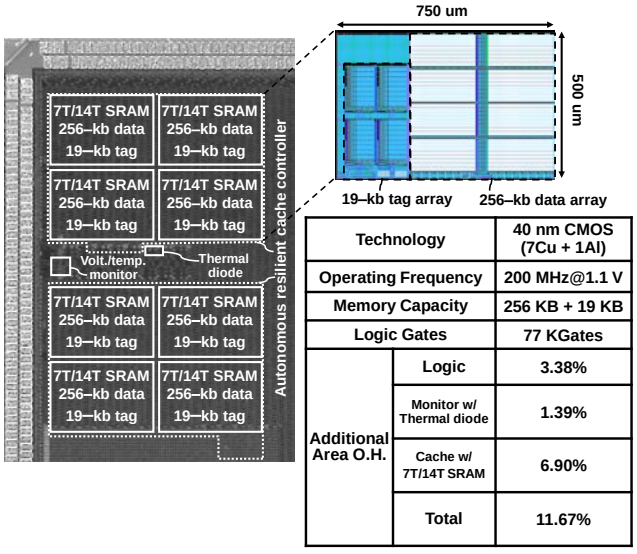
Figure 12: Migration process for dirty cache lines in the mode transition target.

If the V_{dd} is over V_{ref_high} again, then the autonomous controller changes the operation mode of the blocks from bit-enhancing mode to normal mode. In such cases, it is unnecessary to migrate cache lines. The controller simply inactivates the control signal of the 7T/14T bit-enhancing SRAM (CL depicted in Fig. 2) and sets the cache state of the cache lines in the odd index to invalid.

We estimate migration time when all eight blocks are changed into bit-enhancing mode simultaneously (in the worst-case situation). The estimation using gem5 simulator [12] shows the controller can migrate dirty cache lines in 153 µs.

3. Measurement Results

Measurement results obtained using a test chip fabricated in 40-nm CMOS (Fig. 13) are presented in Figs. 14–16.



Technology		40 nm CMOS (7Cu + 1Al)
Operating Frequency		200 MHz@1.1 V
Memory Capacity		256 KB + 19 KB
Logic Gates		77 KGates
Additional Area O.H.	Logic	3.38%
	Monitor w/ Thermal diode	1.39%
	Cache w/ 7T/14T SRAM	6.90%
	Total	11.67%

Figure 13: Micrograph and features of test chips.

3.1 On-chip voltage droop waveform and V_{min} of memory blocks

The voltage monitoring circuit measures the on-chip voltage droop waveform (Fig. 14). An upper waveform in Fig. 14 is the injected waveform from outside the chip. This

waveform is measured at off-chip probing point on the global power rail. A lower waveform is acquired by measurement with the on-chip monitoring circuit, which probes the local power rail of each memory block. The on-chip measurement waveform shows a different shape from that of the injected waveform because of parasitic elements of the chip. The result shows that the on-chip monitoring circuit is necessary to obtain a precise voltage level.

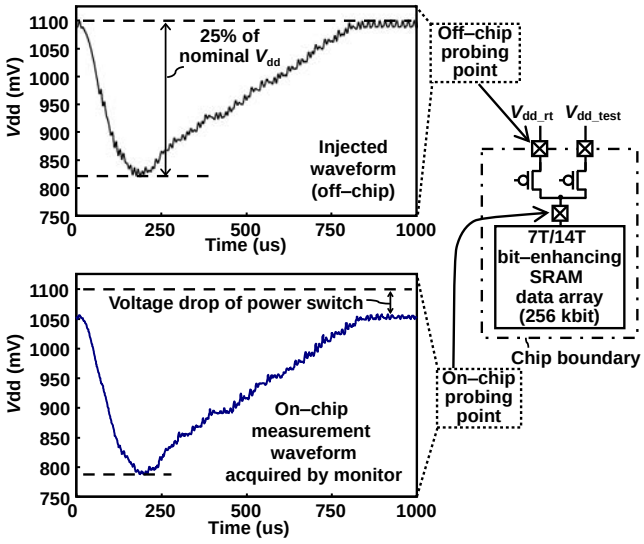


Figure 14: Measured off-chip/on-chip voltage droop waveforms.

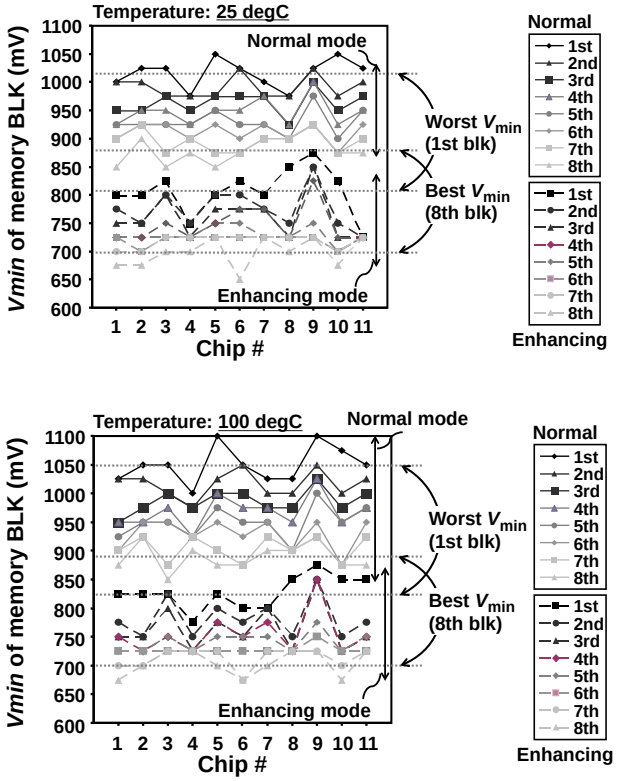


Figure 15: V_{min}s of eight memory blocks of 11 chips (measured).

Measured minimum operating voltage (V_{min}) characteristics of the memory blocks are shown in Fig. 15. The V_{min}s are acquired for 8 blocks of 11 chips at each operation mode of BE SRAM. The temperature at the measurement is normal (25 °C) and high (100 °C). The averages of the V_{min} of the worst block (i.e. V_{min} of the entire cache) for 11 chips are 1015 mV in normal mode and 806 mV in bit-enhancing mode at 25 °C. At 100 °C, the average V_{min} in normal and bit-enhancing modes are 1050 mV and 827 mV respectively. Results show that changing the operation mode of BE SRAM to bit-enhancing mode improves the operating margin by 205 mV at 25 °C and 223 mV at 100 °C, on average.

3.2 Voltage variation tolerance

The voltage variation tolerance of the resilient cache is evaluated using a voltage droop injection to the external power supply rail. During voltage droop injection, the trace of cache access is input to the resilient cache. Then the accesses to fail bits are counted as the number of failure. Five cache traces were taken from SPEC 2006 [13]. The evaluation shows that the resilient cache does not fail irrespective of the droop duration length when the voltage droop amplitude is 20%. Therefore, it is seen that the resilient cache can be applied to the ECUs in electronic vehicles.

To investigate the voltage variation tolerance of the resilient cache, we conducted evaluation under voltage droop conditions with amplitude higher than 20%. The amplitudes of the voltage droop are assumed to be 25%, 30%, and 35% of V_{dd} as shown in Fig. 16 (a). The droop durations are 500 µs, 5 ms and 50 ms. Evaluation results under 25%, 30% and 35% droop condition are depicted respectively in Fig. 16(b)–16(d). Under 25% and 30% droop conditions, the failures increase linearly with droop duration length without the proposed scheme (no variation adaptive control and always normal mode). Using the proposed scheme (variation adaptive control and adopt switching to enhancing mode), the resilient cache does not fail irrespective of the droop duration length. Under a severe 35% droop condition, failures without the proposed scheme increased numerically to about ten times those under a 25% droop condition. Using the proposed scheme, the failure rate improved by 91 of that without the proposed scheme under 50 ms droop duration.

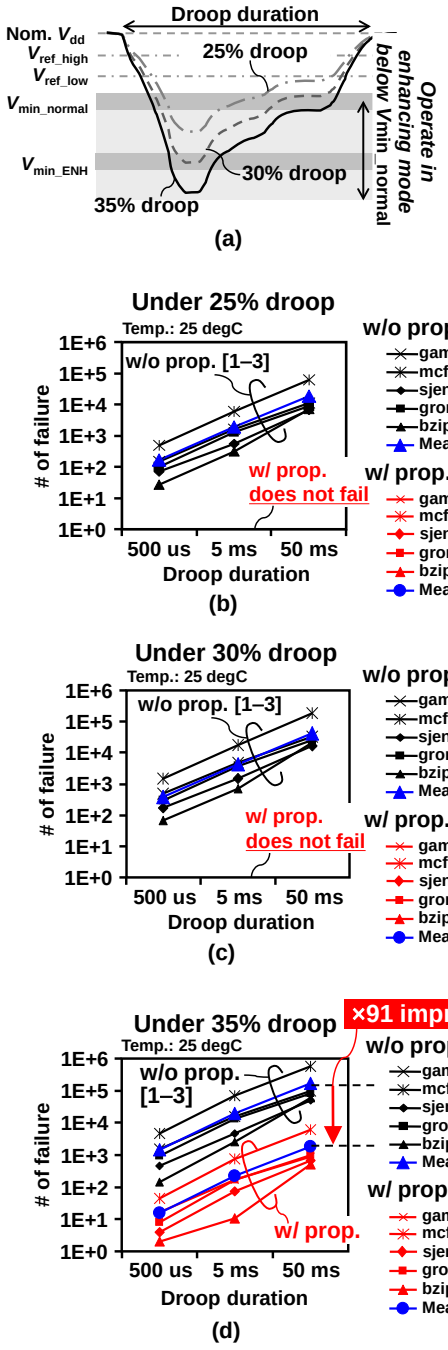


Figure 16: Voltage droop tolerance and failure count evaluation: (a) droop waveform example, (b) 25% V_{dd} droop, (c) 30% V_{dd} droop, and (d) 35% V_{dd} droop.

3.3 Processor Performance

The cache reconfiguration affects processor performance. The cache capacity decreases by 16 KB when one block changes its operation mode into bit-enhancing mode. The capacity decrease degrades processor performance since cache misses occur more frequently. Figure 17 shows normalized instruction per cycles (IPCs) with respect to the number of bit-enhancing mode blocks. The evaluation is conducted using gem5 simulator [12], with benchmarks selected from SPEC 2006 [13]. The average IPC loss is

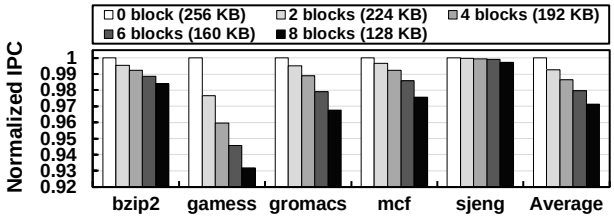


Figure 17: Normalized IPCs with respect to the number of bit-enhancing mode blocks.

2.88% when all blocks are bit-enhancing mode (128 KB cache capacity). The resilient cache operates in bit-enhancing mode only if the operating margin is insufficient, and continues stable operation though processor performance degrades.

3.4 Area and Power

The area overhead of the autonomous controller is 3.38% and that of the monitoring circuits is 1.39%. The estimation using CACTI [14] shows the proposed resilient cache with 7T memory cell is imposed 6.90% area overhead compared to the conventional cache with 6T memory cell. The total area overhead is 11.67%. Total power overhead for the proposed resilient cache with 7T memory cell, the online testing and the monitors is 12.7% compared to the conventional cache with 6T memory cell.

4. Conclusion

As described in this report, we proposed a resilient cache with bit-enhancing memory and on-chip diagnosis structures in 40-nm CMOS. The resilient cache has a bit-enhancing memory that can dynamically change itself to enhancing mode and on-chip voltage/temperature monitoring circuit. It dynamically reconfigures its operation mode using the voltage/temperature monitoring result. It achieves a 91 times better failure rate under 35% droop of V_{dd} compared with that of the conventional design.

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