A Ferroelectric-Based Non-Volatile Flip-Flop for Wearable Healthcare Systems

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***Abstract*—The low-power FE-based NVFF is developed by reduction of FE capacitor size. In the proposed NVFF, coupled FE capacitors with complementary data storage are introduced. The use of complementarily stored data in coupled FE capacitors achieves 88% FE capacitor size reduction while maintaining a wide read voltage margin of 240 mV (minimum) at 1.5 V, which results in 2.4 pJ low access energy with 10-year, 85◦C data retention capability. An access speed of FE capacitors can be adaptively changed according to required retention time, which becomes 1.6 μs for 10-year data retention, and 170 ns for 10-hour data retention. Especially, short-term data retention is suitable for power gating implementation. As a design example, the proposed NVFF is applied to 32-bit CPU in a vital sensor LSI for wearable healthcare applications. The vital sensor LSI consists of an electrocardiogram (ECG) sensor, the 32-bit CPU core with NVFF, and a 16-Kbyte FE-based non-volatile memory (NVRAM) for data and instruction. Because the frequency range of vital signals is low, both the standby power reduction and sleep time maximization is important to system level power reduction. Its standby current can be cut when the state of CPU core transits to deep sleep. Then the data in the memory and register values of CPU core in the NVFF are stored sequentially to ferroelectric capacitors. The implementation result demonstrates that 87% of total power dissipation during measurement of the heart rate can be reduced with 64% area overhead using 130-nm CMOS with $Pb(Zr,Ti)O_3$(PZT) thin films.**

Keywords- non-volatile flip-flop; ferroelectric capacitor; non-volatile microprocessor; mobile healthcare; wearable sensors

I. INTRODUCTION

Low power logic circuits have been attracting more and more attentions with the rapid spread of LSI applications such as mobile electronics. And the reduction of standby power is one of critical issues for low-power LSI since the leakage current increases with downscaling of technology node.

The technology of non-volatile logic (NVL) using nonvolatile flip-flops (NVFF) is one of the promising candidates to solve the above problem [1]. In the NVL, all registers consist of NVFFs which have capability to retain its state without power supply. Therefore, leakage current can be cut off by turning off the power supply during standby state. The NVL technology is also suitable for energy harvesting applications such as infrastructure because it is capable of continuously operating a logic circuit and retaining state during frequent power interruption, i.e., unstable power supply.

As a possible approach to implementing the NVL circuit, we have been proposed a ferroelectric-based (FE-based) NVFF [2, 3]. The use of the FE capacitors makes it possible to implement non-volatile storage elements to all flip-flops (FFs) randomly placed on a logic circuit by these CMOS-process compatibility and low-voltage operation capability. Moreover, data protection techniques have also been proposed to prevent data destruction caused by an illegal access for the FE capacitor during standby state [3], which contributes to implement highly reliable NVL LSI. These NVL circuit technologies have already been applied to mass-produced LSIs. However, the previous NVFF involves energy loss of 19.4pJ per read and write operations of FE capacitors, which degrade power reduction effect based on zero standby power.

To overcome this problem, the low-power FE-based NVFF is developed by reduction of FE capacitor size. In the proposed NVFF, coupled FE capacitors with complementary data storage [4] are introduced to perform reduction of FE capacitor size while maintaining a read voltage margin ΔV_{OUT} required for non-volatile storage capability. Since ΔV_{OUT} is determined by only a ratio of remnant polarization charges between coupled FE capacitors, FE capacitor size can be reduced within maintaining a ratio of remnant polarization charges. An evaluated result of an NVFF test chip shows that FE capacitor size can be reduced to 12% of that used in the previous NVFF with minimum ΔV_{OUT} of 240mV under 1.5V operation, thereby resulting in 2.4pJ low access energy with 10-year, 85°C data retention capability. An access speed of FE capacitors can be adaptively changed according to required retention time, which becomes 1.6μs for 10-year data retention, and 170ns for 10-hour data retention. The former is suitable for event-driven applications like as energy-harvesting systems, which require 10-year data retention characteristic for an unexpected period of power off state, while the access speed of will be negligible because it needs a few milliseconds at power on/off sequence accounts for its weak power supply. The later is suitable for task-scheduled applications like as power-gating systems, which need short access time for instant power control, while 10-hour data retention characteristic will be acceptable because a period of power off state is controllable.

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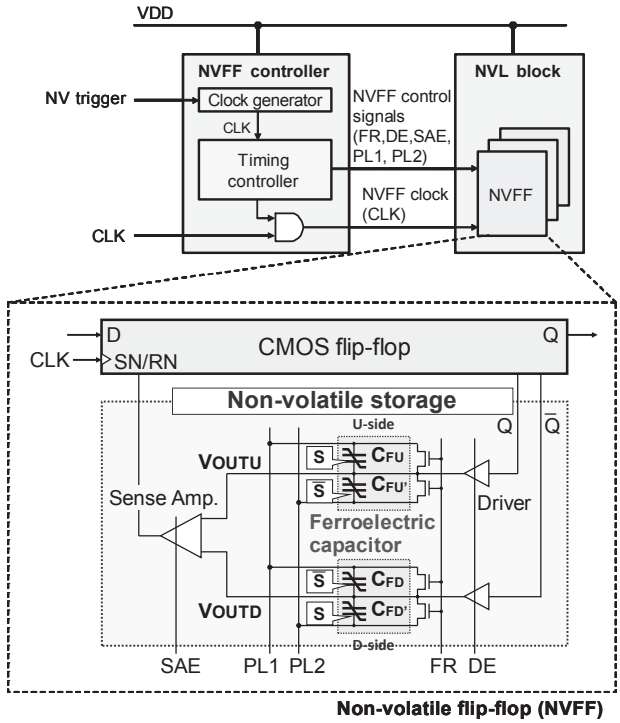


Figure 1. Overall structure of a non-volatile logic circuit.

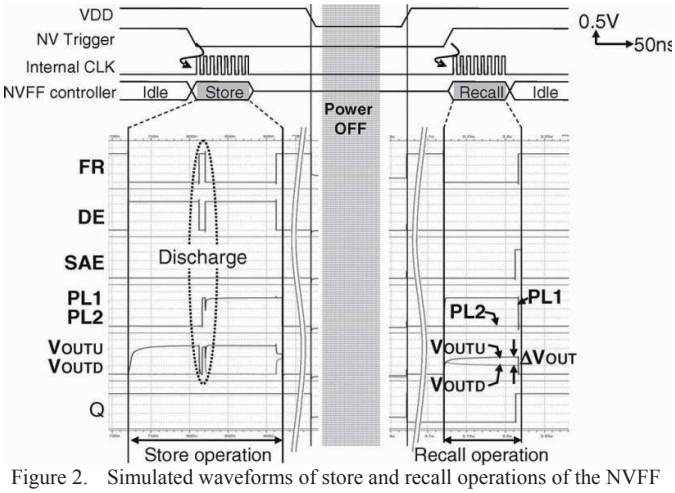


Figure 2. Simulated waveforms of store and recall operations of the NVFF at 1.5V power supply.

As a design example, the proposed NVFF is applied to 32bit CPU used in a vital sensor LSI. It demonstrates that the total power dissipation of the 32bit CPU during measurement of the heart rate is reduced to 13% of that of conventional one with area overhead of 64% using 130nm CMOS with $Pb(Zr,Ti)O_3$(PZT) thin films..

II. Non-Volatile Logic Circuit

A. General Structure

Fig. 1 shows the general structure of an NVL circuit, which consists of three components, NVFFs, a clock generator and a timing controller. The NVFF is designed on the basis of a conventional FF circuit with an FE-based non-volatile data storage circuit, in which a write driver and a comparator are controlled by a driver enabling signal DE and a sense-amplifier

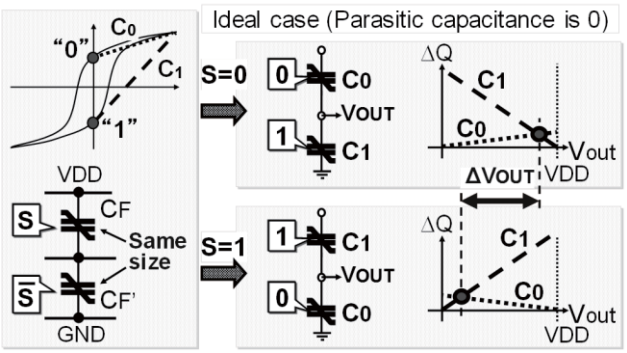


Figure 3. Capacitive coupling with complementary data storage.

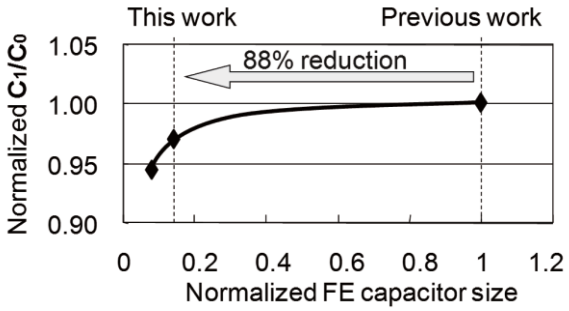


Figure 4. Relationship between FE capacitor size and C_1/C_0.

enabling signal SAE, respectively. These signals are controlled by the NVFF controller module, which is synchronized to a clock signal supplied by the clock generator. Fig. 2 shows a basic operation of the proposed NVL circuit. At power on state, the NVFF works as a conventional FF. The write driver is constantly at high-impedance state with two plate lines PL1 and PL2 grounded. Since the applied voltage across the FE capacitor is kept at OV, no power loss is induced by the FE capacitor. Therefore, in the logic operation, performance of the NVFF is equal to that of the conventional FF.

When a negative edge of the NV trigger signal is applied to the NVFF controller, the clock generator starts to generate clock signals for the timing controller, and the store operation is performed. In this operation, the clock signal for the FF is stopped by the NVFF controller. The write drivers are enabled by DE. Then, a positive voltage pulse is applied to PL1 and PL2 in the same way as an write operation of the conventional FeRAM [5], and state Q in the FF circuit is written into U-side and D-side of series-connected FE capacitors as pairs of complementary code $(S,\bar{S})$ and $(\bar{S},S)$, respectively. Before applying a positive voltage pulse to PL1 and PL2, FE capacitors are discharged to OV, because the electric charge on the FE capacitor causes a voltage overshoot, and leads damages in circuit devices. In the same way, a recall operation is enabled by the positive edge of the NV trigger. In this operation, a positive voltage pulse is applied to PL1 with PL2 grounded. Simultaneously, output voltage signals V_{OUTU} and V_{OUTD} are induced by capacitive coupling of U-side and D-side FE capacitors, respectively.

Fig. 3 shows relationship between an output voltage signal V_{OUT} and pairs of complementary code $(S,\bar{S})$. V_{OUT} becomes high V_1 for $S = 1$ or low V_0 for $S = 0$ because capacitance of the

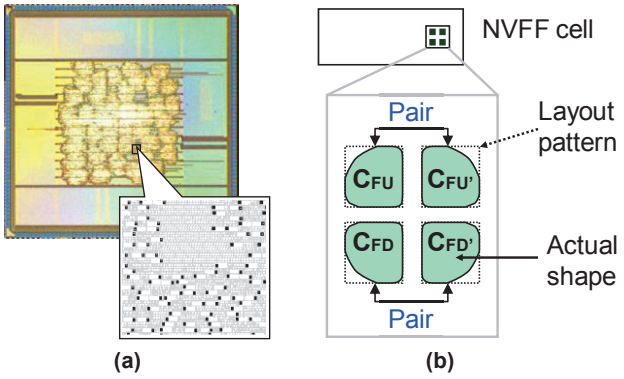


Figure 5. 1024 NVFFs-chained test chip. (a) Chip photograph. (b) Placement of FE capacitors in the NVFF cell and actual shape of FE capacitors.

Figure 6. Total energy disspated in store and recall operations.

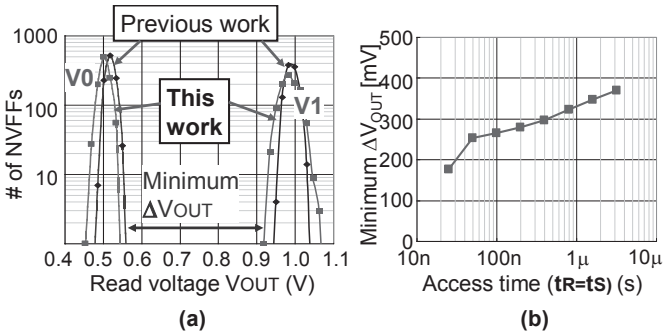


Figure 7. Read voltage V_{OUT} of the nvff. (a) V_{OUT} distribution of the test chip. (b) Relationship among minimum ΔV_{OUT} and access time.

FE capacitor becomes C_0 or C_1 depending on stored data S. Then, V_{OUTU} and V_{OUTD} are compared by the comparator, and the FF circuit is set or reset depending on the comparison result as shown in Fig. 2. In the proposed NVFF, coupled FE capacitor with complementary data storage [4] is introduced to realize the wide read voltage margin $\Delta V_{OUT} = V_1 - V_0$ with small FE capacitors. Theoretically, when parasitic capacitance on an intermediate node between two FE capacitors is negligible, ΔV_{OUT} is represented as $\Delta V_{OUT} = (C_1/C_0 - 1)/(C_1/C_0 + 1)V_{DD}$. Here, two FE capacitors are same size. Fig. 4 shows that 88% reduction of FE capacitor size causes only 3% decrease of C_1/C_0, that is, FE capacitor size can be reduced until 88% with maintaining the magnitude of ΔV_{OUT}.

B. Evaluation of Non-Volatile Flip-Flop

Characteristic of the proposed NVFF is evaluated by using an NVFF test chip which consists of two shift registers of 512 NVFFs. Fig. 5(a) shows a test chip using 130nm CMOS with

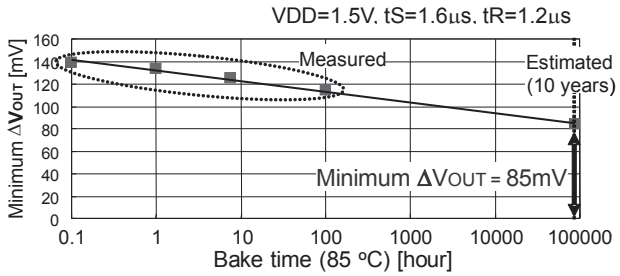


Figure 8. Minimum of read voltage margin ΔV_{OUT} after 10 years equivalent

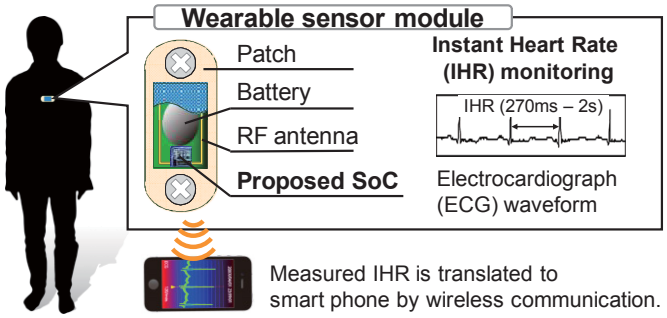


Figure 9. Wearable healthcare application.

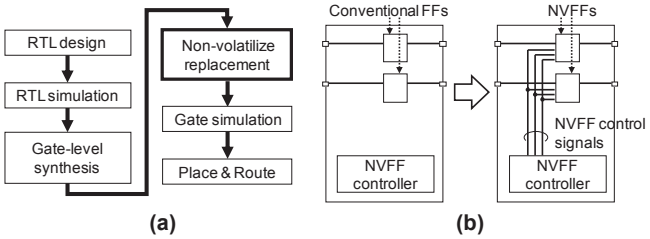
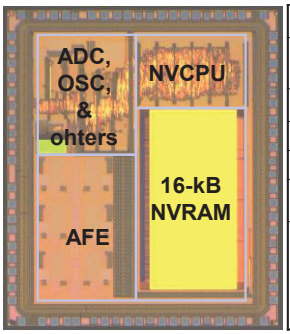


Figure 10. Design flow of an NVL circuit. (a) Design flow chart. (b) Nonvolatile replacement.

$Pb(Zr,Ti)O_3$(PZT) thin films in which all NVFFs are randomly placed on a logic circuit. In the NVFF, two pairs of series-connected FE capacitors are arranged as 2 by 2 array so as to prevent variety of actual FE capacitor size which depends on the density of the FE capacitor as shown in Fig. 5(b).

The total energy consumption of the store and recall operations becomes 2.4pJ per the NVFF as shown in Fig. 6, which is 88% lower than that of the previous NVFF. Fig. 7(a) and (b) show V_{OUT} distribution of the test chip, and relationship among minimum ΔV_{OUT}, t_R and t_S , respectively. The randomly placed FE capacitors have minimum V_{OUT} of 240mV at V_{DD} = 1.5V, In case of t_S = 1.6µs and t_R = 1.2µs, the minimum ΔV_{OUT} is still larger than 85mV after being baked at 85 °C for 10 years as shown in Fig. 8, which is large enough to perform reliable store and recall operations. In addition, in case of t_S = 170ns and t_R = 160ns, the retention capability of 10 hours at 85 °C is also confirmed with the test chip. Therefore, an access speed of FE capacitors can be adaptively controlled according to required retention time, which becomes 1.6µs for 10-year data retention, and 170ns for 10-hour data retention.



Technology	0.13μm CMOS + PZT	
Supply voltage	1.5V (Logic, Memory, Analog), 3.0V (I/O)	
Chip area	3.7x4.3mm2	
Logic freq.	24MHz	
On chip memory	16kB NVRAM	
Processor	Non-volatile 32-bit CPU	
Total power of processor (Heart-beat logging)	w/o power control	0.59uW @RT
	with power control	0.07uW @RT

Figure 11. Photograph and specifications of a vital sensor chip.

TABLE I. NVL COMPARISON.

	ISSCC'13 [8]	Khanna2014 [9]	This work	
Supply voltage	1.5V	1.5V	1.5V	
Store and recall energy	3.4pJ	3.75pJ	**2.4pJ**	**2.34pJ**
Store time	2.2us	0.32us	1.64us	0.17us
Recall time	2us	0.384us	1.23us	0.16us
Data retention	-	-	>10 years	> 10 hours
Design example	FIR filter	32bit core	32bit Cortex-M0	
Area overhead (Gate counts)	49%	-	64%	
Clock frequency in a logic operation	5MHz	8MHz	24MHz	

III. Normary-Off Microprocessor for Wearable Healthcare Application using Non-Volatile Flip=Flop

As a design example, the proposed NVFF is applied to 32-bit CPU in a vital sensor LSI for wearable healthcare applications, which is used for an Instantaneous Heart Rate (IHR) monitoring on the human body [6] as shown in Fig. 9.

A. Design Flow

The design flow of the proposed NVL circuit is same to that of the conventional one except for non-volatile replacement as shown in Fig. 10(a). A given RTL specification is synthesized into a gate net list together with the NVFF controller module. Then, all conventional FFs in a target logic module are replaced by NVFFs. At the same time, signal wires used to transit NVFF control signals are connected to the NVFF controller and NVFFs as shown in Fig. 10(b). Since the performance of the NVFF is the same as that of the conventional one in a logic operation, timing mismatch will not occur after the NV replacement.

B. Implementation Results of Normary-Off Microprocessor

Fig. 11 shows the vital sensor LSI for wearable healthcare applications [7], which consists of an electrocardiogram (ECG) sensor, the 32-bit CPU core with NVFF, and a 16-Kbyte FE-based non-volatile memory (NVRAM) [8] for data and instruction. Because the frequency range of vital signals is low, both the standby power reduction and sleep time maximization is important to system level power reduction. The operating frequency of the CPU core and memory is 24 MHz, whereas the operating frequency of sensing blocks is 32 kHz. Slow signals in the 32 kHz domain are synchronized at the low-speed bus to the 24 MHz domain. Standby current of the entire 24 MHz domain including an on-chip 24-MHz oscillator can

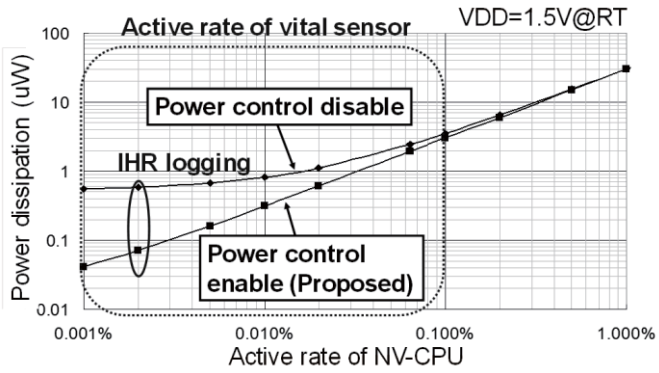


Figure 12. Relationship between power dissipation and active rate.

be cut when the state of CPU core transits to deep sleep. Then the data in the memory and register values of CPU core in the NVFF are stored sequentially to ferroelectric capacitors. The data and register values will be recalled if the interrupt occurs from the 32 kHz domain. Fig. 12 shows the relationship between the power dissipation and the active rate of the microprocessor. The measurement result shows that the non-volatile microprocessor with proposed NVFFs is suitable for vital sensor applications.

In this implementation, the store and recall times of NVFF are set to 170ns and 160ns, respectively, because a period of standby state is about 1s. Since the standby power of 32bit CPU is reduced to zero by turning off the power supply during standby state, its total power dissipation is reduced to 13% in comparison with that without a power control. Table I summarizes a comparison of this work with other NVL technology reported so far.

References

[1] S. Sugibayashi, et al., "Nonvolatile magnetic flip-flop for standby-power-free SoCs," IEEE CICC, 2008, pp.14-4-1-14-4-4.

[2] Y. Fujimori, et al., "Ferroelectric non-volatile logic devices," *Integrated Ferroelectrics*, Vol .56, pp.1003–1012, 2003.

[3] H.Kimura, et al., "Highly Reliable Non-Volatile Logic Circuit Technology and Its Application," *Proc. of IEEE ISMVL*, 2013, pp.212–218.

[4] H. Kimura, et al., "Complementary ferroelectric-capacitor logic for low-power logic-in-memory VLSI," *IEEE J-SSC*, Vol. 39, No. 6, pp.919–926, 2004.

[5] A. Sheikholeslami, et al., "A Survey of Circuit Innovations in Ferroelectric Random-Access Memories," Proc. IEEE, Vol .88, No.5, pp.667-689, 2000.

[6] Y. Nakai, et al., "Noise Tolerant QRS Detection using Template Matching with Short-Term Autocorrelation," *Proc. of IEEE EMBC*, pp. 34–37, Aug. 2014.

[7] S. Izumi, et al., "A 6.14μA Normally-Off ECG-SoC with Noise Tolerant Heart Rate Extractor for Wearable Healthcare Systems," *Proc. of IEEE BioCAS*, pp. 280–283, Oct. 2014.

[8] T. Nakagawa, et al., "A Low Power 6T-4C Non-volatile Memory using Charge Sharing and Non-precharge Techniques," *Proc. of IEEE ISCAS*, pp. 2904–2907, May 2015.

[9] M. Qazi, et al., "A 3.4pJ FeRAM-enabled D flip-flop in 0.13um CMOS for nonvolatile processing in digital systems," *IEEE ISSCC*, 2013, pp.192-193.

[10] S. Khanna, et al., "An FRAM-Based Nonvolatile Logic MCU SoC Exhibiting 100% Digital State Retention at VDD=OV Achieving Zero Leakage With 400-ns Wakeup Time for ULP Applications," *IEEE J-SSC*, Vol. 49, No.1, pp.95-106, 2013.