A 40-nm 0.5-V 12.9-pJ/Access 8T SRAM Using Low-Power Disturb Mitigation Technique

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Abstract - This paper presents a novel disturb mitigation technique which achieves low-power and low-voltage SRAM. Our proposed technique consists of a floating bitline technique and a low-swing bitline driver (LSBD). We fabricated a 512-Kb 8T SRAM test chip that operates at a single 0.5-V supply voltage. The proposed technique achieves 1.52-pJ/access active energy in a write cycle and 72.8-μW leakage power, which are 59.4% and 26.0% better than the conventional write-back technique.

I Introduction

As process technology has been scaled down, it has become much more difficult to realize a stable bitcell design in a 6T SRAM due to the tradeoff between read and write margins [1]. An 8T bitcell with a dedicated read port is proposed to neglect the 6T's read margin, which achieves low-voltage operation in nature. The separation of read and write ports frees the bitcell design of the read/write tradeoff; the area of the 8T cell is expected to be smaller than that of the 6T cell in a future process [2]. Although low-voltage and high-yield 8T SRAMs under 1.0-V operation are proposed [3–5], the power per operation cycle (= energy) is larger than that in 6T SRAMs [5–7]; this is because an assist circuit needs to be implemented to avoid the disturb (= half-select) problem. Fig. 1 shows the tendency of the power per cycle among recent SRAMs. Our research object is to achieve a low-voltage and low-energy SRAM: 0.5-V and sub-100 μW/MHz/Mb (= pJ/access) operation is the target.

II. Proposed Disturb Mitigation Technique

To reduce the extra power for the disturb, we propose a new disturb mitigation technique: (1) a floating write bitline (WBL) with precharge-less equalizer, and (2) a low-swing bitline driver (LSBD) with nMOS pull-up transistors for the WBLs.

The proposed 8T SRAM employs a hierarchical read bitline (RBL) structure and the number of cells per RBL is 16 for stable read operation, as illustrated in Fig. 2. In the read operation, a read enabling (RDE) signal is activated, and then a global RBL (GRBL) is discharged when an RBL is pulled down.

In the proposed technique, the active power in the write cycle is reduced and the leakage power in the read/write operation is also improved. In the half-selected cells, the column line enabling signals (CLEs) are low in the unselected columns and the driver disable signal (DRN) is pulled down in the selected row. Thus, the LSBD pulls up or down each WBL by the nMOSes.

Fig. 3 shows the waveforms in the write cycle assisted by the proposed technique. In the proposed technique, the WBLs are floating not only in a standby mode but also in an activated mode, and their voltage is at an intermediate voltage between the ground and supply voltage. After the LSBD pulls up a WBL (or WBLN) with an nMOS and the WBL (or WBLN) level goes up to "VDD – Vtn", some disturb current flows through the access gate from a "high" internal node. However, the "high" node is not flipped and keep the original datum because the other internal node is strongly grounded. Consequently, the LSBD has an advantage to reduce the active power without any area overheads: The half-selected cell is not flipped and the WBL swing is small in the write cycle. To save more power, the RDE is sustained low in the write operation and the GRBL does not swing in the proposed disturb mitigation technique. The delay penalty derived from the GRBL is also reduced.

III. Measurement Results and Conclusion

We fabricated a 512-Kb 8T SRAM macro using a 40-nm CMOS bulk process (Fig. 4), which characteristics are summarized in Table I. The 8T bitcell area is 0.706 μm^2 using a logic rule. The transistor width of an access gate is doubled to enhance the write margin while the others are minimum sizing.

Figs. 5(a) and 5(b) illustrate that the measured leakage power and active write energy are improved by 26.0% and 59.4% at the supply voltage of 0.5 V. The active energy is 1.52 pJ/access. The total energy is 12.9 pJ/access when the read and write cycles are fifty-fifty at 0.5V.

Acknowledgments

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References

[1] R. Heald, et. al., IEEE ICCAD, pp. 347-352, 2004.
[2] Y. Morita, et al., VLSI Cir. Digest, pp. 256-257, 2006.
[3] M. E. Sinangil, et. al., IEEE ESSCIRC, pp. 282-285, 2008.
[4] L. Chang, et. al., VLSI Cir. Digest, pp. 252-253, 2007.
[5] K. Nii, et. al., VLSI Cir. Digest, pp. 212-213, 2008.
[6] K. Takeda, et. al., VLSI Cir. Digest, pp. 101-102, 2010.
[7] M. Khellah, et. al., ISSCC Digest, pp. 2572-2581, 2006.

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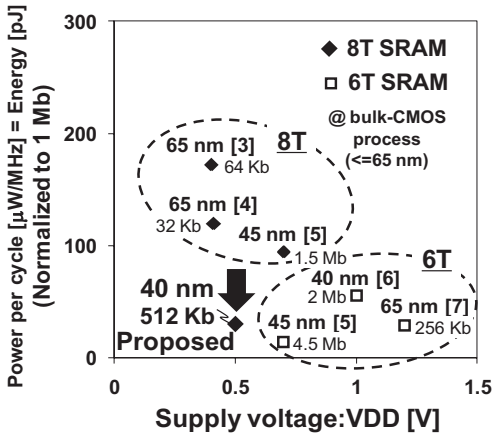


Fig. 1. Supply voltage versus energy among low-power bulk-CMOS SRAMs [3–7].

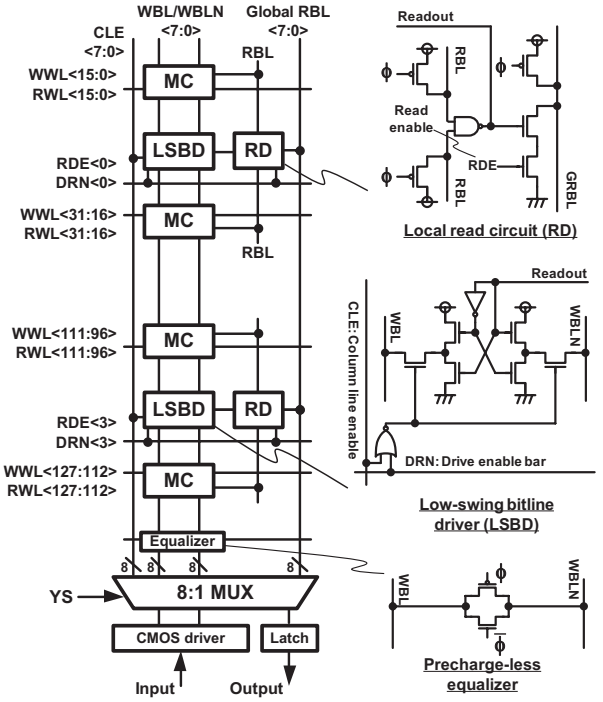


Fig. 2. Local cell array with the proposed circuitry. “MC” signifies “single-ended 8T memory cell”.

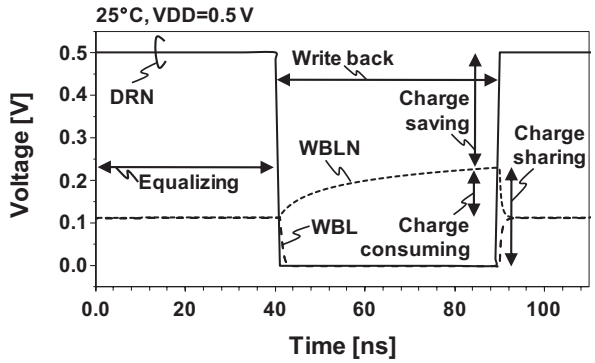


Fig. 3. Waveforms of the half-selected cell assisted by the proposed technique.

TABLE I
Features of the test chip

Technology	40-nm bulk CMOS
Macro size	0.723 mm × 1.010 mm
Macro configuration	512 Kb(16 Kb × 4 × 8), 16 bits/word
Cell size	0.706 μm^2 (logic rule)
# of cells / BL	16 (RBL), 128 (WBL)
Cell density	701 Kb/mm^2
Write active energy	1.52 μW/MHz @ 0.5 V, 6.25MHz
Total energy (R/W=50/50)	12.9 μW/MHz @ 0.5 V, 6.25MHz
Access time	160 ns @ 0.5 V, 4.5 ns @ 0.8 V

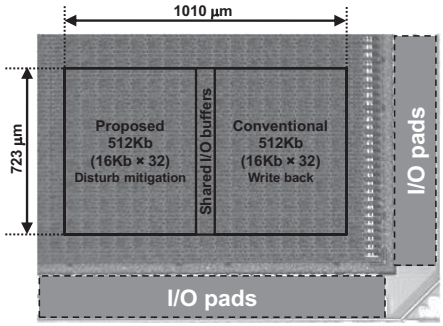
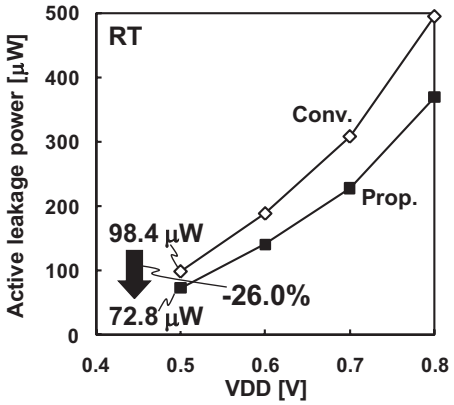
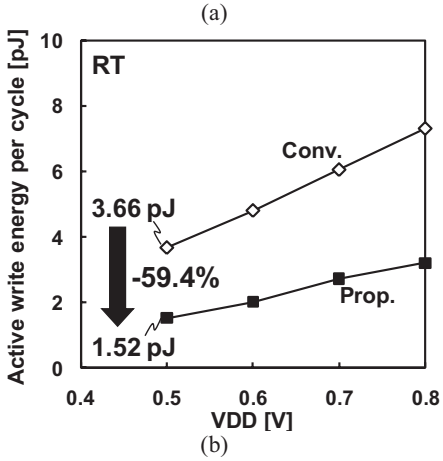


Fig. 4. Micrograph of the test chip: 1 Mb SRAMs include the proposed and conventional technique.



(a)



(b)

Fig. 5. Measured (a) leakage power and (b) write active energy.