An Low-Energy 8T Dual-Port SRAM for Image Processor with Selective Sourceline Drive Scheme in 28-nm FD-SOI Process Technology

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***Abstract*— This paper presents a low-energy and low-voltage 64-kb 8T dual-port image memory in a 28-nm FD-SOI process technology. Our proposed SRAM adopts the selective sourceline drive (SSD) scheme and the consecutive data write technique for improving active energy efficiency at the low voltage. We fabricated a 64-Kb 8T dual-port SRAM in the 28-nm FD-SOI process technology; the test chip exhibits 0.48 V operation and an access time of 135 ns. The energy minimum point is at a supply voltage of 0.56 V and an access time of 35 ns, where 265.0 fJ/cycle in write operation and 389.6 fJ/cycle in read operation are achieved; these factors are 30% and 26% smaller than those in the 8T dual-port SRAM with the conventional selective sourceline control (SSLC) scheme, respectively.**

Keywords—Image Memory, Multi-Port SRAM, 8T SRAM, FD-SOI, 28-nm SRAM, Consecutive Access, Low power.

I. INTRODUCTION

Internet of Things (IoT) aims high-quality image recognition that has been extended to various fields such as automatic driving systems, robot vision, and augmented reality systems with fine resolution. The image resolution enhancement leads to large capacity, large area, and high power consumption because of the increasing amount of image data. Power consumption in SRAM dissipates 43% of a whole image processor in a 65-nm CMOS process [1]. For the IoT devices handling image information, more energy efficient SRAM will be expected.

Fully Depleted SOI (FD-SOI) technology is promising to provide high-speed and low-voltage SRAM [2]. A 28-nm FD-SOI has a fully depleted transistor with an ultra-thin silicon body and a buried oxide (BOX) layer, giving them excellent electrostatic control. Therefore, it brings stable features at low-voltage operation. The BOX layer reduces the leakage current by controlling the electrical flow from a source node to a drain node in a transistor. Moreover, the BOX layer reduces the parasitic capacitance between the source node and the drain node. This feature of the 28-nm FD-SOI enables the production of ultra-low-power SRAMs [3–5].

Input data for image processing are stored temporarily in SRAM. In an image processor, many processing cores access the SRAM for multi-thread processing. Demands for multi-port SRAM have been increased to accommodate high-speed and low-power image processing. The multi-port SRAM is suitable for parallel operation; it improves the total chip performance. Parallel processing is the key for real time image applications, in which the embedded memories with multi access-ports are needed [6]. To date, multiport SRAMs that support simultaneous write and read operations have been proposed for use as image processors [7–8].

An 8T 1-read/1-write (1R1W) dual-port SRAM is typically used for leveraging disturb-free access due to the dedicated read port [9]. Thus, 8T dual-port SRAM with lower active/standby powers have become more crucial than ever. An read port of 8T dual-port SRAM employs a sourceline (SL) as a footer line, which are shared in the same row addresses to perform the low-power operation. This SRAM reduces leakage current through unselected read bitlines (RBLs). The RBL is, however, discharged slightly in the unselected columns because the SL is floating in the conventional scheme, which degrades energy efficiency [10]. To completely cut off the RBL discharge, we proposed novel footer circuitry.

In this paper, we design a 28-nm FD-SOI 8T dual-port SRAM for a low-energy image processor and compare it to the conventional one. High energy efficiency of sub-pJ/cycle in the proposed SRAM will be exhibited.

II. PROPOSED DUAL-PORT SRAM

A. Selective sourceline drive (SSD) scheme

Figure 1 illustrates the memory matrix of the conventional 8T 1R1W dual-port SRAM with the selective sourceline control (SSLC) scheme [10]. An only selected local read bitline (RBL) is connected to a global RBL by a multiplexer in the conventional structure whereas SLs of non-selected read ports becomes floating. The floating node of the non-selected SL is charged up when a readout datum is “0” on a local RBL. The voltage of the local RBL is not a full swing due to the cutoff SL, but it is unnecessary and consumes certain energy in the conventional scheme.

Figure 2 illustrates the concept of the proposed selective sourceline drive (SSD) scheme. It has a pair of nMOS switches (M1 and M2), an inverter and an OR gate, as a footer circuit in

every column. Those switches keep the SL on the ground for the selected column, or drive the SL to VDD−Vth (Vth is a threshold voltage of M1) when the column is not selected. In the standby mode, all the SLs are grounded to prepare for upcoming random read access.

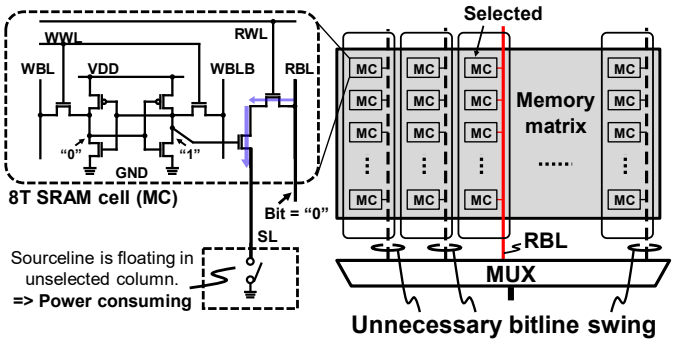

Fig. 1. Conventional 8T memory matrix with SSLC scheme. SLs are floating due to single nMOS switch; it consumes unnecessary energy.

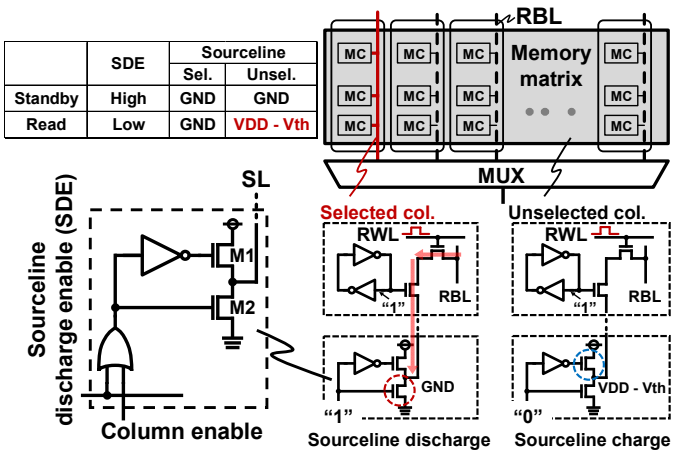

Fig. 2. Concept of proposed selective sourceline drive (SSD) scheme in read operation.

The right side of Figure 2 also depicts the behavior of the proposed SSD scheme. In the read operation, the sourceline discharge enable (SDE) signal for all the columns is "0". In the selected column, the output of the OR gate becomes high and M2 is activated for readout. At this time, the charge/discharge power consumes on the selected local RBL because the SL at the selected column is grounded. In the unselected column, the output of the OR gate is low and M1 drives the SL to VDD−Vth. In this situation, there is no read current flowing through the local RBL. It is noteworthy that the area overhead is only 0.8% of a whole memory macro in our design although the proposed SSD circuit must be implemented in every column.

Figure 3 portrays simulated operating waveforms during read cycles. Figure 3(a) shows the waveform of the read wordline (RWL) commonly used in the conventional SRAM and the proposed SRAM. Figure 3(b) shows the waveforms of the RBL and the SL in the conventional SSLC read scheme. The charge/discharge on the RBL is not a full swing but consumes unnecessary power in every cycle although the columns are unselected.

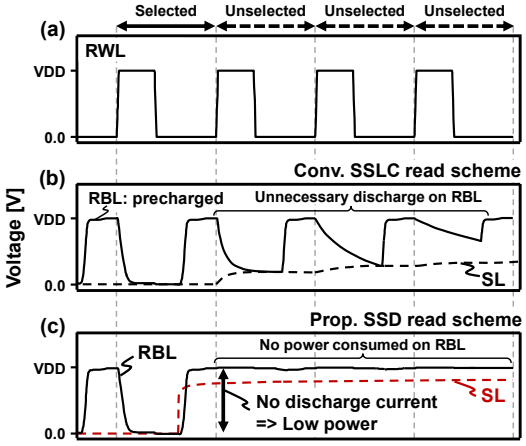

Fig. 3. Operating waveformes of proposed SSD scheme in read operation.

Figure 3(c) portrays the waveforms of the unselected read bitlines in the proposed SSD scheme. The SL is driven to VDD−Vth by the nMOS switch (M1). In terms of power consumption, the SSD scheme is better than the conventional SSLC scheme; there is no voltage swing on the local RBL in the proposed SSD scheme. Note that the output voltage amplitude of the SL is restricted to VDD−Vth because it minimizes the dynamic power consumption of the driver switches (M1 and M2) and its leakage current flowing through M2. Thus, the proposed SSD scheme eliminates the unnecessary read current in the unselected columns.

B. Consecutive memory access in video processing

Image data such as people or landscape reflects luminance information; it has similar brightness in adjacent pixels, with similarity of data pattern. Figure 4 presents the switching possibility of a readout bit between a present pixel and a next pixel. The maximum switching possibility is 50% on the least-significant bit (LSB = 1-st digit), which means the value of the LSB is random and this is reasonable. The most-significant bit (MSB = 8-th digit) has a switching possibility of 10% or less because it has much stronger correlation between adjacent pixels. Therefore, in the consecutive accesses, it is better to map their addresses along the row direction as presented in Fig. 5(a), where a column address is not changed very often.

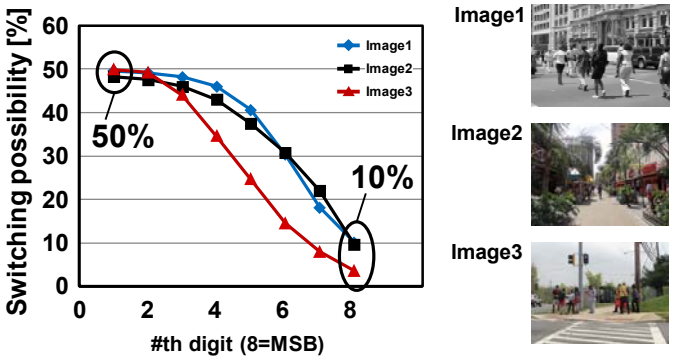

Fig. 4. Switching possibility in image data.

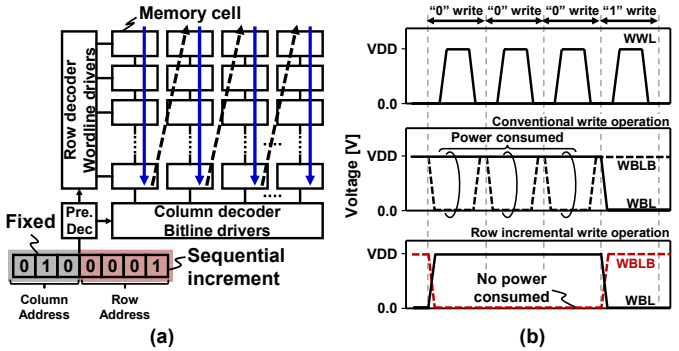

Fig. 5. Consecutive memory access in video processing: (a) Block diagram and (b) waveforms in write operation.

Figure 5(b) shows the waveform of the proposed SRAM in write operation. By virtue of the precharge-less and incremental write operation, the proposed SRAM reduces the write energy; the charge/discharge on a pair of write bitlines (WBL and WBLB) is consumed only when a write datum is changed. The consecutive write of the same datum consume less energy because the proposed dual-port SRAM has a dedicated write port and does not need a precharge scheme on the WBLs. However, it incurs the well-known half-select problem along the write wordline (WWL). The divided wordline structure is therefore adopted only for the write port to avoid the half-select problem [11]. Note that the read port has the common interleaving structure and does not have divided RWLs; this is because an image processor often requires a larger number of read ports and is given a serious impact on its area.

III. Chip Implementation and Measurement Results

We fabricated a 64-kb 8T dual-port SRAM macro in a 28-nm FD-SOI process technology. Figure 6 shows a test chip micrograph. The proposed 64-kb macro consists of 2 × 32-kb sub-blocks, and the macro size is 242 x 189 μm^2 (= 0.045 mm^2). Figure 7 presents a measured read Shmoo plot of the designed SRAM. In the proposed SRAM, the operation of the single-ended read port limits its performance because the write has more operating margin. We verified that it can operate at a supply voltage of 0.48 V and an access time of 135 ns (= 7.4 MHz) at a room temperature (=25 degree). The operating point that achieves the minimum energy per cycle is at a supply voltage of 0.56 V and a cycle time of 35 ns (= 28.6 MHz).

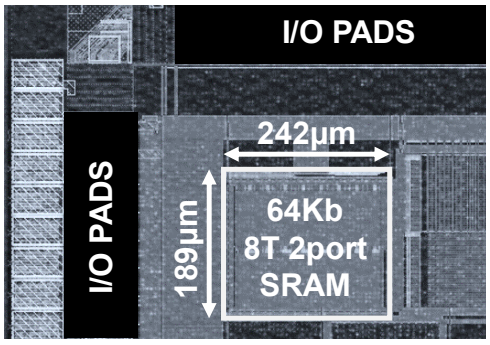

Fig. 6. Test chip photograph.

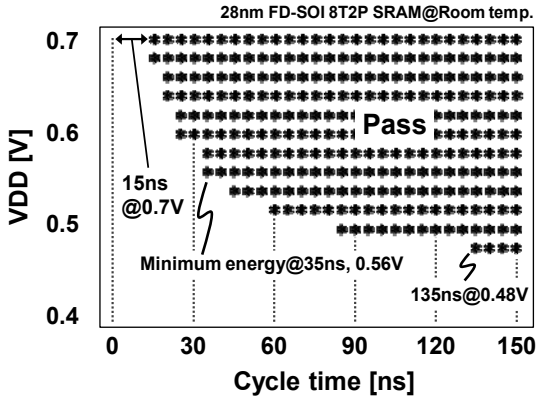

Fig. 7. Measured Shmoo plot in read operation.

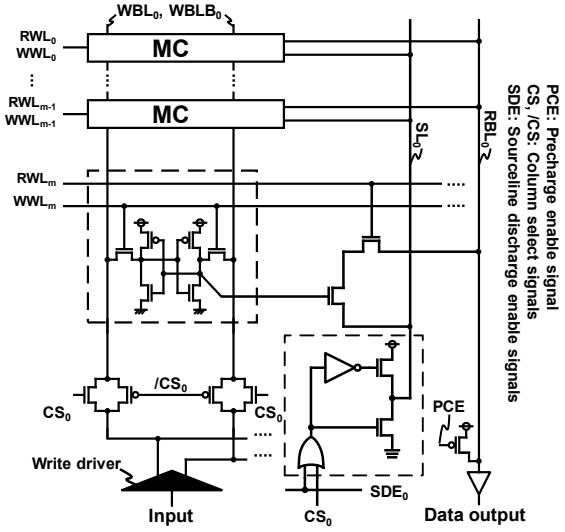

Fig. 8. Schematic of proposed 8T dual-port SRAM with SSD scheme.

Figure 8 portrays a schematic of the proposed 8T dual-port SRAM array with the SSD scheme. Figure 9 shows the simulated and measured active/leakage energy comparisons between the conventional SSLC scheme and the proposed SSD scheme in read operation. It is noteworthy that the both read circuits must have the RBL precharge scheme because of the single-ended read ports. In the read operation, the test patterns of the "ALL0" and "ALL 1" mean consecutive "0" and "1" read operations of the incremental row address accesses, respectively. The checkerboard patterns using the incremental row address (CKB X+) have 50% "0" and 50% "1" data, whose energies is in the middle between "ALL0" and "ALL1". In the CKB using the incremental column address (CKB Y+), the column address is changed at every cycle. The energy comparison demonstrates that the proposed SSD scheme improves the read energy by 26% on average, which is 389.6 fJ/cycle.

In the write operation, the proposed 8T dual-port SRAM does not require the precharge on the WBLs. In addition, its WWL has the divided structure. Therefore, the proposed SRAM can reduce the needless write energy due to the charge/discharge in the half-selected columns. The measured "0" and "1" write energies are 196.2 fJ/cycle and 215.2

fJ/cycle, respectively. Figure 10 portrays the impact of the incremental write operation for the write energy saving. As a counterpart, the write energy becomes 382.0 fJ/cycle in the consecutive column access in the CKB test pattern. In the monochrome Image1, the write energy is reduced by 29% while, in the color Image3, that reaches 32% saving; it is advantageous that the image has high similarity among entire pixels. In Image3, the write energy is 258.0 fJ/cycle, and the write energy achieves 265.0 fJ/cycle on average, which is 30% lower than that in the consecutive column access.

Therefore, our proposed 8T dual-port SRAM with the SSD scheme can reduces both of the read and write energies, and is suitable for low-power image processing devices. TABLE I summarize the characteristics of the SRAM test chip.

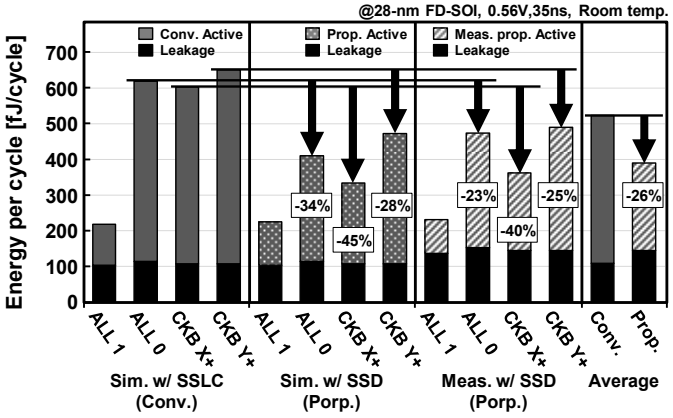

Fig. 9. Simulated and measured energy comparisons between conventional SSLC scheme and proposed SSD scheme in read operation.

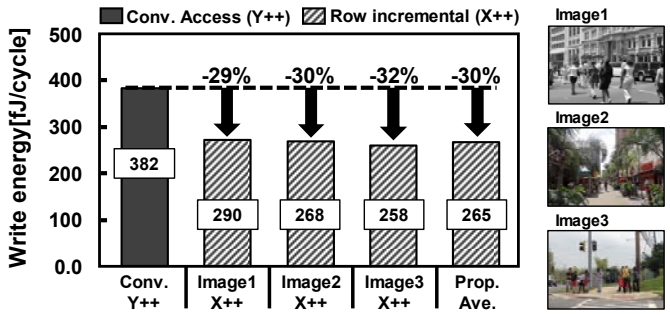

Fig. 10. Impact of incremental accesses in write operation.

TABLE I. TEST CIHP FEATURES

Technology	28-nm FD-SOI
Supply voltage	0.48-0.7V (Memory macro)
	1.8V (I/O)
Chip area	1.0x1.0mm^2
Macro size	189x242μm^2
Macro configulation	64Kb (32Kb X 2), 16bits/word
Cell size	0.291x1.457μm^2
Frequency	7.4MHz@0.48V, 66.7MHz@0.7V
Read active energy	389.6fJ@0.56V, 28.6MHz, RT
Write active energy	265.0fJ@0.56V, 28.6MHz, RT

IV. SUMMARY

We presented an 8T dual-port SRAM with the selective sourceline drive (SSD) scheme for an image processor. Our proposed SRAM drives the sourceline (SL) to VDD−Vth at unselected columns in read operation and exploits the consecutive row accesses in write operation for improving energy efficiency at low voltage. We fabricated a 64-Kb 8T dual-port SRAM in a 28-nm FD-SOI process technology. The test chip exhibits 0.48 V operation at an access time of 135 ns. The energy minimum point is a supply voltage of 0.56 V at a frequency of 28.6 MHz, at which 265.0 fJ/cycle in the write operation and 389.6 fJ/cycle in the read operation are achieved.

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