A 40-nm 640-μm² 45-dB Opampless All-Digital Second-Order MASH ΔΣ ADC

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Abstract—**This paper presents a second-order ΔΣ analog to digital converter (ADC) operating in a time domain. In the proposed ADC architecture, a voltage-controlled delay unit (VCDU) converts an input analog voltage to a delay time. Then the number of clocks output from a gated ring oscillator (GRO) is counted up during the delay time. Because no switched capacitor or opamp is used, the proposed ADC can be implemented in a small area and at low power. For the same reason, it has process scalability: it can be in keeping with Moore's law. A time error is propagated to the second GRO by a multi-stage noise-shaping (MASH) topology, which provides second-order noise-shaping. In a standard 40-nm CMOS process, a SNDR of 45 dB is achievable at an input bandwidth of 3 MHz and a sampling rate of 100 MHz, where the power is 583.2 μW. Its area is 640 μm².**

I. INTRODUCTION AND CONVENTIONAL STUDIES

To produce competitive information and communication equipment, designing high-performance and low-cost chips at low power is needed. Scaling in process technology has enabled miniaturization of transistors. Consequently, the number of transistors can be increased. Functionality in a digital system has developed rapidly at low cost. The low-power feature is also achieved by reducing the supply voltage.

For analog circuits, however, it is difficult to benefit from scaling. Operating at low supply voltage yields a small dynamic range. Linearity becomes degraded, and a gain in an opamp is lowered. To compensate for these disadvantages, transistor sizing and the area of passive components are ever-increasing. Consequently, a mixed-signal chip comprising digital and analog circuitry can achieve neither low cost nor low power in the recent advanced process. An analog-to-digital converter (ADC) is a critical component in mixed-signal circuits, in which opamps and capacitors—particularly in a ΔΣ ADC—prevent merits derived from scaling.

Several ADCs operating in a time domain have been researched recently. One ADC uses two-ring oscillators comprising inverters and voltage-controlled delay units (VCDUs) [1]. The VCDUs are put in the inverter chains, where an analog input voltage is fed to only one VCDU. Depending on the value of the analog input voltage, the pulse in this ring oscillator is delayed as a function of the VCDU. The delay time appears behind another ring oscillator with no input voltage. In other words, a phase delay between the ring oscillators is sampled as a datum in each period. Then, a 1-bit time-to-digital converter (TDC) with a data flip-flop (DFF) digitizes the phase delay. This ADC architecture inherently has a first-order noise-shaping characteristic, because the output from the TDC is fed back to the ring oscillator via the VCDU, and it acts as an integrator. However, it is extremely difficult, virtually impossible, to match the frequencies in the two ring oscillator, which incurs a timing error although a signal is handled in the time domain. Another issue is nonlinearity in the VCDU. To make matters worse, the mismatch between the two VCDUs produces adverse effects. Consequently, implementing a higher-order ADC with the VCDUs or even first-order ADC implies a difficult design.

Instead of the VCDU, a voltage-controlled oscillator (VCO) is used as an ADC [2]–[4], in which a VCO frequency varies depending on the analog input voltage. A multi-bit quantizer counts up rising edges of the oscillation. This mechanism also has a first-order noise-shaping characteristic. A higher-order ΔΣ ADC can be achieved using active filters with opamps and other analog elements. This type of ADC, however, presents disadvantages; the VCO has nonlinearity like the VCDU-type ADC in terms of a voltage-to-frequency conversion. Designing higher-order ADC requires opamps and other analog elements that are unsuitable to advanced processes.

II. PROPOSED OPAMPLESS ALL-DIGITAL MASH ADC

In our proposed design, we also use a time delay as a signal instead of a voltage signal; only one VCDU is implemented to avoid the unwanted mismatch. The VCDU converts an analog input signal to a delay time. Then it is forwarded to a TDC and digitized. The TDC is one of the most active research areas because it is suitable to process scaling; we can apply an up-to-date TDC technique to the analog to digital conversion.

Figure 1 portrays a gated ring oscillator TDC (GRO TDC). The GRO TDC has been studied as a TDC that uses a ring oscillator comprising gated inverters [5]. A pulse width (T_{in}) is

input to the GRO TDC as a time-varying analog datum. During T_{in}, the GRO TDC quantizes it with the counter by counting up the clock, CK. Then the datum is shown as a discrete value. It is noteworthy that this GRO TDC also has a first-order noise-shaping characteristic, but in the literature, its function as the first-order modulator is merely exhibited; it is not completed as an ADC.
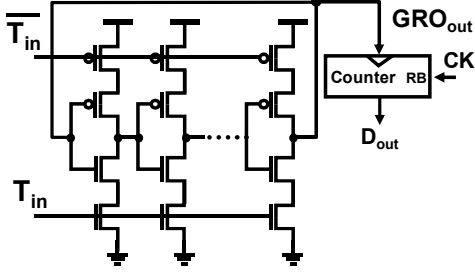

Figure 1   Gated ring oscillator time-to-digital converter (GRO TDC).

Figure 2 depicts the mechanism of the first-order noise shaping. The quantization error, $QN[1]$, is propagated to the next pulse ($T_{in}[2]$) by holding the waveform of GRO_{out}. In the proposed ADC architecture, the quantization error can be propagated to the next-stage TDC in a multi-stage noise-shaping (MASH) manner. This MASH-type $\Delta\Sigma$ modulator achieves high accuracy without opamps, analog elements, or capacitors that occupy a large area; a low-cost and low-power ADC is possible. Because all control circuits can be implemented using a standard cell library, the proposed ADC has scalability to the advanced process.
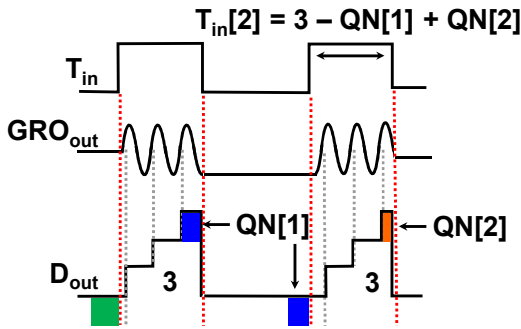

Figure 2   First-order noise-shaping characteristic in GRO TDC.

A. *Second-order MASH ΔΣ ADC*

As shown in Figure 3, the second-order MASH ADC generally has first-order $\Delta\Sigma$ modulators, quantizers, and a subtractor for quantization error propagation. Figure 4 is our proposed architecture, which employs the GRO TDCs as $\Delta\Sigma$ modulators. The counters are quantizers. The DFF propagates the quantization error to the next stage. As far as we know, this type of MASH $\Delta\Sigma$ ADC only with TDCs but without opamps has not been presented yet.

B. *Quantization error propagation*

In Figure 5, T_{in} signifies the input pulse width into the GRO, GRO_{out} stands for the output of the oscillation, D_{out} denotes the number of clocks, and T_{QN} represents a period of the GRO's oscillation that includes the discrete datum, D_{out},

and quantization error, QN. As the figure shows, the quantization error is preserved in the GRO's oscillation; the DFF detects the first rising edge of the GRO_{out}, and outputs T_{QN} including QN. It is possible to obtain QN by subtracting D_{out} from T_{QN}. Consequently, the quantization error can be forwarded to the next GRO, and the higher-order MASH ADC is achievable.
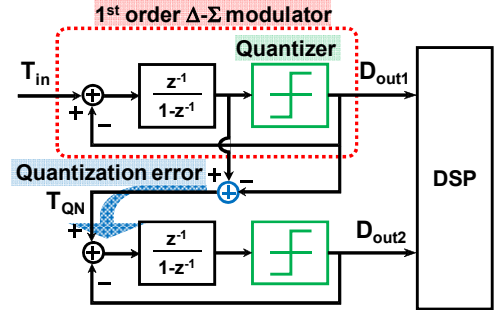

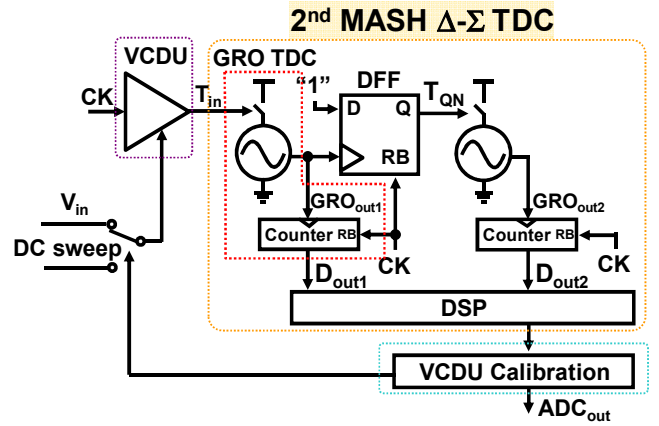Figure 3   Diagram of second-order MASH ADC.

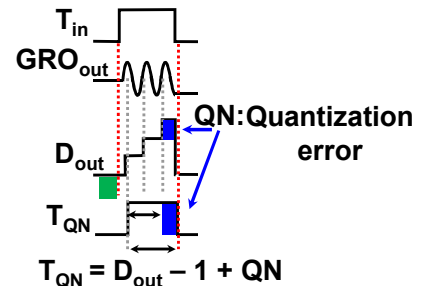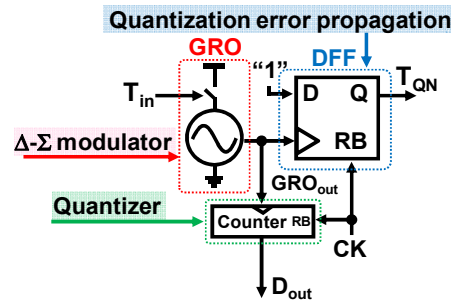Figure 4   Proposed second-order MASH ADC architecture.

Figure 5   Concept of quantization propagation in time domain.

C. Voltage-controlled delay unit (VCDU)

In [1], a current-starved inverter presented in Figure 6(a) is used as a VCDU. When ϕ_{in} is "low", the pMOS transistor, M1, sources a current to the gate of the inverter, and precharges it to the supply voltage. Then it is discharged in the opposite phase. The current-sink nMOS transistor, M3, controlled by an analog input voltage (V_{in}), draws the charge; the discharging speed depends on V_{in}. This is the basis of the voltage-to-delay conversion. The diode-connected nMOS transistor, M4, draws a certain current, which avoids producing an infinite delay even if V_{in} is 0 V. In this conventional VCDU, however, the node voltage of V_X can not be recovered to the supply voltage at each sampling time. It therefore becomes unstable, thereby producing a variation of the delay time because the fluctuation of V_X influences the operating point of M3.

Figure 6(b) presents our proposed VCDU. While ϕ_{in} is "low", the VCDU is reset to the precharge state. Then, after ϕ_{in} becomes "high", the inverter gate is discharged directly by M6, and the inverter output is flipped, in which the switching time depends on a voltage of V_{in}. In this configuration, irrespective of the voltage of V_{in}, the gate voltage of the inverter is fully recovered at each sampling time.
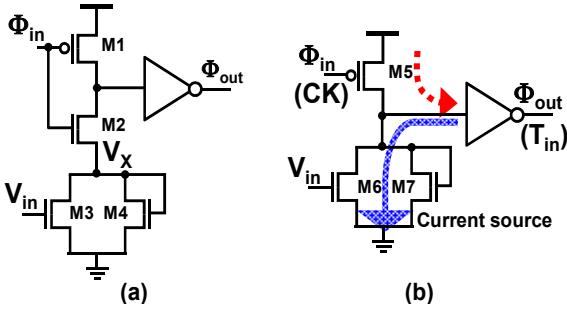

Figure 6   VCDU circuits: (a) conventional current-starved inverter VCDU and (b) proposed VCDU.

The SPICE simulation result in Figure 7 presents the characteristic of the voltage-to-delay conversion in the proposed VDCU. Nonlinearity exists, but it can be corrected using digital signal processing (DSP) after decimation filtering because the characteristic is monotonic [3]. The DSP coefficients for nonlinearity correction are obtainable by inputting the DC sweep to the VCDU (DC sweep in Figure 4) at the initial calibration phase.
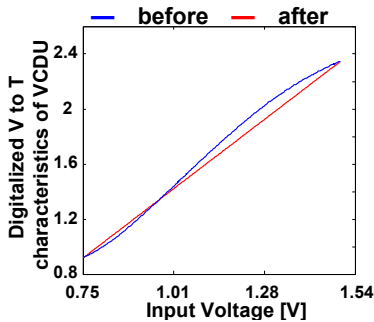

Figure 7   Voltage-to-delay conversion characteristics in the proposed VCDU: before and after nonlinearity correction.

III. IMPLEMENTATION RESULTS

We designed the proposed ADC architecture and implemented it in a 40-nm CMOM process. The layout area is 640 μm² (Figure 8). The output spectra of the first-order ΔΣ TDC and second-order MASH ΔΣ TDC are presented in Figure 9. We can observe the second-order noise-shaping characteristic, which demonstrates that the MASH functions in our design.
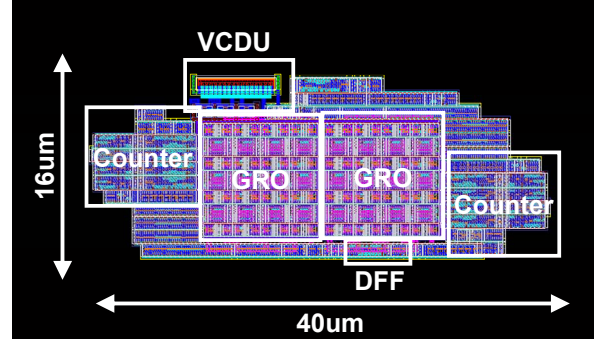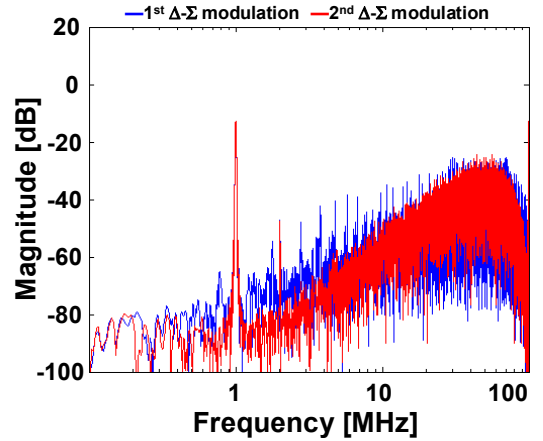

Figure 8   Layout of proposed ADC.

Figure 9   Output spectra of first-order and second-order ΔΣ TDCs.

Figure 10(a) presents a case after decimation filtering with DSP. It shows the second harmonic distortion, which degrades the SFDR to 34.94 dB. This tone comes from the nonlinearity of the VCDU. After making the nonlinearity correction described in Subsection II.C, the SFDR is improved to 52.3 dB (17.36 dB improvement compared to the case before the nonlinearity correction) as shown in Figure 10(b). The SNDR is 45 dB, and the effective number of bits (ENOB) corresponds to 7.2 bit. The power dissipation is 583.2 μW in total (GROs, VCDU, and digital logics including DFFs and counters consume 100.8 μW, 134.4 μW, and 348.0 μW, respectively). The figure of merit (FOM) at a 3-MHz bandwidth is 660 fJ per conversion step.

The specifications of the proposed ADC are compared in TABLE I with other state-of-the-art ADCs. Our proposed ADC is superior to them, particularly in terms of area. In the table, we introduce a new metric of FOM2 (= FOM × area), which emphasizes the area as a figure. Our proposed ADC

exhibits better area efficiency than the SAR architecture [6] that has an excellent FOM. To achieve high accuracy, the SAR ADC needs large capacitors, whose area cannot be scaled down with process scaling.
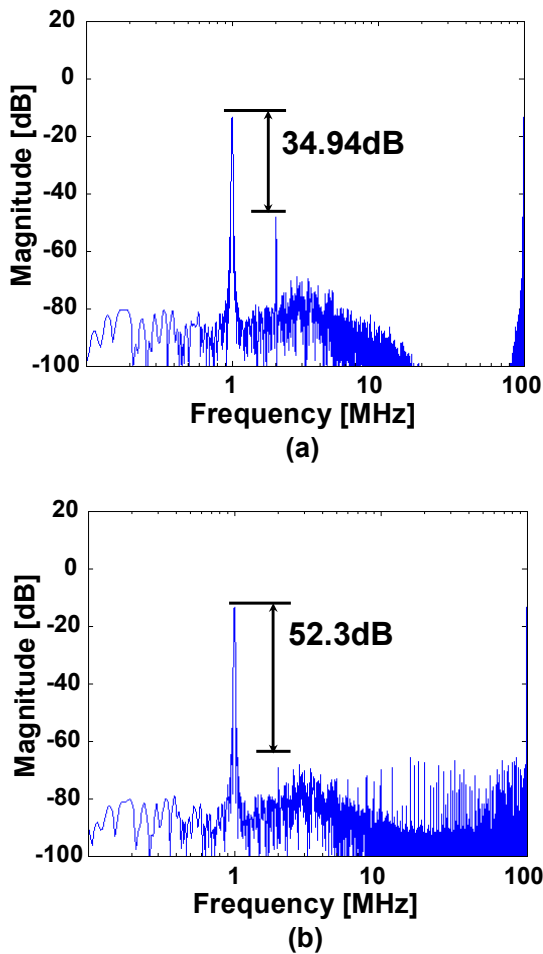

Figure 10   Decimation-filtered output spectra: (a) before and (b) after VCDU's nonlinearity correction.

IV. SUMMARY

We proposed a 640-μm^2, 45-dB, and 583.2-μW second-order MASH $\Delta\Sigma$ ADC. In the proposed architecture, analog circuits such as opamps and switched capacitors can be eliminated. The control and calibration of the TDC are implemented with digital circuits, which achieve the low-cost and low-power ADC. The proposed ADC thereby maintains scalability with future advanced processes. The design cost and turn around time (TAT) are reduced as well.

The proposed ADC exploits an oversampling technique. Therefore, by increasing the sampling rate, we can further enhance the quantization accuracy (resolution). If the sampling rate is doubled, then ENOB increases by 1.5 and 2.5 bits, respectively, in the first-order and second-order $\Delta\Sigma$ modulators. Furthermore, the ENOB can be improved with the third-order or higher MASH topology by connecting multiple stages. As process technology advances, the ring oscillator frequency becomes faster, which is good news for the proposed ADC. Process scaling will back up our proposed ADC architecture in the future.

This ADC can be adopted for a range of applications such as a ubiquitous sensor, in which many ADCs must be implemented on a chip. Therein, one node collects various information through the ADCs; it then forwards it to a base station. Small-area and low-power ADC without opamps or capacitors is useful for the future ubiquitous applications.

TABLE I   COMPARISON WITH STATE-OF-THE-ART ADCS WITH SIMILAR SPECIFICATIONS.

	[2]	[3]	[6]	This work
Technology (nm)	65	65	90	**40**
Bandwidth (MHz)	20	30	5	**3**
Sampling rate (MS/s)	250	300	10	**100**
Power (mW)	10.5	11.4	0.069	**0.583**
SFDR (dB)	N/A	79	N/A	**52.3**
SNDR (dB)	60	64	N/A	**45**
ENOB (bits)	9.7	10.3	8	**7.2**
Area (mm^2)	0.15	0.02	0.0156	**0.00064**
FOM (fJ/conv. step)	319	150	30	**660**
FOM2 (fJ·mm^2/conv. step)	47.9	3.00	0.468	**0.422**

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