0.45-V Operating V_t-Variation Tolerant 9T/18T Dual-Port SRAM

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Abstract

This paper proposes a dependable dual-port SRAM with 9T/18T bitcell structure. The proposed SRAM has two operating modes: a 9T normal mode and an 18T dependable mode. The 9T bitcell has an outside single-ended bitline as a dedicated read port along with a pair of conventional differential inside bitlines. Therefore, the 18T bitcell has two differential pairs of the outside bitlines and inside bitlines. For the dedicated read port, the 18T bitcell can exploit a differential sense amplifier operating at low voltage, but the 9T bitcell must have a single-ended readout inverter at high voltage. To achieve the 9T/18T SRAM architecture, an interleaved bitline scheme is incorporated for the dedicated read port. The 9T/18T dual-port SRAM can scale its speed, operating voltage, and power dynamically by combining two bitcells for one-bit information.

We designed and fabricated the proposed SRAM using a 65-nm process. The measurement results show that the dependable read mode using the pair of the single-ended bitlines can reduce the operation voltage to 0.45 V at a frequency of 1 MHz because of the disturb-free read port, although the dependable read mode using the inside bitlines needs 0.54 V at the same frequency.

Keywords

SRAM, dependability, quality of a bit

1. Introduction

The minimum feature size in transistors decreases with the advance of process technology, which achieves higher density and lower cost. Technology scaling, however, increases the threshold voltage (V_t) variation of transistors mainly because of a random dopant fluctuation (RDF). Consequently, in the recent deep submicron era, it is important to design SRAM with both read and write margins considering the V_t variation tolerance [1, 2].

The 7T/14T SRAM presented in Fig. 1(a) has been proposed to enhance SRAM dependability: two pMOS transistors (P3 and P4) are added between internal nodes in a pair of the conventional 6T bitcells [3−5]. The structure thereby achieves a dependable mode that features margin enhancements by combining two bitcells, especially at low voltage, in both read and write operations. In the dependable read mode, only one wordline is asserted to gain a large β ratio (a ratio of two driver transistors' total size to one access transistor size). A bitcell with no static noise margin (SNM) is recovered by the other bitcell through the two connecting pMOS transistors. In the dependable write mode, a datum is written into a pair of bitcells by asserting both wordlines, which averages and mitigates the write margin degradation.

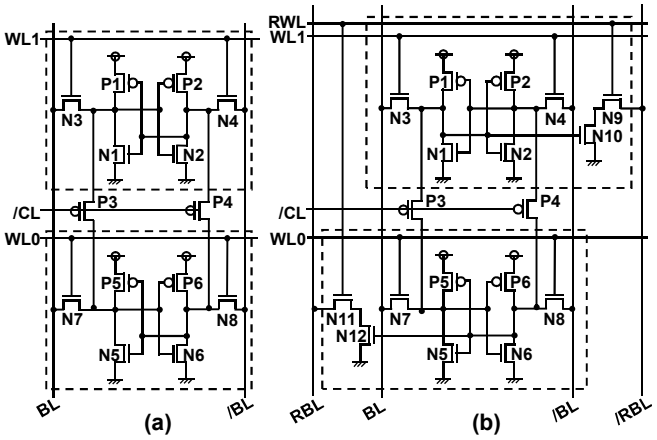

Figure 1: Schematics of (a) a conventional 7T/14T bitcell pair and (b) the proposed 9T/18T bitcell pair.

If the 7T/14T SRAM has sufficient operation margins, for instance, when operating at high voltage, then this recovery feature can be disabled by negating the two connecting pMOS transistors; it is used as a normal mode. The dependable mode and normal mode can be switched according to the operating voltage, power limit, or required dependability in an application. This concept is called "quality of a bit (QoB)", in which the operating voltage, power, and a bit error rate (BER) are controlled as attributes of one-bit information.

The QoB concept [3−5] and its applications [6−7] have been widely studied. The 7T/14T SRAM is suitable for low-voltage cache architectures [6]. Furthermore, it realizes block-level instantaneous copying that needs only four cycles to copy all the data in a 32-kb memory block [7]. This block-level copying feature is particularly eligible for high-speed data transfer among multi-core processors.

In this paper, by adding a dedicated read port, we propose 9T/18T dual-port SRAM presented in Fig. 1(b). The additional read port is disturb-free, and can thereby operate at a lower voltage than the 7T/14T SRAM. The proposed SRAM also has a 9T normal mode and 18T dependable mode, in which a single-ended inverter and differential sense amplifier are used, respectively, for readout. To incorporate the two modes, an interleaved bitline (BL) scheme is adopted. This proposed 9T/18T SRAM is suitable for use in a multimedia processor and multi-core DSP architecture.

2. 9T/18T SRAM

Fig. 1 again depicts schematics of the 7T/14T and 9T/18T bitcell pairs. The control signal, /CL, is for switching between the normal mode (/CL = "H") and

dependable mode (/CL = "L"). In the dependable mode, a 14T or 18T bitcell pair acts as a single bitcell. In the 9T/18T bitcell, four nMOS transistors (N9, N10, N11, and N12) and dedicated read bitlines (RBLs) are appended to the 7T/14T bitcell. Read wordlines (RWLs) are appended for the read ports' control.

To shrink an area of the proposed 9T/18T SRAM and reduce its area overhead, we use an interleaved BL structure for the read port. Fig. 2 depicts the interleaved bitcell array structure. A pair of right and left bitcells shares an RBL. Instead, two RWLs must be interconnected through each row of the bitcell array.

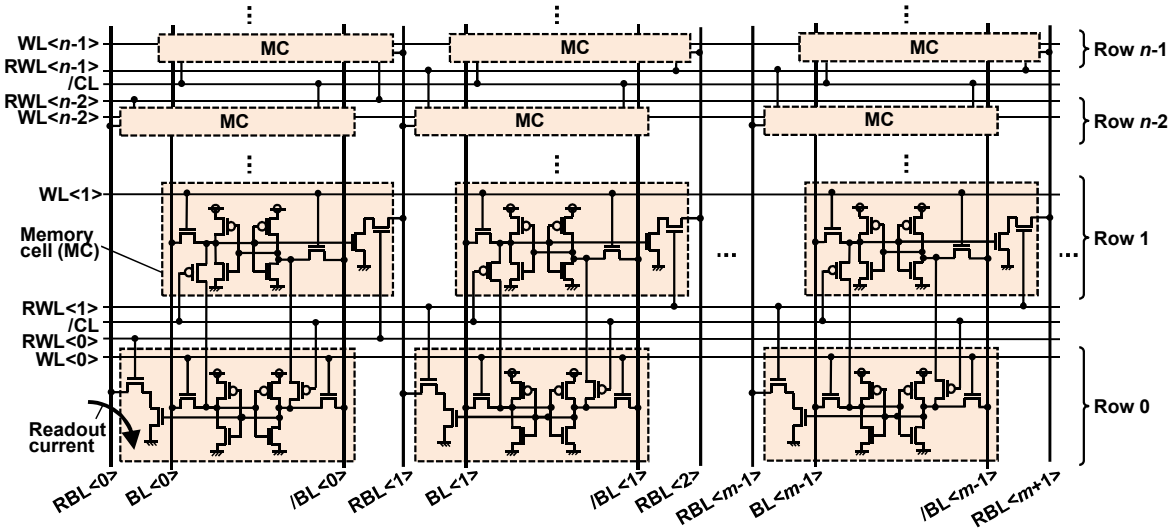

Figure 2: Interleaved BL structure for read port in proposed 9T/18T SRAM. An RBL is shared by an upper left and lower right (or upper right and lower left) bitcells. An RWL is also shared but connected to every other bitcells.

Fig. 3 portrays the layout of the 9T/18T bitcell pair. The design is based on a logic design rule; all transistors have a minimum size (W/L = 170/60 µm). The area of this pair cell is 3.075 × 1.100 µm^2, which has, respectively, a 26.54% and 12.20% area overhead compared to the 7T/14T (= 2.43 × 1.1 µm^2) and 2-b 8T cells (= 2.70 × 1.1 µm^2).

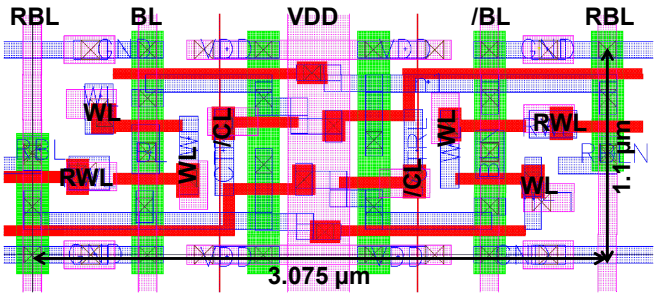

Figure 3: Layout of 9T/18T bitcell pair in a 65-nm process.

When RWL<0> in Fig. 2 is asserted, the even-numbered column's read ports in Row 0 and Row 1 become active. The stored data are read out to RBLs. When /CL is asserted, every pair of RBLs come to a differential readout. Consequently, additional multiplexers must be prepared to choose a single-ended or differential readout. Furthermore, the proposed 9T/18T SRAM has the other inside read port because it is a dual-port SRAM; a datum can be read out though the inside BL pairs as well as the outside read port. Therefore, the 9T/18T SRAM achieves higher memory bandwidth than the 7T/14T SRAM. It is useful for multimedia processor such as video processing and multi-core DSP architecture.

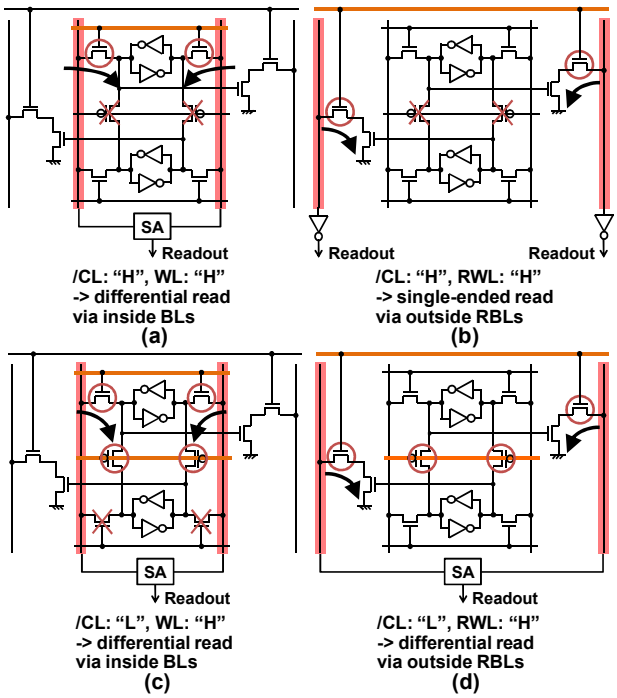

Figure 4: Readouts of four kinds: (a) normal-mode differential read via inside BLs, (b) normal-mode single-ended read via outside read port, (c) dependable-mode differential read via inside BLs, and (d) dependable-mode differential read via outside read port. Here, SA denotes a sense amplifier.

Consequently, as portrayed in Fig. 4, the proposed 9T/18T SRAM possesses readouts of four kinds. Figs 4(a) and 4(c) are read operations with the inside BLs in the respective normal and dependable modes, which corresponds to those in the 7T/14T SRAM. Fig. 4(b) and 4(d) show other read operations using the additional read ports.

As for a write operation, no difference exists between the 7T/14T SRAM and 9T/18T SRAM. In the normal write mode, its condition is the same as that of the classic 6T SRAM. In the dependable write mode, to assure the conductance of the access transistors, both wordlines in the bitcell pair are enabled. Results show that the conductance of the access transistors is averaged, and that the V_t variation is suppressed. Thereby, the write margin becomes larger.

3. Chip Implementation and Measurement Results

We designed and fabricated a 128-kb SRAM macro in a 65-nm process technology for measurement and verification. Fig. 5 presents the chip micrograph and SRAM macro layout. The core size of the 9T/18T SRAM macro is 1130 × 413 μm^2. The macro comprises eight blocks (block size, 141 × 413 μm^2); each has a 16-kb array (128 rows × 8 columns × 16 b), address decoders, write drivers, inverters for the outside single-end BLs, and two sets of sense amplifiers for the inside and outside differential BLs. For the sense amplifier circuit, we adopt a commonly used latch type sense amplifier.

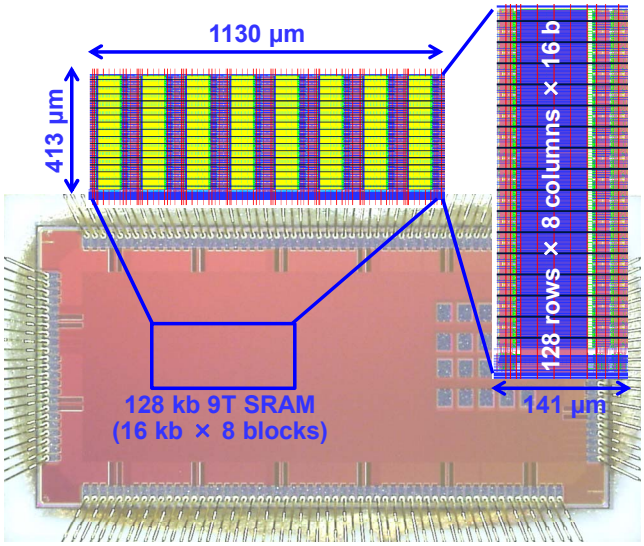

Figure 5: Chip micrograph and SRAM macro layout.

Fig. 6 presents the measured bit error rates (BERs) of the 9T/18T SRAM. The minimum operating voltages in the normal mode are 0.67 V and 0.72 V, respectively, with the inside differential BLs and outside single-ended BL; the minimum operating voltage in the single-ended BL is worse by 50 mV than that in the differential BLs because the single-ended BL must be a full swing.

However, in the dependable mode, the outside differential BLs lowers the minimum operating voltage to 0.45 V (90-mV reduction) by virtue of the disturb-free differential readout, whereas that in the inside differential BL needs 0.54 V. This minimum operating voltage reduction can achieve lower power in a low-voltage region.

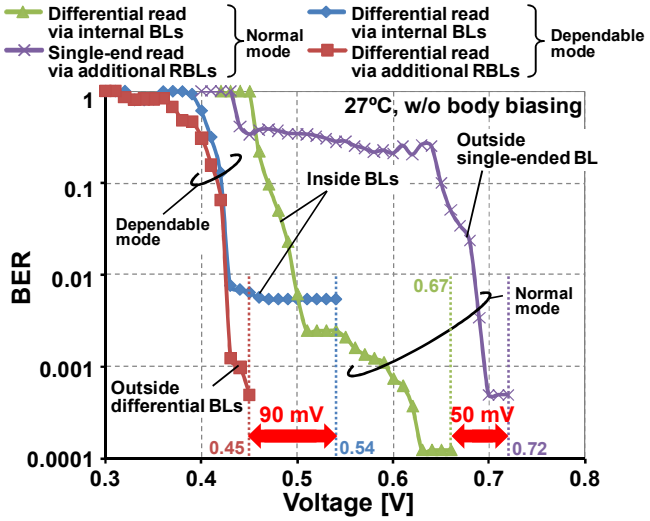

Figure 6: Measured BERs of 9T/18T SRAM for four read operations. Frequency is 1 MHz.

To apply body biasing and to simulate behaviors at various process corners, the SRAM macro is designed with a triple-well process. In other words, the body biasing control gives global V_t variations, which means that we can estimate reliabilities under the global V_t variations. To guarantee the V_t control accuracy, we implemented a pMOS and nMOS test transistors on the chip for characteristic measurements.

Table 1 presents the body bias settings at which four process corners (FF, FS, SF, and SS) are emulated. ΔV_{tn} ($\Delta|V_{tp}|$) represents an nMOS (pMOS) transistor's threshold voltage difference from the fabricated CC transistor.

Table 1: Body bias settings: ΔV_{tn} and $\Delta|V_{tp}|$.

Corner	ΔV_{tn} [mV]	$\Delta\|V_{tp}\|$ [mV]
CC	±0	± 0
FF	−146	−92
FS	−97	+67
SF	+74	−61
SS	+108	+99

Fig. 7 portrays curves of access time versus supply voltage when body biasing is applied according to Table 1. The access time is the period from a time at which a clock rises up to a time at which an output is fixed: it includes delays in a decoder, wordline, BL charging/discharging, sense amplifier, and terminal I/O buffer. Body biasing is applied not only to a bitcell array but also to peripheral circuits aside from the I/O buffer.

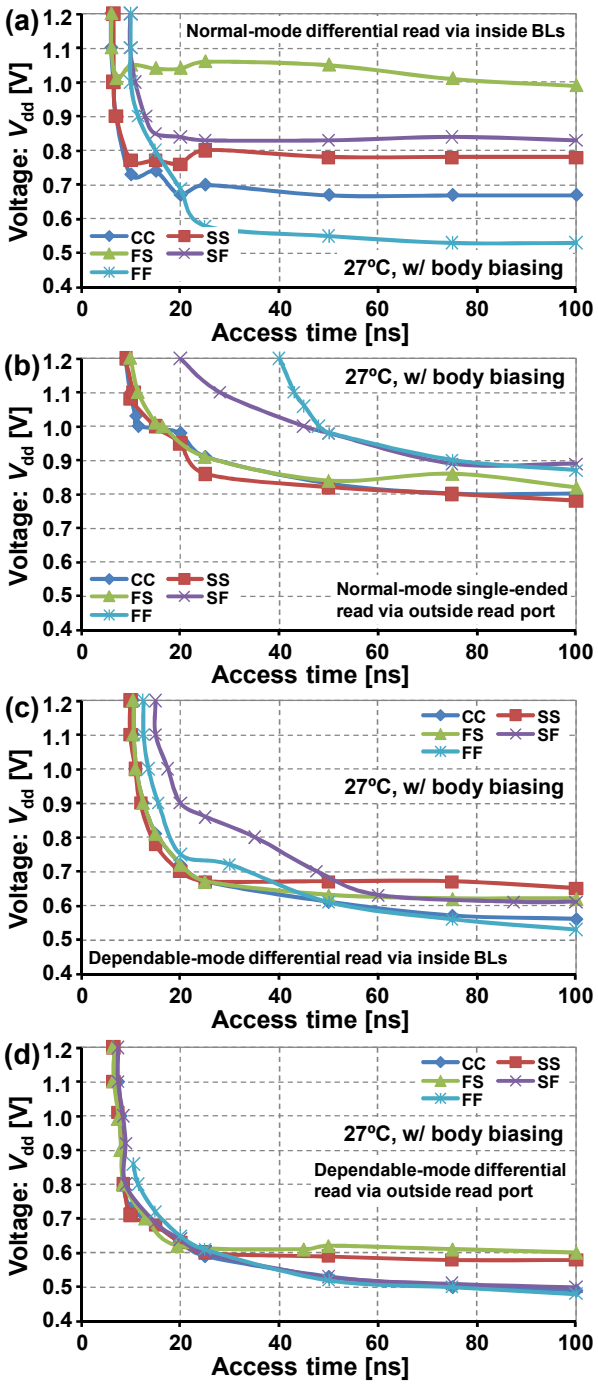

Figure 7: Measured characteristics in access time versus supply voltage: (a) normal-mode differential readout, (b) normal-mode single-ended readout, (c) dependable-mode inside differential readout, and (d) dependable-mode outside differential readout.

Fig. 7(a) shows the inside differential readout in the normal mode, which suffers most from the V_t variation, and the operating voltages are widely varied. Fig. 7(b) shows the out single-ended readout in the normal mode. The readout inverter needs a full swing, causing slower operation especially at the FF and SF corners. This is because a storonger pMOS discharges a bitline even when a "H" readout and it leads to fail readout operation. Figs. 7(c) and 7(d) respectively show the inside and outside differential readouts in the dependable mode. The outside BLs exhibit better performance with the disturb-free feature, although the inside differential readout becomes particularly slower at the SF corner.

4. Conclusion

We proposed the 9T/18T SRAM, which provides better read margin than that of the conventional 7T/14T SRAM. The 9T/18T bitcell topology is comprised of the conventional 7T/14T cell and an additional read port. In the 9T/18T SRAM, the additional read port can operate without care of the static noise margin because of the disturb-free read operation. Consequently, the 9T/18T SRAM is more stable than the 7T/14T SRAM under threshold-voltage (V_t) variation. We fabricated the proposed SRAM using a 65-nm triple-well process. The measurement results show that the dependable read mode using the additional read port can suppress the V_t variation, and reduce the operation voltage to 0.45 V, although the dependable read mode using internal bitlines needs 0.54 V. Body biasing controlling reveals the weakness of the conventional 7T/14T SRAM read process and clarifies that the 9T/18T SRAM has greater reliability against unbalanced process corners, particularly SF corner, than the 7T/14T SRAM.

Acknowledgement

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