Block-Basis On-Line BIST Architecture for Embedded SRAM Using Wordline and Bitcell Voltage Optimal Control

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Abstract

A system on a chip (SOC) is becoming smaller and denser. Shrinking transistor size facilitates the integration of functionality on the chip operating at low supply voltage, although this trend lowers the silicon chip reliability. Nevertheless, it is necessary to maintain complete functionality during a long duration, even under changing environments such as temperature fluctuation and/or device wearout: Bias temperature instability must be considered as a time-varying parameter as well. Consequently, techniques that can maintain chip reliability with self-diagnosis and self-repair capabilities are required.

In this paper, we propose a dependable SRAM with a built-in self-test that can diagnose and repair itself using wordline and bitcell voltage control. The proposed SRAM comprises memory blocks; each block has independent supply voltages for the wordlines and bitcells. This diagnosis and repair scheme is especially effective for faults that occur in the field. The self-testing capability is available on-line. It is completely transparent to a user, who can use the SRAM with no modification or speed degradation in the memory access protocol. A 1-Mb (64-Kb × 16 blocks) SRAM with the BIST was fabricated with a 65-nm CMOS process and verified. The area overhead is 2.8%.

Keywords

SRAM, fault model, BIST, BISR, test, on-line, background

1. Introduction

Because of improvement of very large scale integration (VLSI) fabrication technology, many components can now be embedded on a single chip. The fabrication density of a regular structure circuit, such as static random access memory (SRAM), is especially high. Therefore, they are very vulnerable. To reduce test costs and conduct on-chip tests, many built-in self-test (BIST) and built-in self-repair (BISR) techniques have been proposed for SRAM [1–3].

Although embedded SRAM on a chip is thoroughly tested before shipping, it might become defective in normal operation. The chip must continue operating with complete functionality during long durations, but in operating environments, temperature and transistor threshold voltage (V_T) are fluctuated: bias temperature instabilities (BTIs), particularly negative bias temperature instability (NBTI) in a standard gate oxide pMOS transistor [9] and positive bias temperature instability (PBTI) in a recent high-k metal gate nMOS transistor [10], increase the transistor's V_T and degrade its drive. Therefore techniques that test a chip periodically in the field and maintain its reliability are necessary.

To address this problem, several BIST and BISR techniques have been proposed for embedded memory to carry out a test periodically in the field, without being noticeable by a user. The transparent BIST preserves memory content until the end of a test [4–5]. The input vector monitoring concurrent BIST exploits input vectors arriving at the inputs of the memory under test (MUT) in normal operation [6]. Although both techniques can test a chip periodically, they are not at-speed tests. To make matters worse, memory bandwidth suffers from a timing penalty.

The on-line BIST conducts a test after transferring memory content to a safety area [7]. This technique does not degrade the memory access speed because the memory access remains connected to the memory content during test operation. Most studies including [7] use a dedicated redundant area to repair a fault. A stack-at fault and open fault can be repaired by the small redundant area, but they do not generally occur in the field. A wide area of the chip suffers from the environmental change. Therefore, these techniques using the redundant area are ineffective to repair faults in the field. To save them, a larger extra memory is necessitated, resulting in a further area overhead.

We propose a dependable SRAM with an on-line BIST. It can periodically test its memory content in the field and keep the chip reliable using block-level voltage control. The SRAM is divided into memory blocks. Then each block is tested one after another in the background. In each block, by changing wordline and bitcell voltages, a self-test can be conducted at various combinations of the voltages. Therefore, the optimal voltage combination can be found at which both read and write margins are maximized; then the voltage combination is supplied to the memory block.

The paper is organized as follows. Section 2 presents the concept of the proposed scheme, particularly addressing the wordline and bitcell voltage control and on-line BIST architecture. Section 3 describes chip implementation. In section 4, we conclude this paper.

2. Proposed Scheme

2.1. Read and Write margins

Many assist techniques for SRAM have been proposed to improve operating margins. Fig .1 presents a static noise margin (SNM) and write trip point (WTP) defined as a respective read and write margins. The SNM and WTP are improved respectively by lowering a wordline voltage (V_{WL}) and bitcell voltage (V_{BC}). These techniques are very effective in a low-voltage SRAM [11] because no room exists to increase the supply voltage in a scaled transistor. However, improving the read margin by lowering V_{WL} worsens the write margin, and vice versa. Consequently, it is difficult to improve both SNM and WTP simultaneously: the optimal combination of V_{WL} and V_{BC} presents itself, but they are affected by temperature and V_T fluctuations.

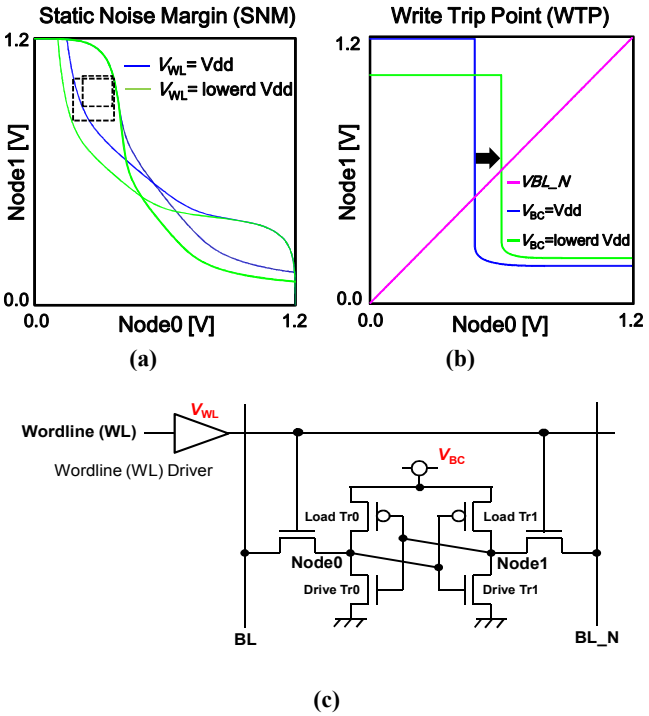

Figure 1: (a) Static noise margin (SNM), (b) write trip point (WTP), and (c) SRAM bitcell circuit.

Thus, the NBTI and PBTI are important issues related to reliability. The NBTI shifts V_T of the pMOS load transistor in a bit cell with stress time, which degrades the SNM. The PBTI in the nMOS drive transistor degrades the SNM as well. In fact, the SRAM retains the same data for a long time; the operating margin degradation is a crucial problem.

2.2. BIST Structure

Fig. 2 presents a brief explanation of the proposed block-basis on-line test. The MUT block is tested by changing the supply voltages, and their optimal combination is found. If not found, fault information (fault addresses, supply voltages, and temperature) of the MUT block is sent to the log block. The next block is tested after transferring its content to the MUT that has just been tested. In this way, the BIST changes an MUT block one after another without losing its memory content.

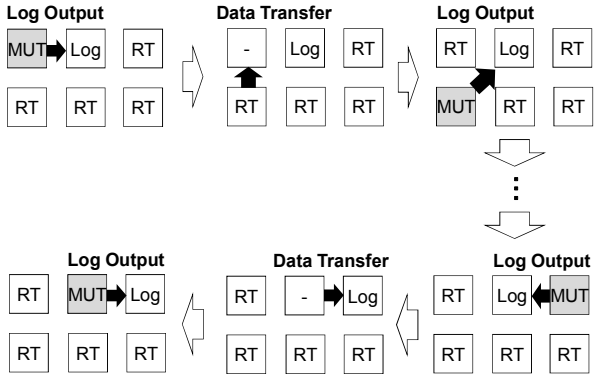

Figure 2: Block-basis on-line test.

Fig. 3 shows the proposed block-basis SRAM with a BIST. Each 64-Kb block has an independent supply voltage for the wordline drivers and bitcells. The BIST can access all blocks, but at a single time, at most, one is an MUT block and another is a log block that stores a testing log as the fault information of the MUT block. In the MUT block, the testing voltages for V_{WL} and V_{BC} are changed with the dedicated power supply ($V_{rt0,1}$ in the V_{ctrl} module); then a test is conducted. The other blocks act as run time (RT) blocks; their V_{WL}s and V_{BC}s are optimally selected from V_{mut0-3}. A user can access the RT block directly. All blocks might be used as the RT blocks if testing or logging is necessary, in which case no memory capacity overhead exists.

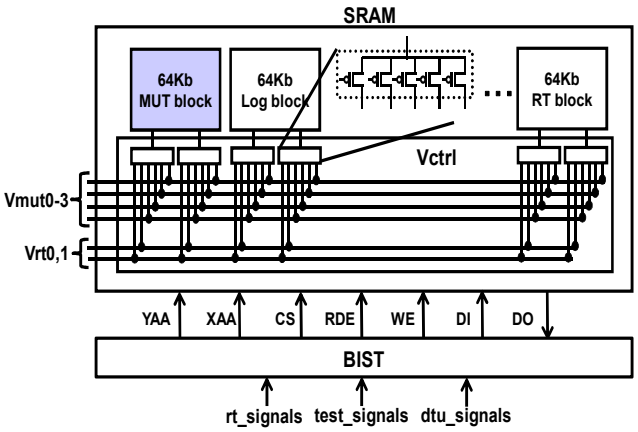

Figure 3: Block diagram of the proposed SRAM architecture with BIST. XAA and YAA are X and Y addresses. CS is a chip select signal. RDE and WE are a read and write enabling signals. DI and DO are input and output data. "rt_signals", "test_signals", and "dtu_signals" are control signals for RT operation, test operation, and data transfer unit (dtu) operation, respectively.

Fig. 4 shows a block diagram of the proposed BIST, which comprises a data transfer unit, test unit, address translator, and controller. The data transfer unit transfers data between an RT and MUT blocks with direct memory access (DMA). After the data transfer, the test unit conducts a test without losing memory content, and obtains fault information. To provide the transparent test to a user, the address translator translates a logical address to a physical one. It then enables a user to access an arbitrary address seamlessly. The controller handles real-time user accesses. It is interrupted temporarily and the user access is conducted before the data transfer if memory access from a user occurs to the block that is under the data transfer. Subsequently, the data transfer is resumed.

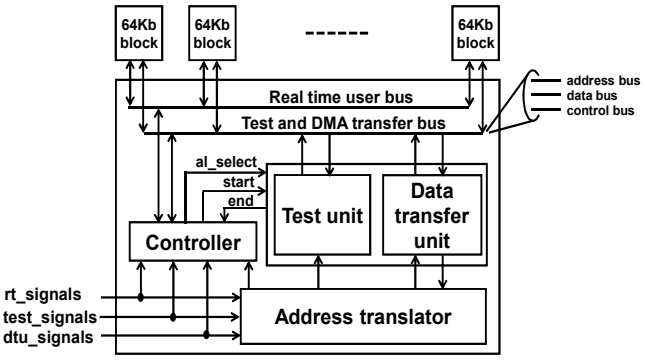

Figure 4: Block diagram of the proposed BIST.

Fig. 5 portrays a block diagram of the test unit including an algorithm generator, test controller, data generator, address generator, and comparator. The test unit selects one block as an MUT block and another block as a log block to store a testing log. The test is based on algorithm testing; the algorithm generator outputs a series of simple operation codes (op_code) according to the algorithm select signal (al_select). The data generator and address generator respectively generate a test pattern and addresses. The test controller controls both the data generator and address generator. The comparator compares acquired data from the MUT block (data_out) with calculated expected data from the data generator (data_in). The fault information (fault_info) is sent to a logging address (log_address) in the log block if the comparison result fails. Fault information includes a fault address, voltages (V_{WL} and V_{BC}), and the temperature (temp) when the fault occurred.

A complicated test algorithm can cover more faults, whereas a simple one can detect only simple faults, but the test time is shorter. Consequently, a suitable test algorithm varies with the circumstances. The algorithm generator supports seven algorithms, as shown in Table 1. Regarding notation, "r" ("w") signifies read (write) operation, "0" ("1") denotes non-inverted (inverted) test data, and "↑" ("↓") denotes ascending (descending) order address. The March SS algorithm is the most complicated but it offers superior coverage.

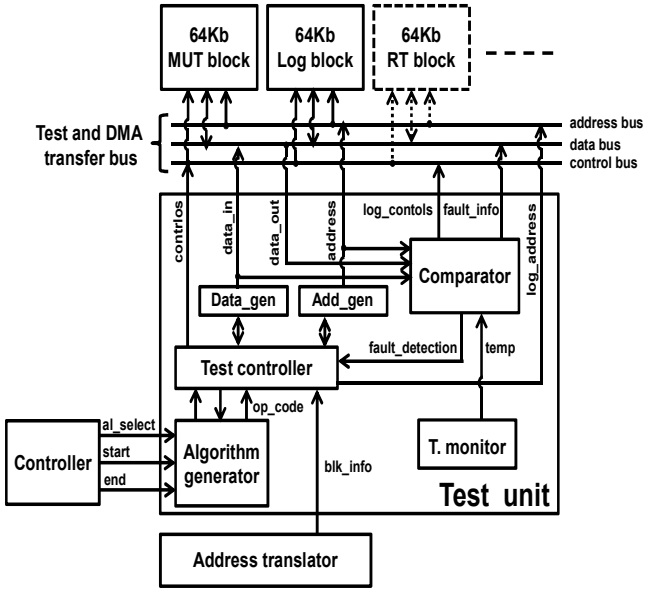

Figure 5: Block diagram of the test unit. "start" and "end" are start and end signals for testing. "blk_info" is information on the MUT block and log block coming from the address translator so that the test controller can select the MUT block and log block correctly.

Table 1: Algorithm selection table

No	Algorithm	
001	MATS+	↑w0 ↑r0,w1 ↓r1,w0
010	March X	↑w0 ↑r0,w1 ↓r1,w0 ↑r0
011	March C-	↑w0 ↑r0,w1 ↑r1,w0 ↓r0,w1 ↓r0,w0 ↑r0
100	March B	↑w0 ↑r0,w1,r1,w0,r0,w1 ↑r1,w0,w1 ↓r1,w0,w1,w0 ↓r1,w1,w0
101	March U	↑w0 ↑r0,w1,r1,w0 ↑r0,w1 ↓r1,w0,r0,w1 ↓r1,w0
110	March LR	↑w0 ↓r0,w1 ↓r1,w0,r0,w1 ↓r1,w0 ↑r0,w1,r1,w0 ↑r0
111	March SS	↑w0 ↑r0,r0,w0,r0,w1 ↑r1,r1,w1,r1,w0 ↓r0,r0,w0,r0,w1 ↓r1,r1,w1,r1,w0 ↑r0

3. Implementation

We implemented a 1-Mb SRAM with the proposed BIST in an industrial 65-nm process. Fig. 6 shows a chip micrograph and layout consisting of 16 × 64-Kb blocks. The areas of the SRAM and BIST are, respectively, 3,270 × 1,200 μm^2 and 3,270 × 30 μm^2. The area overhead of the BIST module is 2.8% for the 1-Mb SRAM.

Fig. 7 presents an example of a fail bit map. The red spots are fault cells. The waveform shows detailed information of the fault cell.

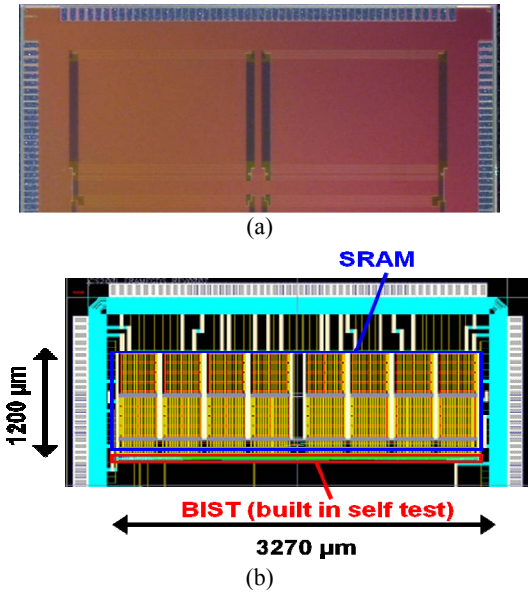

Figure 6: (a) Chip micrograph and (b) layout of the proposed SRAM.

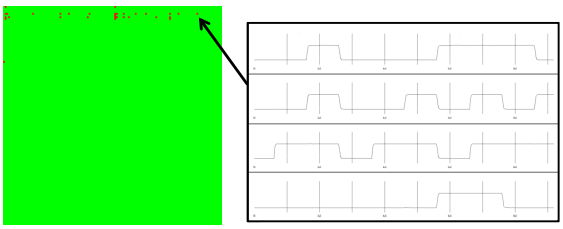

Figure 7: Fail bit map and real wave.

4. Conclusion

As described in this paper, we proposed a dependable SRAM with BIST that can maintain its own reliability by controlling supply voltages. The block-basis on-line BIST is especially effective for the fault in the field. The test and repair capabilities function in the background of the normal operation and completely transparent to an external user, who can use the SRAM with no modification or speed degradation in the memory access protocol. A 1-Mb (64-Kb × 16 blocks) with the BIST was fabricated in a 65-nm CMOS process and verified. The area overhead by the BIST is 2.8% for the 1-Mb SRAM.

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