A 14μA ECG Processor with Noise Tolerant Heart Rate Extractor and FeRAM for Wearable Healthcare Systems

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Abstract – This report describes an electrocardiograph (ECG) processor for use with a wearable healthcare system. It comprises an analog front end, a 12-bit ADC, a robust Instantaneous Heart Rate (IHR) monitor, a 32-bit Cortex-M0 core, and 64 Kbyte Ferroelectric Random Access Memory (FeRAM). The IHR monitor uses a short-term autocorrelation (STAC) algorithm to improve the heart-rate detection accuracy despite its use in noisy conditions. The ECG processor chip consumes 13.7μA for heart rate logging application.

I Introduction

Key factors affecting wearable system usability are miniaturization and weight reduction. Battery weight is a dominant characteristic of a wearable system. Therefore, the battery capacity and power consumption must be limited to the greatest degree possible. This report specifically describes an electrocardiograph (ECG) monitoring SoC for use in a wearable healthcare system. The proposed SoC has normally-off computing using nonvolatile memory and a dedicated Instantaneous Heart Rate (IHR) extractor. The IHR is an important bio-signal used for heart disease detection, heart rate variation analysis, and exercise intensity estimation.

II. Processor Architecture

Fig. 1 presents a block diagram showing the proposed ECG processor, which consists of an ECG sensing block, Ferroelectric Random Access Memory (FeRAM), 32-bit Coretex-M0 core, and extra interfaces. Because the frequency range of vital signals is low (less than 1 kHz), both the standby power reduction and sleep time maximization are important to minimize the total power consumption. The 64-Kbyte FeRAM is integrated as a data buffer for daily life monitoring because the leakage current of the data buffer is dominant in the standby state.

The ECG sensing block has an analog front end (AFE), a 12-bit SAR ADC, and a robust IHR monitor. The AFE includes a 34-dB gain instrumental amplifier and a 20-dB gain amplifier. The ADC sampling rate can be set to 1kSamples/s for ECG processing mode and 128 Samples/s for IHR monitoring mode. The robust IHR monitor is the main contribution of this study.

III. Robust Instantaneous Heart Rate Monitor

A. Heart rate extraction algorithm in wearable healthcare

Extracting R-waves with threshold determination is a general approach. Autocorrelation [1, 2] and template matching [3] are more robust approaches to prevent incorrect detection because these algorithms use the similarity of QRS complex waveforms and have no threshold calculation process. Autocorrelation has been used in a non-invasive monitoring system [2]. However, the method necessitates numerous computations because it calculates the average heart-rate over a long duration (30 s). In our previous work, a short-term autocorrelation (STAC) technique was proposed for IHR detection [4].

Fig. 2 portrays IHR extraction using STAC. As depicted in Fig. 2, the IHR at time tn (IHRn) is obtained as a window shift length (Tshift) that maximizes the correlation coefficient between the template window and the search window. The STAC method can improve the noise tolerance about 5.6 dB with a 95% success rate.

B. Hardware implementation of the heart rate monitor

In this work, we introduce a robust IHR monitor, which employs two-step noise reduction technique. In the first stage, a quadratic spline wavelet transform (QSWT) [5] is used to mitigate the baseline wander and hum noise.

In the second stage, the IHR is extracted using the STAC method. The STAC is also implemented as dedicated hardware to minimize the power overhead. Fig. 3 presents the block diagram of the IHR monitor and STAC processing core. Each STAC core has CC buffer to store the intermediate value of correlation coefficient. The CC buffer is updated in synchronization with ADC output. Since the Lwin is 1.5 s and because IHR is updated every second, two STAC cores alternately calculate IHR with 0.5 s overlap.

IV. Implementation Result

The test chip is fabricated using 130-nm CMOS technology. Fig. 4 presents a chip photograph and a performance summary. The operating voltage is 1.2 V for AFE, ADC, SRAM, 24-MHz oscillator, and digital blocks. The FeRAM, 32-KHz oscillator, and IO circuits are operated with 3.0 V supply voltage.

To demonstrate the test chip performance, we implemented a heart rate logging application. An Android smartphone is used for program loading and logging data retrieval. As portrayed in Fig. 5, the IHR is extracted correctly in a noisy condition.

As presented in Fig. 6, the IHR monitor and FeRAM respectively contribute to active ratio reduction and sleep power reduction. Table 1 presents a performance comparison of the ECG processor. Compared with earlier ECG processors, the proposed processor has lower power and grater memory capacity for daily-life monitoring.

V. Conclusions

As described in this paper, we proposed a low-power ECG processor with a robust heart rate monitor. The robust heart rate monitor can correctly extract a heart rate from noisy environments using the STAC algorithm. The measured total current consumption is 13.7 µA at 1.2V and 3.0V power supply for the heart rate logging application.

Acknowledgement

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TABLE I
Performance comparison with previous studies

	This work	ISSCC'12 [12]	VLSI'11 [13]
Technology	130 nm	130 nm	180 nm
Supply voltage	1.2V/3.0V	0.3-0.7V	1.2V
Frequency	24 MHz/32 kHz	1.7 MHz-2 kHz	1 MHz
MCU	Cortex M0 (32 bit)	8b RISC	n/a
On chip memory	129.75 kB	5.5 kB	46 kB
Total power for heart rate extraction	18.24 µW	19 µW	31.1 µW
Total current for heart rate extraction	13.7 µA	>27 µA	25.9 µA

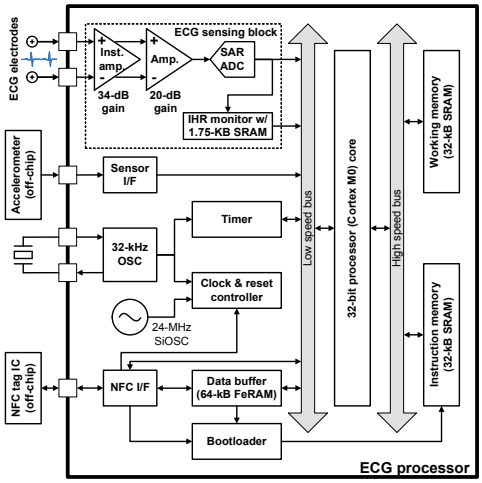


Fig. 1. Block diagram of ECG processor.

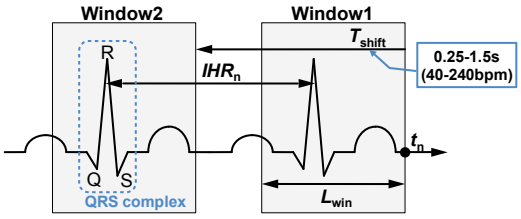


Fig. 2. IHR extraction with short-term autocorrelation (STAC).

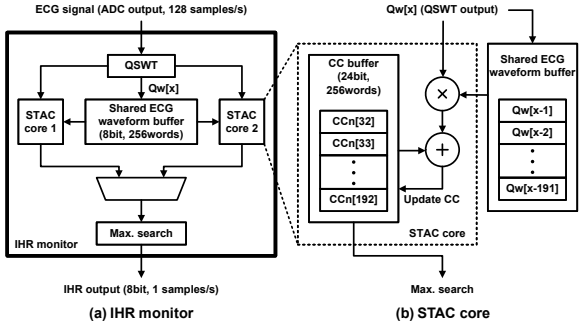
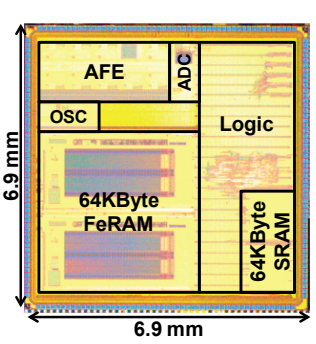


Fig. 3. Block diagram of robust IHR monitor.



Technology		130-nm CMOS
Supply voltage		1.2V (Digital, SRAM, ADC, AFE)
		3.0V (FeRAM, 32kHz OSC, I/O)
Chip area		6.9 mm × 6.9 mm
Frequency		24 MHz (for MCU)
		32 kHz (for other blocks)
MCU		32-bit Cortex M0
On chip memory		64-KB FeRAM (for logging data)
		64-KB SRAM (for MCU)
		1.75-KB SRAM (for IHR detector)
ADC	Resolution	12 bit
	Current	0.5 µA@128 S/s, 1.4 µA@1 kS/s
AFE	Gain	54 dB
	Bandwidth	0-100 Hz
	Current	3.4 µA
Total current		12.7 µA (for heart rate logging)

Fig. 4. Chip photograph and chip specifications.

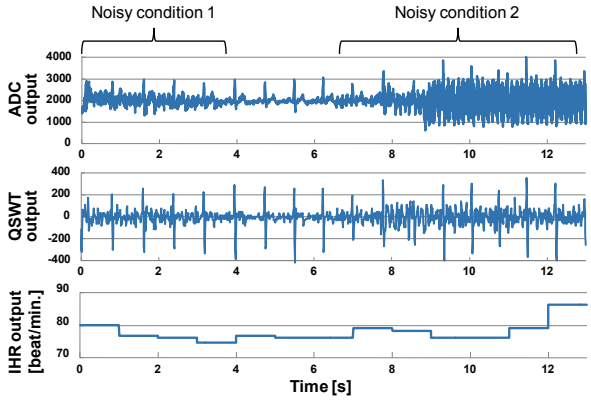


Fig. 5. Measured waveform of IHR monitor in a noisy condition.

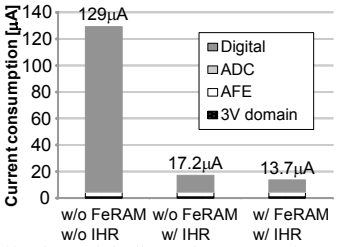


Fig. 6. Contribution of dedicated IHR monitor and FeRAM.