Temperature Compensation using Least Mean Squares for Fast Settling All-Digital Phase-Locked Loop

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***Abstract*—This paper presents a temperature compensation technique for a digitally controlled oscillator (DCO) using least means square (LMS) filtering. The proposed scheme contributes to reduction of the start-up settling time of all-digital phase-locked loop (ADPLL). The proposed method estimates the temperature using the output frequency of DCO because it is affected by temperature fluctuation. An optimal value of oscillation tuning word (OTW) for DCO can be estimated using the LMS algorithm because a linear relation exists between the output frequency of maximum OTW and the output frequency of other OTWs. These characteristics are confirmed using measurement results of the DCO, which is fabricated in 65-nm CMOS process. We modeled the ADPLL with the proposed temperature compensator in MATLAB using the measurement results of DCO. The simulation results show that the ADPLL with proposed temperature compensator achieves more than 53% settling time reduction and less than 10-MHz frequency error.**

I. INTRODUCTION

Recently, a digitally controlled oscillator (DCO), which tunes using digital codes without analog voltage control, has been used for RF wireless applications [1]. Using a DCO, an all-digital phase-locked loop (ADPLL) can be composed with no analog component. Ideally, the PLL has zero time for on/off transition and zero stand-by power. However, a gap separates the ideal and reality because the settling time of PLL prevents achievement of these ideal conditions. In this work, we specifically addressed the settling time of ADPLL.

The settling time is an important issue related to modern wireless communication applications, which use periodic wake-up for stand-by power reduction. Especially if the application has a slight active ratio (e.g. sensor network), then the settling time of PLL in RF circuits directly affects the battery lifetime because the RF circuits usually dissipate a dominant power in the system [2].

Several settling time reduction techniques have been proposed for ADPLL. The simple way is preserving the state of ADPLL including a control word for DCO at the turn-off transition. The preserved values are recalled at the next turn-on transition to mitigate the initial frequency error [3]. The problem of this method is the disturbance caused by the temperature and voltage fluctuation during stand-by. The settling time of ADPLL is increased because the output frequency of DCO is affected by these fluctuations in spite of the same control word input. Then, a voltage regulator and a band gap reference can suppress the voltage variation [4][5]. However, it is difficult to suppress the frequency variation of DCO output caused by temperature variation.

A temperature compensation technique using least-mean-squares (LMS) has been proposed [6]. The preserved control word is adjusted by the LMS algorithm. The adaptation circuit samples the filtered phase error in ADPLL and adjusts the compensation value accordingly. The technique entails very little hardware overhead. However, this algorithm assumes that the temperature difference between the turn-off transition and the turn-on transition is constant at any time. In this work, we propose compensation techniques for dynamic temperature fluctuation.

II. PROPOSED TEMPERATURE COMPENSATION ARCHITECTURE FOR FAST SETTLING ADPLL

A. Temperature Characteristics of DCO

Fig. 1 presents a schematic of an inverter-based DCO. This DCO uses a multi-phase oscillator (MPOSC), proposed in our previous work [7]. And this DCO consists of a current source. The oscillator outputs 20 phases, which can improve the phase accuracy of ADPLL [8]. The current source, which consists of variously sized pMOS, is controlled by the oscillation tuning word (OTW). The DCO has 16-bit to cover the frequency range from 800 kHz to 3 GHz.

As presented in Fig. 2, the relation between the output frequency of maximum OTW and the output frequency of other OTWs is linear in the SPICE simulated result. Here, the horizontal axis expresses the maximum frequency of DCO at each temperature. According to this relation, the proposed temperature compensation estimates suitable OTW using LMS algorithm.

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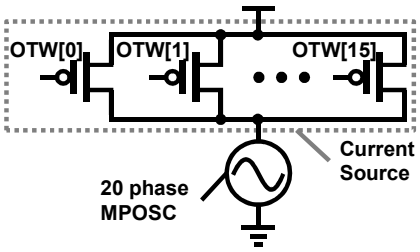

Figure 1. Schematic of digitally controlled oscillator (DCO).

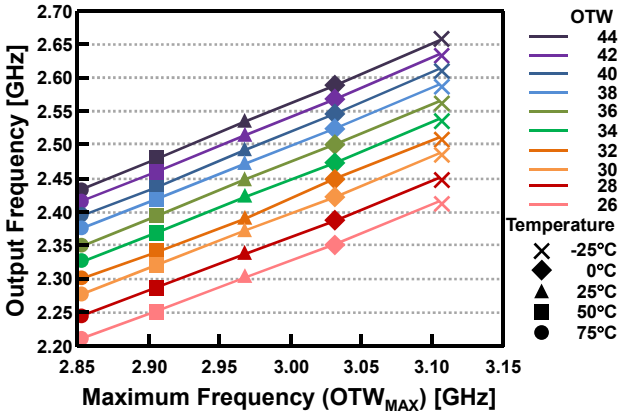

Figure 2. Simulated temperature characteristics of DCO.

B. *Temperature Compensate Architecture using LMS filter*

Fig. 3 shows the proposed scheme, which consists of the DCO and an estimation block. A counter count up the DCO output (DCO_{OUT}), and the counter output (D_{OUT}) is updated at a rising edge of reference clock (F_{REF}). Then, D_{OUT} expresses the DCO frequency. The estimation block detects the temperature fluctuation using D_{OUT} and estimates the optimal value of OTW. If the optimal OTW is estimated correctly, then D_{OUT} equals the frequency command word (FCW).

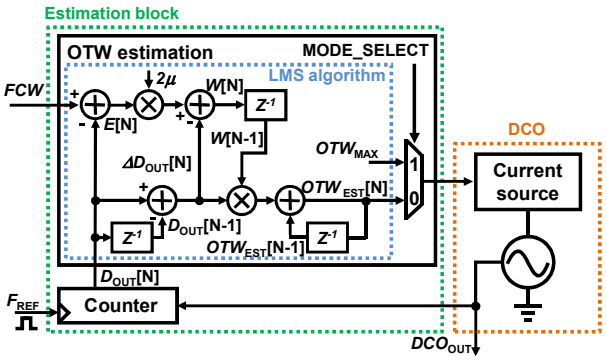

Figure 3. Proposed architecture.

Fig. 4 presents behaviors of the proposed architecture. The proposed scheme has two states: thermometer mode and DCO mode. In thermometer mode, the DCO oscillates with the maximum OTW immediately after power-on. The estimation block detects the temperature fluctuation from the output frequency of DCO. The OTW estimation block calculates an optimal value according to LMS algorithm. In DCO mode, the DCO oscillates with estimated OTW by the estimation block. The estimation block detects the frequency of the DCO output and compares D_{OUT} and FCW.

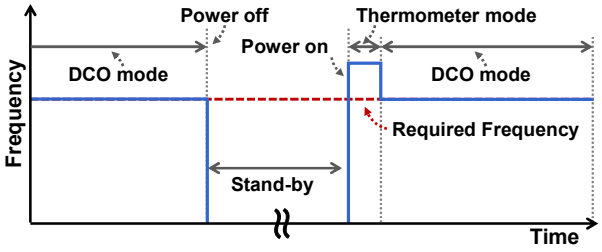

Figure 4. Behavior of proposed architecture.

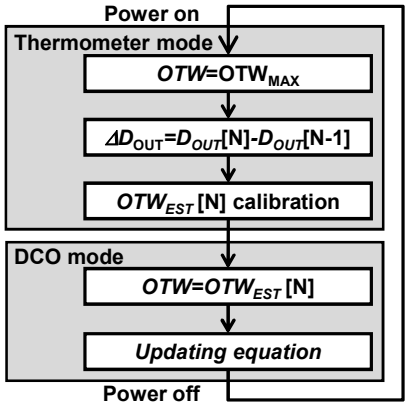

Figure 5. Calculation flow of temperature compensation.

Fig. 5 shows the calculation flow of temperature compensation. To detect the temperature at start-up, the DCO oscillates with maximum OTW (OTW_{MAX}). D_{OUT} expresses the present temperature. Therefore, the temperature fluctuation value ($\Delta D_{OUT}[N]$) is calculated. The proposed scheme estimates the temperature characteristic using a first-order equation. The estimate block calculates the first-order estimate equation using LMS algorithm. The first-order estimate equation is expressed as

$$OTW_{EST}[N] = W[N] \times \Delta D_{OUT}[N] + OTW[N-1], \quad (1)$$

where N is the start-up number, and $W[N]$ is the coefficient of the estimation equation, $OTW_{EST}[N]$ is an estimated optimal value.

The estimation accuracy is improved by updating the estimation equation. LMS filter updates the equation using an estimation error. The required frequency is determined as $FCW \times F_{REF}$. Furthermore, $D_{OUT}[N] \times F_{REF}$ expresses the frequency of the present DCO. Therefore, the error from frequency is determined as

$$E[N] = FCW - D_{OUT}[N]. \quad (2)$$

$E[N]$ is the error of the estimate equation. LMS filter updates $W[N]$ to reduce $E[N]$ using

$$W[N] = W[N-1] + 2 \times \mu \times E[N] \times \Delta D_{OUT}, \quad (3)$$

where μ is the step size. Before setting the DCO powered-off, the estimation block updates $W[N]$ using (3).

C. ADPLL with Temperature Compensation

The proposed scheme can be combined a ADPLL [2]. Fig. 6 portrays the ADPLL with the proposed scheme. The counter accumulates a *FCW* and a DCO_{OUT} with rising edge of reference clock. The TDC is the sample-and-hold based TDC (SH-TDC), which detects the frequency error with high resolution [8]. In the SH-TDC, 20-phase signals from the MPOSC are sampled. The digital phase error (ϕ_E) represents the difference between *FCW* and D_{OUT}. The digital filter normalizes ϕ_E to OTW. DCO_{OUT} is calculated as shown below.

$$DCO_{OUT} = FCW \times F_{REF} \tag{4}$$

Using the proposed scheme, the effect of temperature fluctuation is compensated, and the start-up settling time is reduced. The enable signal (MODE_SELECT) selects the output of the loop filter or OTW estimation block. When MODE_SELECT is low, the OTW estimation block compensates the temperature fluctuation. The ADPLL with the proposed scheme can estimate the temperature characteristic of the DCO. The OTW estimation block renews the compensated equation using the counter at locking frequency.

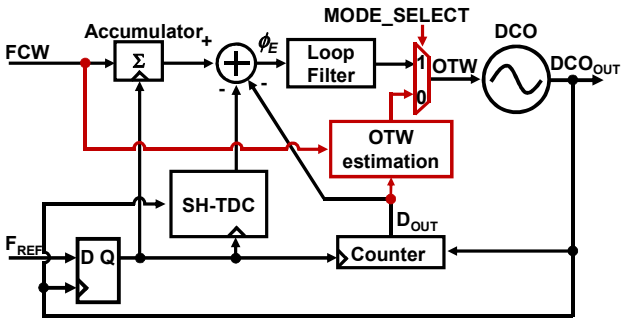

Figure 6. ADPLL with the proposed architecture.

III. Performance Evaluation

First, we measured the temperature characteristics of DCO fabricated in 65-nm CMOS process technology. Fig. 7 portrays a test chip of the DCO. The MPOSC and current source areas are respectively, 8.58×18.2 μm^2 and 98.5×48.5 μm^2. The measurement environment is portrayed in Fig. 8. Thermo stream alters the temperature condition of the test chip. FPGA outputs various OTWs into the test chip. DCO_{OUT} is measured and analyzed by mixed domain oscilloscope.

Fig. 9 depicts measurement results of output frequency in the same format as that used for Fig. 2. The measured temperatures are five points from -25°C to 75°C. The measurement result show the same tendency of simulation results presented in Fig. 2.

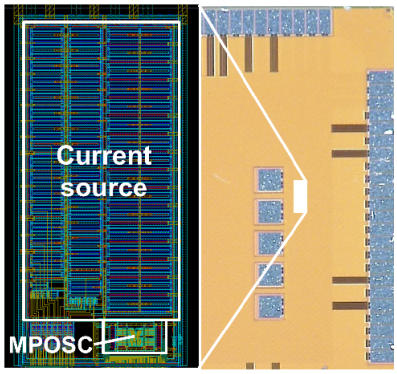

Figure 7. Chip photograph.

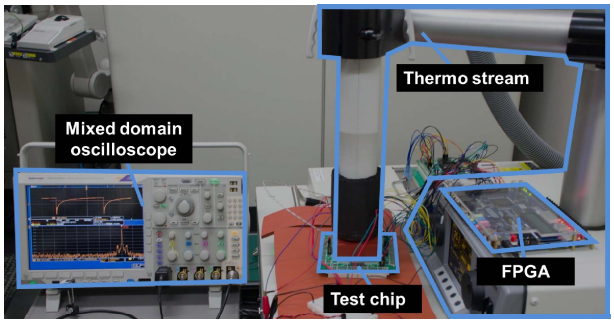

Figure 8. Measurement environment.

Based on the measurement result, we modeled the proposed temperature compensator and ADPLL in MATLAB. Fig. 10 shows the simulation result of temperature compensation. The estimation block suppresses the frequency error to less than 10 MHz. Fig. 11 presents the settling time of ADPLL. We compared the proposed method and the conventional method [6]. The simulation results show that the ADPLL with proposed scheme can achieve more than 53% settling time reduction.

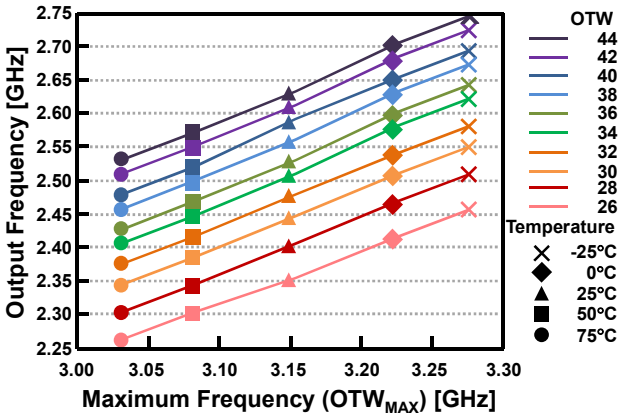

Figure 9. Temperature characteristics of DCO in measurements.

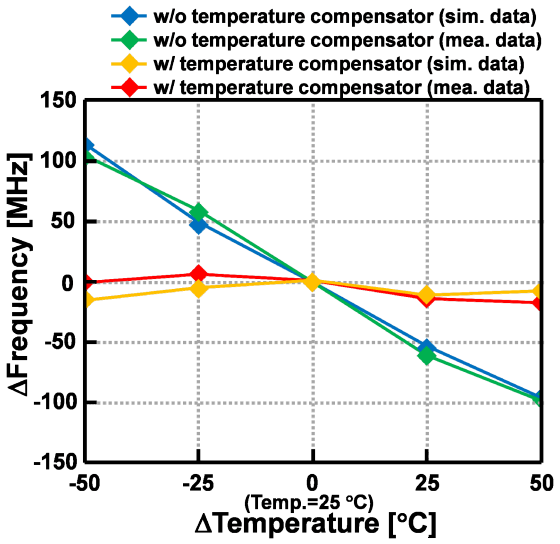

Figure 10. Simulation result of temperature compensation.

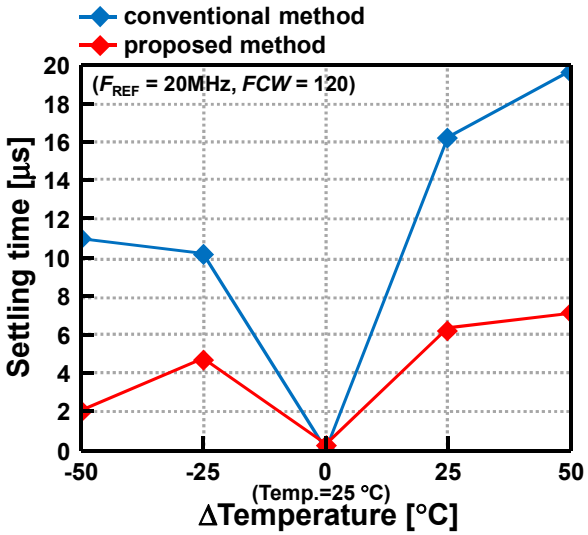

Figure 11. Simulation result of settling time.

IV. SUMMARY

We proposed the temperature-compensated method to reduce settling time using a LMS algorithm. The proposed scheme detects the temperature fluctuation by the output frequency of DCO, and estimates an optimal value of OTW. The simulation results show that the ADPLL with the proposed temperature compensator can achieve more than 53% settling time reduction and less than 10-MHz frequency error.

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