Normally-Off Technologies for Healthcare Appliance

Shintaro Izumi, Hiroshi Kawaguchi, and Masahiko Yoshimoto

Kobe University
Kobe, Japan, 6578501
Tel : +81-78-803-6629
e-mail : {shin, kawapy, yosimoto}@cs28.cs.kobe-u.ac.jp

Yoshikazu Fujimori

Rohm
Kyoto, Japan, 8891695
Tel : +81- 985-85-5111
yoshikazu.fujimori@lsi.rohm.co.jp

Abstract - Battery mass and power consumption of wearable system must be reduced because the key factors affecting wearable system usability are miniaturization and weight reduction. This report describes a wearable biosignal monitoring system using normally-off technologies to minimize the power consumption. Especially we focused on daily-life monitoring and electrocardiograph (ECG) processor. Our system employs Ferroelectric Random Access Memory (FeRAM) and Near Field Communication (NFC) for normally-off data logging and normally-off data communication. A robust heart rate monitor and Cortex M0 core are used to on-node processing for logging data reduction.

I Introduction

Because of the advent of an aging society in Japan, mobile health plays an ever more prominent role [1]. Daily-life monitoring is especially important in preventing lifestyle diseases, which have rapidly increased the number of patients and elderly people requiring nursing care. Our goal is the monitoring and display of vital signals and physical activity in daily life to improve users' quality of life and realize a smart society.

This report specifically describes a wearable biosignal monitoring system, which can acquire long-term instantaneous heart rate (IHR) data and an acceleration value. The physical activities in daily life (e.g., locomotive, household activities) are classifiable using a triaxial accelerometer [2]. The IHR, which is calculated from the interval of R-waves in electrocardiogram (ECG), is useful for heart disease detection, heart rate variation (HRV) analysis [3], and exercise intensity estimation [4].

The key factors affecting wearable system usability are miniaturization and weight reduction. Battery mass and power consumption must be reduced because battery mass dominates wearable systems. To reduce the power consumption, a wearable and wireless ECG telemetry system [5, 6] and single-chip ECG monitoring system LSIs [7-9] have been developed. However, strict limitations on power consumption and electrode distance of wearable ECG monitors render them sensitive to noise of various kinds. Especially, if a subject is not at rest (e.g. during exercise), the signal-to-noise ratio (SNR) of ECG signals will be significantly degraded.

To realize the low-power and noise-tolerant system, we proposed a ECG processor using normally-off architecture and robust IHR monitor [10].

II. Normally-off Wearable Biosignal Monitor Design

A. System Description and Architecture

Fig. 1 presents an overview of the wearable healthcare system, comprising the proposed ECG processor, Near Field Communication (NFC) tag IC, and accelerometer IC. The NFC is used for program loading, individual optimization, and data retrieval from the ECG processor.

Fig. 2 presents a block diagram showing the proposed ECG processor, which consists of an ECG sensing block, 64-Kbyte Ferroelectric Random Access Memory (FeRAM), 32-bit Coretex-M0 core, and extra interfaces.

The ECG sensing block has an analog front end (AFE), a 12-bit SAR ADC, and a robust IHR monitor. The AFE includes a 34-dB gain instrumental amplifier and a 20-dB gain amplifier. The ADC sampling rate can be set to 1 kSamples/s for ECG processing mode and 128 Samples/s for IHR monitoring mode.

The operating frequency of the Cortex M0 core, which is used for an on-node vital signal processing, is 24 MHz, whereas the operating frequency of other digital blocks is 32 kHz. The slow signals in the 32-kHz domain are synchronized at the low-speed bus to the 24-MHz domain. When the Cortex M0 core is in a deep sleep state, the on-chip 24-MHz oscillator is also stopped.

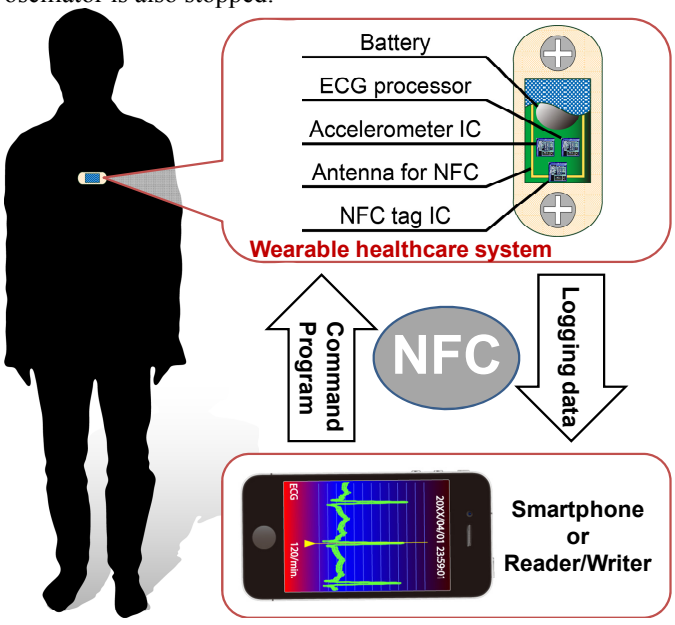

Fig. 1. Wearable healthcare system overview.

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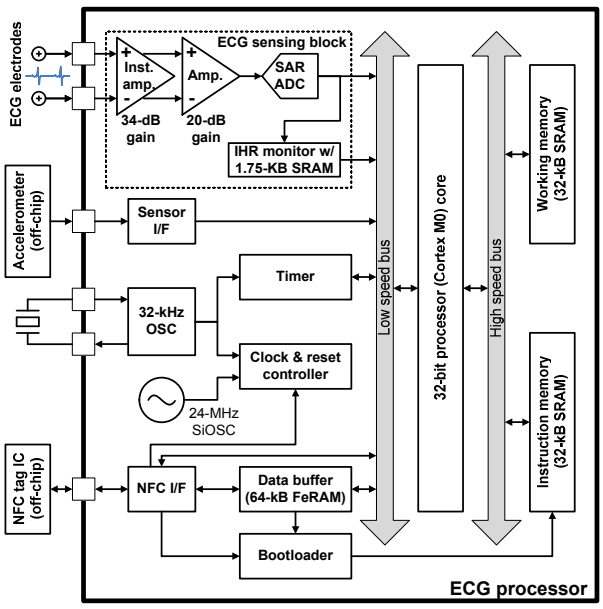


Fig. 2. Block diagram of ECG processor.

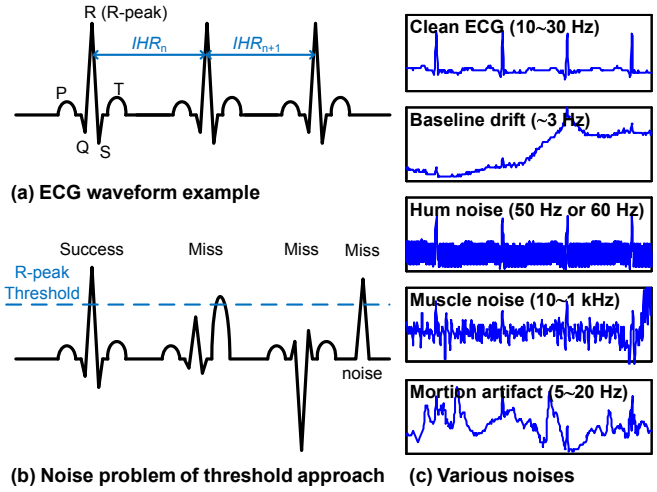


Fig. 3. Threshold based R-wave detection and its noise problems in wearable healthcare systems.

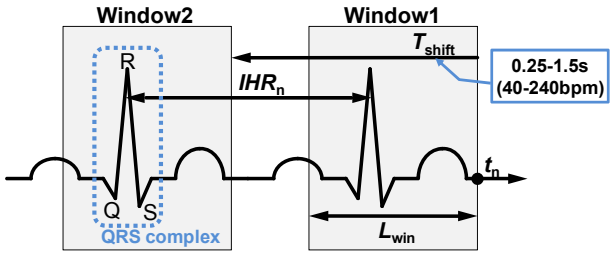


Fig. 4. IHR extraction with short-term autocorrelation (STAC).

B. *Normally-off data logging using FeRAM and IHR monitor*

Because the frequency range of vital signals is low (less than 1 kHz), both the standby power reduction and sleep time maximization are important to minimize the total power consumption. The 64-Kbyte FeRAM is integrated as a data buffer for daily life monitoring because the leakage current of the data buffer is dominant in the standby state. However, the FeRAM has larger read/write power, lower speed and endurance compared with SRAM. To mitigate these issues of FeRAM, our system has on-node IHR monitoring system and CM0 core to reduce the logging data. The detail of robust IHR monitor is described in Sect. III.

C. *Normally-off data communication using NFC*

The power consumption of transceiver circuits is ten or hundred times larger than other blocks, although the active time can be suppressed by data compression and on-node processing. The stand-by power of receiver circuit is also a problem. Our proposed system employs NFC to cooperate with smartphone (or a reader/writer). Several smartphones and tablet devices now support NFC technology.

Generally, a wireless transceiver consumes the greatest amount of power in the biosignal monitoring system. However, compared with Bluetooth Low Energy or ZigBee, the standby power of NFC is extremely small. Moreover, the active communication energy is only consumed on the reader/writer side when using a passive mode, in which only the initiator generates a carrier during communications [11]. In other words, the transceiver of our wearable biosignal monitor can achieve normally-off communication. In addition, NFC enables us to initiate communication without manually configuring the communication link, unlike Bluetooth [12]. The NFC also has high security because it has a short communication range. Some secure payment services already use NFC [12].

In our system, the NFC controller can update the stored program to configure the logging parameters. The logging data can be retrieved directly from the data buffer. The user can also directly access the low speed data bus to communicate with CM0. The logging start, logging stop, and system reset command are issued from a smartphone to CM0.

III Robust IHR Monitor

A. *IHR Extraction Algorithm*

The wearable ECG monitor is sensitive to extraneous noise because its electrodes are close together. The SNR of ECG signals will be especially degraded if a user is not at rest. Consequently, a sophisticated and costly analog front end is usually required. However, the feature and purpose of our approach is digital signal processing to reduce the performance requirements of the analog portion and to minimize the overall system power consumption.

Extracting R-waves (see Fig. 3(a)) with threshold determination is a general approach. Recently, various statistical approaches have been proposed for noise-tolerant threshold calculation such as using root-mean-squares (RMS) [13], standard deviations (SD), and mean deviations (MD) [14]. However, as depicted in Fig. 3, both misdetection and false detection are increased in the wearable healthcare system by noise from various sources such as myoelectric signals from muscle and electrode movement because the power consumption and electrode distance of the wearable sensor are strictly limited to reduce its size and weight.

Autocorrelation [15, 16] and template matching [17] are

more robust approaches to prevent incorrect detection because these algorithms use the similarity of QRS complex waveforms and have no threshold calculation process. Autocorrelation has been used in a non-invasive monitoring system [16]. However, the method necessitates numerous computations because it calculates the average heart-rate over a long duration (30 s). In our previous work, a short-term autocorrelation (STAC) technique was proposed for IHR detection [18].

Fig. 4 portrays IHR extraction using STAC. As depicted in Fig. 4 and (1–4), the IHR at time t_n (IHR_n) is obtained as a window shift length (T_{shift}) that maximizes the correlation coefficient between the template window and the search window (CC_n). The STAC method can improve the noise tolerance about 5.6 dB with a 95% success rate.

$$CC_n[T_{shift}] = w_1 \cdot \sum_{i=0}^{L_{win}-1} Q_w[t_n - i] \cdot Q_w[(t_n - T_{shift}) - i] \quad (1)$$

$$IHR_n = \underset{0.25\times F_s \le T_{shift} \le 1.5\times F_s}{\arg\max_{T_{shift}}} \{CC_n[T_{shift}]\} \quad (2)$$

$$L_{win} = 1.5 \times F_s \quad (3)$$

$$w_1 = \begin{cases} 1 & (T_{shift} \le 0.546 \times F_s) \\ 0.75 & (0.546 \times F_s < T_{shift} \le 0.983 \times F_s) \\ 0.5 & (0.983 \times F_s < T_{shift}) \end{cases} \quad (4)$$

In the equations presented above, F_s, L_{win}, and w_1 respectively denote the sampling rate (samples/s), the window length, and the weight coefficient. The value of T_{shift} is set as 0.25 s to 1.5 s because the heart rate of a healthy subject is 40 bpm to 240 bpm. The L_{win} is updated according to the estimated IHR to reduce the computational amount and to improve the IHR estimation accuracy. Then, the range of L_{win} and w_1 is determined by the maximum rate of the beat-to-beat variation, which is generally 20% in a healthy subject [19].

B. Hardware Implementation

We proposed the robust IHR monitor hardware, which employs two-step noise reduction technique. In the first stage, a quadratic spline wavelet transform (QSWT) [20] is used to mitigate the baseline drift and hum noise. The QSWT requires few calculations and low hardware cost because it can be implemented using only adders and shift operators. Fig. 5 presents a block diagram and frequency characteristics of the QSWT with 128-Hz sampling rate. The baseline drift and hum noise can be removed easily using QSWT. Unfortunately, it is difficult to remove the myoelectric noise and electrode motion artifacts only using QSWT because these frequency ranges are similar to the desired ECG signal.

Therefore, in the second stage, the IHR is extracted using the STAC method. The STAC is also implemented as dedicated hardware to minimize the power overhead. Fig. 6 presents the block diagram of the IHR monitor and STAC processing core. Each STAC core has CC buffer to store the intermediate value of $CC_n[T_{shift}]$ in (1). The CC buffer is updated in synchronization with ADC output (see Fig. 7). Since the L_{win} is 1.5 s and because IHR is updated every second, two STAC cores alternately calculate IHR with 0.5 s overlap.

The gate level simulation result shows the IHR monitor block, which contains QSWT, two STAC cores, and SRAMs, consumes 1.21 μA. The digital logic and SRAMs respectively consume 0.26 μA and 0.95 μA.

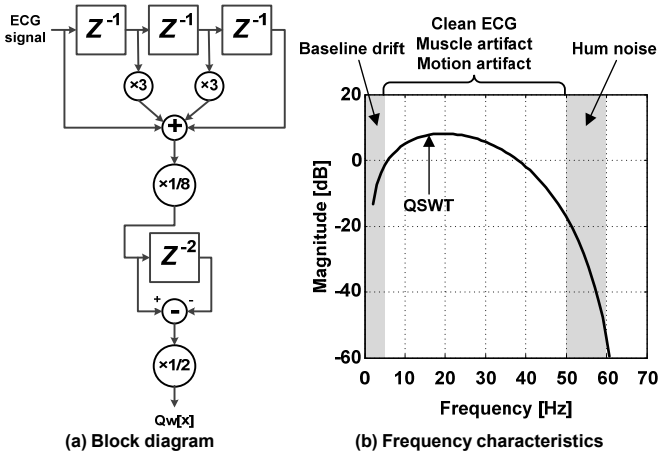


Fig. 5. Block diagram and frequency characteristics of QSWT.

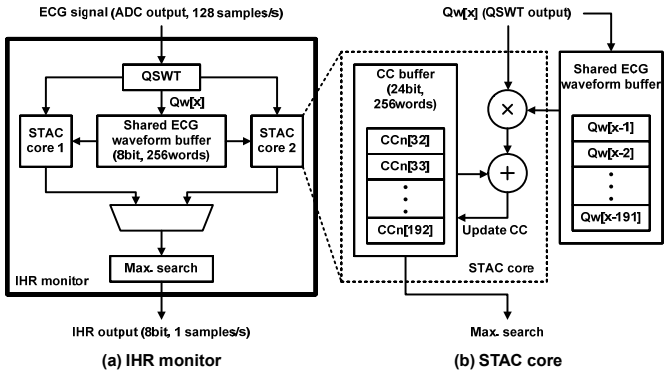


Fig. 6. Block diagram of robust IHR monitor.

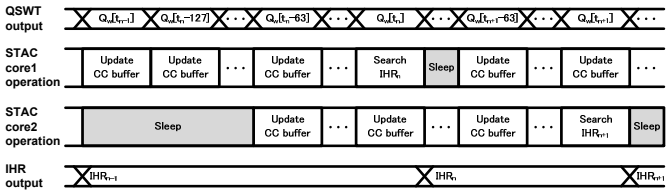
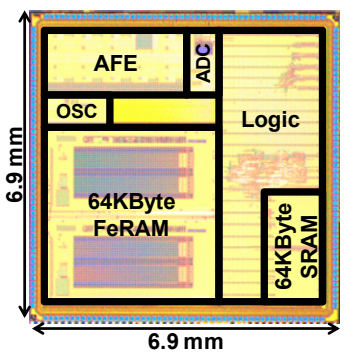


Fig. 7. Timing chart of IHR extraction.



Technology		130-nm CMOS
Supply voltage		1.2V (Digital, SRAM, ADC, AFE)
		3.0V (FeRAM, 32kHz OSC, I/O)
Chip area		6.9 mm × 6.9 mm
Frequency		24 MHz (for MCU)
		32 kHz (for other blocks)
MCU		32-bit Cortex M0
On chip memory		64-KB FeRAM (for logging data)
		64-KB SRAM (for MCU)
		1.75-KB SRAM (for IHR detector)
ADC	Resolution	12 bit
	Current	0.5 μA@128 S/s, 1.4 μA@1 kS/s
AFE	Gain	54 dB
	Bandwidth	0-100 Hz
	Current	3.4 μA
Total current		12.7 μA (for heart rate logging)

Fig. 8. Chip photograph and chip specifications.

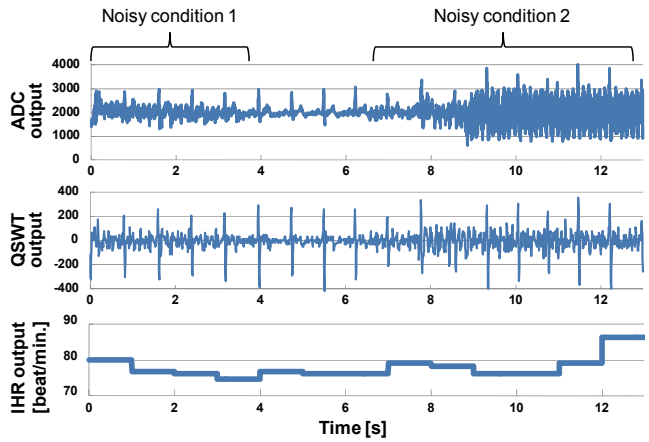


Fig. 9. Measured waveform of IHR monitor in a noisy condition.

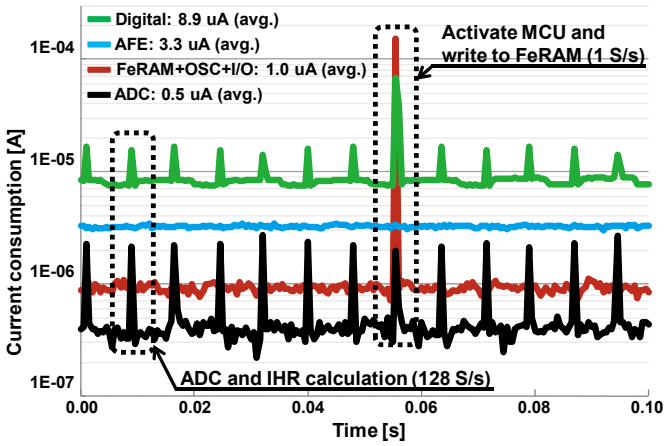


Fig. 10. Measurement result of current consumption with a heart rate logging application.

IV. Implementation Result

The test chip is fabricated using 130-nm CMOS technology. Fig. 8 presents a chip photograph and a performance summary. The operating voltage is 1.2 V for AFE, ADC, SRAM, 24-MHz oscillator, and digital blocks. The FeRAM, 32-KHz oscillator, and IO circuits are operated with 3.0 V supply voltage.

To demonstrate the test chip performance, we implemented a heart rate logging application. As portrayed in Fig. 9, the IHR is extracted correctly in a noisy condition. Fig. 10 portrays the current consumption with a heart rate logging application. In this experiment, the ADC sampling rate and the logging interval of IHR are set respectively to 128 Samples/s and 1 Sample/s. Then the AFE, 32-kHz OSC, and Timer block are always activated. The measurement results show that the test chip consumes 13.7 μA on average for the heart rate logging application. The peak current, which is consumed when the Cortex and FeRAM are activated to store the logging IHR data every second, is less than 1 mA.

Acknowledgments

This research was supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy an Industrial Technology Development Organization (NEDO).

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