A 40-nm 0.5-V 20.1-μW/MHz 8T SRAM with Low-Energy Disturb Mitigation Scheme

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Abstract

This paper presents a novel disturb mitigation scheme which achieves low-power and low-voltage operation for a deep sub-micron SRAM macro. The classic write-back scheme overcame a half-select problem and improved a yield; however, the conventional scheme consumed more power due to charging and discharging all write bitlines (WBLs) in a sub block. Our proposed scheme consists of a floating bitline technique and a low-swing bitline driver (LSBD). This scheme decreases active leakage and active power by 33% and 32% at the FF corner, respectively. In other process corners, more active power reduction can be expected. We fabricated a 512-Kb 8T SRAM test chip that operates at a single 0.5-V supply voltage. The proposed scheme achieves 8.8-μW/MHz active energy in a write cycle and 72.8-μW leakage power, which are 35% and 26% better than the conventional write-back scheme. The total energy is 20.1 μW/MHz at 0.5 V in a 50%-read/50%-write operation.

Keywords: SRAM, 8T, disturb, half-select, write back

Introduction

As process technology has been scaled down, it has become much more difficult to realize a stable bitcell design in a 6T SRAM due to the tradeoff between read and write margins [1]. An 8T bitcell with a dedicated read port is proposed to neglect the 6T's read margin, which achieves low-voltage operation in nature. The separation of read and write ports frees the bitcell design of the read/write tradeoff; the area of the 8T cell is expected to be smaller than that of the 6T cell in a future process [2]. Although low-voltage and high-yield 8T SRAMs under 1.0-V operation are proposed [3-5], the power per operation cycle (= energy) is larger than that in 6T SRAMs [5-7]; this is because an assist circuit needs to be implemented to avoid the disturb (= half-select) problem. Fig. 1 shows the tendency of the power per cycle among recent SRAMs. Our research object is to achieve a low-voltage and low-energy SRAM: 0.5-V and sub-100 μW/MHz/Mb operation is the target.

Proposed Disturb Mitigation Scheme

To reduce the extra power for the disturb, we propose a new disturb mitigation scheme: (1) a floating write bitline (WBL) with precharge-less equalizer, and (2) a low-swing bitline driver (LSBD) with nMOS pull-up transistors for the WBLs.

The proposed 8T SRAM employs a hierarchical read bitline (RBL) structure and the number of cells per RBL is 16 for stable read operation, as illustrated in Fig. 2. In the read operation, a read enabling (RDE) signal is activated, and then a global RBL (GRBL) is discharged when an RBL is pulled down.

In the proposed scheme, the active power in the write cycle is reduced and the leakage power in the read/write operation is also improved. In the half-selected cells, the column line enabling signals (CLEs) are low in the unselected columns and the driver disable signal (DRN) is pulled down in the selected row. Thus, the LSBD pulls up or down each WBL by the nMOSes. Fig. 4 portrays the array configuration of the proposed SRAM in which the CLEs and DRNs are horizontally and vertically connected, respectively. In the selected column, the CLEs are activated, and a write driver drives WBLs instead of the LSBD.

Fig. 3 shows the waveforms in the write cycle; the proposed scheme and conventional write-back scheme [8] are compared. In the proposed scheme, the WBLs are floating not only in a standby mode but also in an activated mode, and their voltage is at an intermediate voltage between the ground and supply voltage. After the LSBD pulls up a WBL (or WBLN) with an nMOS and the WBL (or WBLN) level goes up to "VDD – Vtn", some disturb current flows through the access gate from a "high" internal node. However, the "high" node is not flipped and keep the original datum because the other internal node is strongly grounded. Consequently, the LSBD has an advantage to reduce the active power without any area overheads: The half-selected cell is not flipped and the WBL swing is small in the write cycle. To save more power, the RDE is sustained low in the write operation and the GRBL does not swing in the proposed disturb mitigation scheme. The delay penalty derived from the GRBL is also reduced.

We investigated the margins of the half-select cells with one-million Monte-Carlo analyses at the five process corners and three temperatures at 0.5 V. The fail bit counts (FBC) in Table I show that the SS corner at low temperature is the worst case and the yield is 4.29σ. Fig. 5 illustrates that a pulled-up WBL level depends on Vtn; if nMOS is fast, the Vtn drop is small, the write assist becomes effective. On the other hand, a slow nMOS can save power because its swing is small; the enlarged margin and saving power are a tradeoff. Fig. 6 portrays the active power reduction over the conventional write-back scheme at write cycle. The active power is reduced by 32%, 47%, and 60% at FF, CC and SS corners, respectively. Fig. 7 shows the simulation results of the leakage power at activated cycle in 8T bitcells. The leakage power in the worst corner is improved by 33% thanks to the low-swing feature of the LSBD.

Measurement Results

We fabricated a 512-Kb 8T SRAM macro using a 40-nm CMOS bulk process (Fig. 8). The 8T bitcell area is 0.706 μm using a logic rule. The transistor width of an access gate is doubled to enhance the write margin while the others are minimum sizing.

Fig. 9 shows a measured Shmoo plot of the proposed 8T SRAM macro. The minimum operating voltage is 0.5 V at an access time of 160 ns at room temperature (RT). Figs. 10 and 11 illustrate that the measured leakage power and active energy are improved by 26% and 35% at the supply voltage of 0.5 V. The active energy in the write cycle is 8.8 μW/MHz. The total energy is 20.1 μW/MHz when the read and write cycles are fifty-fifty at 0.5V. Table II summarizes its characteristics of the implemented SRAM macros.

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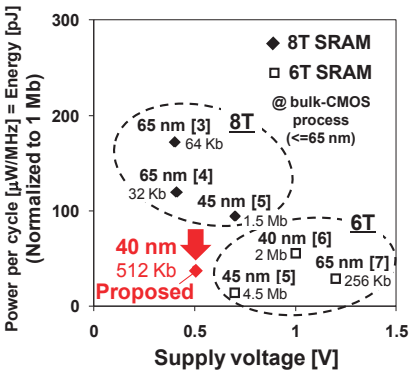

Fig. 1. Supply voltages versus power among low-power bulk-CMOS SRAMs [3-7].

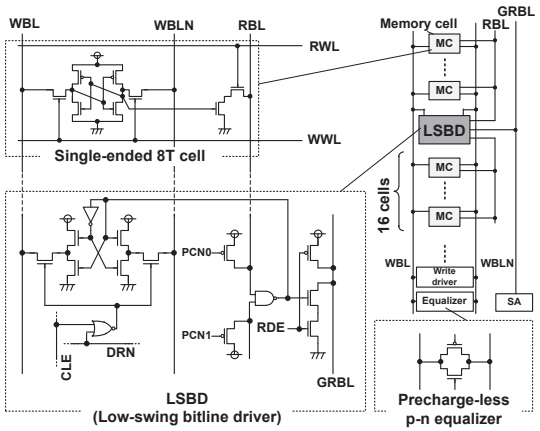

Fig. 2. Proposed low-swing bitline driver (LSBD) and the circuit diagram.

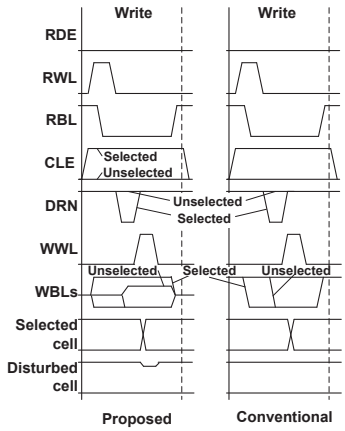

Fig. 3. Operating waveforms in write cycle.

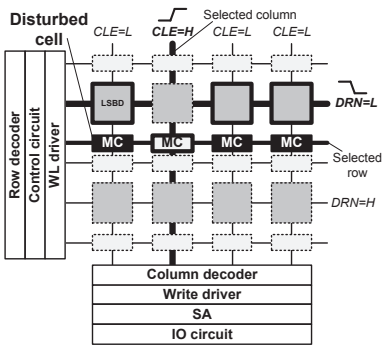

Fig. 4. Array configuration of the proposed SRAM.

TABLE I. Fail bit count results.

Fail bit count @ 0.5 V (1M Monte-Carlo)		Temperature [°C]		
		-40	25	125
Global corner	FF	0	0	0
	FS	0	0	0
	CC	0	0	0
	SF	0	0	0
	SS	19	0	0

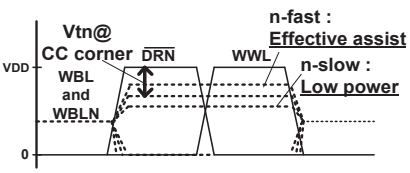

Fig. 5. Pulled-up WBL level dependence on the global corner.

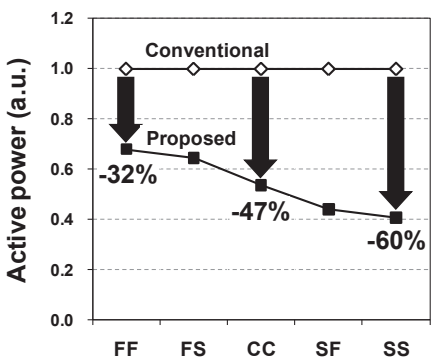

Fig. 6. Active power reduction in WBLs at room temperature (RT).

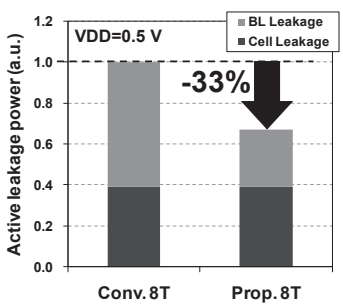

Fig. 7. Active leakage power at FF corner and 125 °C.

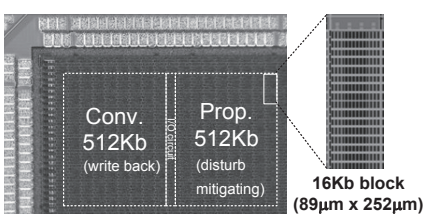

Fig. 8. Micrograph of the test chip.

TABLE II. Features of test chips.

Technology	40 nm bulk CMOS
Macro size	0.723 mm x 1.010 mm
Macro configuration	512 Kb (16Kb x 4 x 8), 16 bits/word
Cell size	0.706 μm (logic rule)
# of cells/BL	16 (RBL), 128 (WBL)
Density	701 Kb/mm^2
Power supply	0.5-0.8 V
Write active power	8.8 uW/MHz @ 0.5 V, RT
Total power (R/W=50/50)	20.1 uW/MHz @ 0.5 V, RT
Access time	160 ns @ 0.5 V, 4.5 ns @ 0.8 V

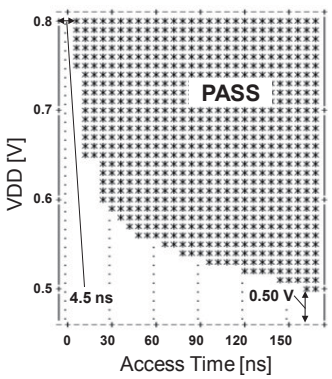

Fig. 9. Shmoo plot of the proposed 512 Kb SRAM macro.

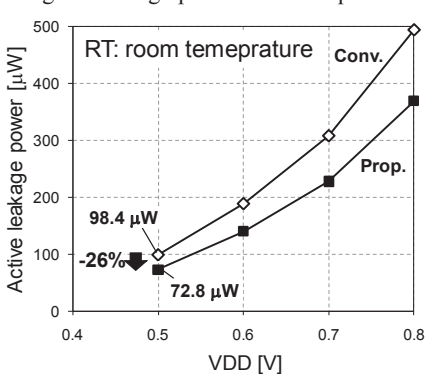

Fig. 10. Measured active leakage power at RT.

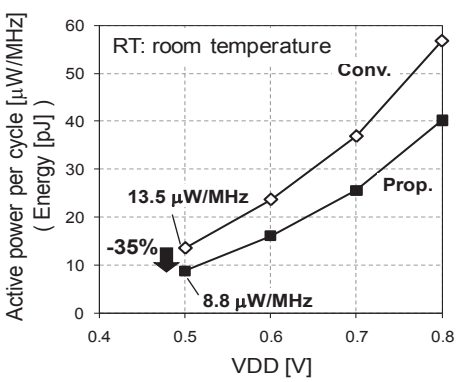

Fig. 11. Measured active energy without leakage in write cycle at RT.