A Counter-based Read Circuit Tolerant to Process Variation for 0.4-V Operating STT-MRAM

YOHEI UMEKI1,a) KOJI YANAGIDA1 SHUSUKE YOSHIMOTO2 SHINTARO IZUMI1 MASAHIKO YOSHIMOTO1 HIROSHI KAWAGUCHI1 KOJI TSUNODA3 TOSHIHIRO SUGII3

Received: December 4, 2015, Revised: March 14, 2016, Accepted: May 9, 2016

Abstract: In this paper, in order to realize 0.4 V operation of STT-MRAM, we propose the counter base read circuit. The proposed read circuit has tolerance for process variation and temperature fluctuation by changing dynamically the load curve in a time-axis at the read operation. We confirmed that the proposed read circuit can operate at the conditions of five process corners (TT, FF, FS, SF, and SS) and three temperatures (−20°C, 25°C, and 100°C) by HSPICE simulations. At the condition of TT corner and 25°C, read time of the proposed circuit is 271 ns, and energy consumption is 1.05 pJ at “1” read operation and 1.23 pJ at “0” read operation.

Keywords: non-volatile memory, STT-MRAM, Low-Voltage, process variation tolerance

1. Introduction
The capacity of embedded memory on a chip has kept increasing. It is important to reduce the leakage power of embedded memory for low-power LSIs. In fact, the ITRS predicts that the leakage power in embedded memory will account for 40% of all power consumption by 2024 [1]. A spin transfer torque magnetoresistance random access memory (STT-MRAM) is promising for use as non-volatile memory to reduce the leakage power. It is useful because it can function at low voltages and has a lifetime of over 1016 write cycles [2]. In addition, making STT-MRAM suitable for use in high-density products [3], [4], [5], [6], [7]. STT-MRAM uses magnetic tunnel junction (MTJ) device. MTJ has magnetoresistance and that value can be changed by MTJ’s state.

The state of MTJ determined by the magnetization direction of the fire layer which is one of the layers consisting the MTJ. The MTJ has two states, parallel and anti-parallel states. In the parallel state, the magnetoresistance value of the MTJ becomes higher than that of anti-parallel state.

2. Conventional Read Circuit

Figure 1 shows the conventional read circuit schematic [8]. The node “S” is the input of the sense amplifier. The voltage of the node “S” determined by the balance between load current (I LOAD) and read out current (I P, I AP). The resistance value of bit cell is dependent on the datum. Therefore, the cell current has two patterns. Figure 2 presents current characteristics of the conventional circuit at TT and FS corners, 0.4 V VDD.

This conventional circuit makes the 130-mV difference between the parallel and anti-parallel states at TT corner.

However, at the FS corner, there is only 40-mV difference between the two states. This voltage difference is too small to be read out for a sense amplifier. As well, it is difficult to make an appropriate reference voltage for every process corner. This is the reason the conventional circuit cannot operate correctly in the low voltage area.

3. Proposed Read Circuit

Figure 3 shows the 1-Mb STT-MRAM macro with the proposed bitline digitize circuit. The proposed read circuit converts a bitline voltage, which depends on a target cell datum, to a digital value. To compare with the cell data, two reference cell columns are further added. All cells in the reference “0” column have data “0” whereas all data are “1” in the reference “1” column. In read operation, both are read out at the same time, and they are changed to digital values in the proposed read circuit. Then, the reference value is determined as an average of their digital values. After that, the target cell’s bitline voltage is changed to digital value and compared with the reference value. The output data are decided by comparing the digital values.

Figure 4 shows the dynamic load circuit. The dynamic load circuit consists of negative resistance circuit and four boosting nMOSes. These four boosting nMOSes have different current driving capabilities. When the minimum is set to 1, the ratio of the current drive capabilities is 1:2:4:8. The dynamic load circuit has a characteristic that the load curve changes over time dynamically. The voltage of node “S” is changed by the dynamic load circuit. It means the input of the ring oscillator changes dynamically. In addition, the bitline voltage can be digitized by counting number of oscillations, because the frequency of the ring oscillator depends on the voltage of node “S”. Therefore, the data of
the target cell can be determined by combining with the bitline digitize circuits.

The left side of Fig. 5 shows the current characteristics in the case of LE<3:0>=“1001”. In this proposed circuit, the supply current from the negative resistance circuit (I_{neg}) will not decrease uniformly. I_{neg} has a characteristic that decreases once it has increased as the voltage of the node “S” increases. This proposed circuit can make the larger voltage difference between the low and high states by summing up the input current from the negative resistance circuit and the NMOS load circuit. This proposed circuit corresponds to the variation of characteristics by sequentially switching the LE signal from LE<3:0>=“0000” to “1111”. The right side of Fig. 5 shows the current characteristics of dynamic load current at all steps.

Figure 6 shows transient simulation results of the proposed circuit at TT corner, 25°C. In this simulation, the LE signal is switched from “0000” to “1111” in every 100 ns. In this case, if the target cell datum is 1 (=AP state), the oscillator stops in LE<3:0>=“0000” because the input voltage becomes higher than their threshold voltage. But if the target cell datum is 0 (=P state), the oscillation continues until LE<3:0>=“1011”. Though, the data can distinguish by counting the number of oscillations.

4. Simulation Results

We simulated the proposed circuit in the all process corners (TT, FF, FS, SF, SS). Temperature conditions are –20°C, 25°C and 100°C. The operating voltage setting is 0.4 V. As the characteristics of the MTJ, we configured the MR ratio is 100%. The resistance values are 3.5 kΩ in the parallel state, and 7 kΩ in the anti-parallel state. We evaluated the bitline digitize circuit with dynamic load circuit for accuracy, readout time and energy consumption.

Table 1 show the count of the ring oscillator in each condition.
Table 2 Read time and energy.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>AP</td>
</tr>
<tr>
<td>TT</td>
<td>-20</td>
<td>666.67</td>
<td>2.14</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>271.19</td>
<td>1.05</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>106.67</td>
<td>0.60</td>
</tr>
<tr>
<td>FF</td>
<td>-20</td>
<td>163.27</td>
<td>0.85</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>90.40</td>
<td>0.57</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>56.94</td>
<td>0.56</td>
</tr>
<tr>
<td>FS</td>
<td>-20</td>
<td>516.13</td>
<td>1.95</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>231.88</td>
<td>1.06</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>101.27</td>
<td>0.71</td>
</tr>
<tr>
<td>SS</td>
<td>-20</td>
<td>4000</td>
<td>7.11</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>1066.67</td>
<td>2.61</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>258.07</td>
<td>0.90</td>
</tr>
</tbody>
</table>

This result shows that the proposed circuit is possible to distinguish between the P and AP states at 0.4 V VDD. However, in particular at the SS corner, the number in the count difference between the P and AP is small. This result implies that the proposed circuit needs more than 100 ns in switching time of the LE signal.

Table 2 shows the energy consumption and cycle time in the read operation. In this simulation, we assumed the read operation is finished when the difference of the count between the two states becomes 10. In the case of TT corner, 25°C, the readout time is 271 ns. The energy consumption of “0” read is 1.23 pJ and “1” read is 1.05 pJ respectively. In the −20°C cases, the readout time becomes longer than the other temperature cases. It degrades the energy consumptions to the other temperature conditions.

5. Chip Implementation and Conclusion

We fabricated a 4-Mb STT-MRAM using a 65-nm process technology. The left side of Fig. 7 shows the layout of test chip and the right side shows TEM micrograph of the MTJ. The area of proposed circuit is 180 µm². It means that the area overhead of 1-Mb macro is 0.53%. In this test chip, the charge pump circuit provides a 1.6-V boosted voltage to a gate of an access transistor, which suppresses effects of a threshold voltage variation of the access transistor and a cell current variation, thus draws more readout current. In the TEM micrograph, thin and white area is tunnel insulating film. The free layer and pinned layer are composed almost entirely of CoFeB.

In this paper, we proposed the counter base read circuit for 0.4-V operating STT-MRAM. The proposed circuit is confirmed that operates in all process corners and three temperature conditions at 0.4-V VDD by the simulation. In the case of TT, 25°C, the cycle time is 271 ns and energy consumptions are 1.23 pJ in “0” read operation and 1.05 pJ in “1” read operation.

Acknowledgments

We would like to thank Toppan Technical Design Center Co., Ltd., for chip implementation. This work was performed as the “Ultra-Low Voltage Device Project” of the Low-power Electronics Association & Project (LEAP) funded and supported by METI and NEDO. Part of the device processing was performed by AIST, Japan.

References


Yohei Umeki was born on December 20, 1985. He received his B.E. and M.E. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2012 and 2014. He is currently Ph.D. in Graduate School of System Informatics of Kobe University. His current research is on low-power SRAM and low-voltage MRAM designs.

Koji Yanagida received his B.E. and M.E. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2011 and 2013. His current research is on low-voltage MRAM designs and low-power FeRAM designs.
Shusuke Yoshimoto received his B.E. and M.E. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2009 and 2011, respectively. He earned Ph.D degree in Engineering from the university in 2013. He was a JSPS research fellow from 2013 to 2014. He worked in Department of Electrical Engineering at Stanford University as a Postdoc from 2013 to 2015. Since 2015, he has been an Assistant Professor in The Institute of Scientific and Industrial Research at Osaka University. His current research interests include biomedical signal processing, flexible electronics, organic circuit design, nanoelectronics, soft error, low-power and robust memory design. He was a recipient of 2011 and 2012 IEEE SSCS Japan Chapter Academic Research Awards, 2013 IEEE SSCS Kansai Chapter IMFEDK Student Paper Award, and 2013 CICC Student Scholarship Award. He served as a program committee student member in IEICE Integrated Circuit Design in 2013.

Shintaro Izumi received his B.Eng. and M.Eng. degrees in Computer Science and Systems Engineering from Kobe University, Hyogo, Japan, in 2007 and 2008, respectively. He received his Ph.D degree in Engineering from Kobe University in 2011. He was a JSPS Research Fellow at Kobe University from 2009 to 2011. Since 2011, he has been an Assistant Professor in the Organization of Advanced Science and Technology at Kobe University. His current research interests include biomedical signal processing, communication protocols, low-power VLSI design and sensor networks. He is a member of the IEEE, IEICE and IPSJ.

Masahiko Yoshimoto joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan, in 1977. From 1978 to 1983 he was engaged in the design of NMOS and CMOS static RAM. Since 1984 he has been involved in the research and development of multimedia ULSI systems. He received his Ph.D. degree in Electrical Engineering from Nagoya University, Nagoya, Japan, in 1998. In 2000, he become a professor at the Dept. of Electrical & Electronic System Engineering in Kanazawa University, Japan. Since 2004, he has been a professor at the Dept. of Computer and Systems Engineering in Kobe University, Japan. His current activity is focused on the research and development of ultra low-power multimedia and ubiquitous media VLSI systems and a dependable SRAM circuit. He served on the program committee of the IEEE International Solid State Circuit Conference from 1991 to 1993. He was also a chair of the IEICE Electronics Society Technical Committee on Integrated Circuits and Devices from 2011-2012. He received R&D100 awards from an R&D magazine for the development of the DISP and the real-time MPEG2 video encoder chipset in 1990 and 1996, respectively.

Hiroshi Kawaguchi received his B.Eng. and M.Eng. degrees in Electronic Engineering from Chiba University, Chiba, Japan, in 1991 and 1993, respectively, and received a Ph.D. degree in Electronic Engineering from the University of Tokyo, Tokyo, Japan, in 2006. He joined Konami Corporation, Kobe, Japan, in 1993, where he developed arcade entertainment systems. He moved to the Institute of Industrial Science, the University of Tokyo, as a Technical Associate in 1996, and was appointed as a Research Associate in 2003. In 2005, he moved to Kobe University, Kobe, Japan. Since 2007, he has been an Associate Professor with the Department of Information Science at Kobe University. He is also a Collaborative Researcher with the Institute of Industrial Science, the University of Tokyo. His current research interests include low-voltage SRAM, RF circuits and ubiquitous sensor networks. Dr. Kawaguchi was a recipient of the IEEE ISSCC 2004 Takuo Sugano Outstanding Paper Award and the IEEE Kansai Section 2006 Gold Award. He has served as a Program Committee Member for the IEEE Custom Integrated Circuits Conference (CICC) and as an Associate Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences and IPSJ Transactions on System LSI Design Methodology (TSLDM). He is a member of the IEEE, ACM, IEICE and IPSJ.
Koji Tsunoda received his B.S. and M.S. degrees in Electronics Engineering from the University of Tokyo, Tokyo, Japan, in 1995 and 1997, respectively. In 1997, he joined Fujitsu Laboratories Ltd., Atsugi, Japan, where he was engaged in the research and development of embedded memory devices. He was also a visiting scholar at Stanford University, California, from 2005 to 2006. He received his Ph.D. in Electronics Engineering from Tohoku University, Sendai, Japan, in 2010. He joined the Low-power Electronics Association & Project (LEAP) in 2010, and his present activities include the development of spin-transfer torque magnetoresistive RAM.

Toshihiro Sugii received his B.S., M.S. and Ph.D. degrees in Electrical Engineering from Tokyo Institute of Technology in 1979, 1981 and 1991, respectively. In 1981, he joined Fujitsu Laboratories Ltd., Japan, where he was engaged in the development of CMOS devices. In 2010, he joined the Low-power Electronics Association & Project (LEAP), Japan, where he is directing a national project on STT-MRAM. Dr. Sugii is a fellow of the Japan Society of Applied Physics and a member of the IEEE Electron Device Society.

(Recommended by Associate Editor: Takeshi Kumaki)