0.5V 電源電圧における低スタンバイ電流 CMOS 設計法

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あらまし　　低消費電力のために 0.5V 程度の電源電圧にしたとき、MOSFET が動作するためには閾値を 0.1～0.2V にしなければならない。しかしこの時、スタンバイ時にゲートあたり 10nA、つまり 100 万トランジスタで 10mA のリーク電流が流れてしまう。本研究では、このリーク電流を抑えるための回路として super cut-off CMOS(SCCMOS)を提案する。SCCMOS を用いることで電源電圧 0.5V～0.8V、閾値 0.1V～0.2V でスタンバイ時のリーク電流がゲートあたり 1pA 以下に抑えることができる。

キーワード　　低消費電力、スタンバイ電流、SCCMOS、パストランジスタ

A CMOS Scheme for 0.5V Supply Voltage with Pico-Ampere Standby Current

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Abstract　　If a VLSI should be operated in 0.5V~0.8V VDD range for low-power consumption, the threshold voltage of MOSFET's, VTH, should be well below 0.5V to turn the MOSFET's on. The low VTH like 0.1V~0.2V, however, causes 10nA order subthreshold leakage current per logic gate in a standby mode, which leads to 10mA order standby current for one million gate VLSI's. In this paper, super cut-off CMOS (SCCMOS) circuit is proposed to overcome this situation. With the SCCMOS, an operation is possible under 0.5V~0.8V VDD with 0.1V~0.2V VTH and at the same time pA order standby current per logic gate can be achieved.

key words　　Low power, Standby current, SCCMOS, Pass-transistor

I. Introduction

Recently, low-power requirements are getting stronger in VLSI designs. Since the power consumption of CMOS VLSI's quadratically depends on the supply voltage, low-voltage circuits have been exploited. If a VLSI should be operated in 0.5V~0.8V VDD range for low-power consumption, the threshold voltage of MOSFET's, VTH, should be well below 0.5V to turn the MOSFET's on. The low VTH like 0.1V~0.2V, however, causes 10nA order subthreshold leakage current per logic gate in a standby mode, which leads to 10mA order standby current for one million gate VLSI's. This hinders an application of the VLSI's to a mobile equipment powered by a small battery. In this paper, super cut-off CMOS (SCCMOS) circuit is proposed to overcome this situation. With the SCCMOS, an operation is possible under 0.5V~0.8V VDD with 0.1V~0.2V VTH and at the same time pA order standby current per logic gate can be achieved.

II. SCCMOS Circuits

Figure 1 shows a circuit diagram of the SCCMOS for a PMOS insertion case. Low-V_{TH} PMOS, M1, whose V_{TH} is 0.1V~0.2V is inserted in series to a low-V_{TH} circuit block. The gate of the inserted PMOS is applied 0V in an active mode and is overly driven up to about 0.9V in a standby mode. The PMOS insertion case is explained and verified by experiments in this paper. This is because a p-type substrate is widely used and then the body of PMOSFET's can be connected to the virtual V_{DD} line, which does not require another line for the PMOS body bias. Therefore, modification to a cell library is not needed. An NMOS insertion case is also possible where the gate of the inserted NMOS is driven to about -0.4V in a standby mode to fully cut off the leakage current. The gate bias generator can be without a feedback loop as is shown in the figure because an exact control of the voltage is not needed. In Figure 1, a technique to reduce the voltage across the gate oxide is shown which can be used when the reliability of the oxide is an issue.

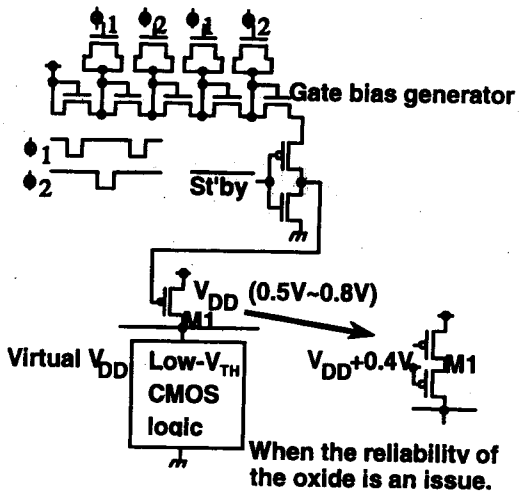

Fig.1 Super cut-off CMOS(SCCMOS) scheme

There have been other ideas to realize a fast operation in low-V_{DD} region. One of the schemes, multi-threshold CMOS (MTCMOS) [1] uses high-V_{TH} device (say 0.6V~0.7V) in series to low-V_{TH} transistor circuits to fully cut off the leakage current in a standby mode. The MTCMOS does not work below 0.7V V_{DD} because the high-V_{TH} MOSFET does not turn on. Another scheme named variable threshold CMOS (VTCMOS) [2,3] apply backgate bias to fully cut off the subthreshold current in a standby mode. The scheme can not be applied to fully-depleted SOI devices and is difficult to be applied to partially-depleted SOI circuits due to the overhead to apply the body bias. Another drawback is that the VTCMOS requires modifications to cell libraries to separate the substrate/well bias lines from the supply voltage lines, being different from the SCCMOS.

On the other hand, dynamic threshold MOS (DTMOS) [4] suffers from 10mA-range leakage current at 0.5V~0.7V V_{DD} for million-gate VLSI's in a standby mode because of the inherent forward bias current of *pn*-junctions. The proposed SCCMOS scheme can be used in conjunction with the DTMOS to cut off the leakage current in a standby mode and enjoys the high-speed nature of the DTMOS in an active mode. Again, VTCMOS can not be used in

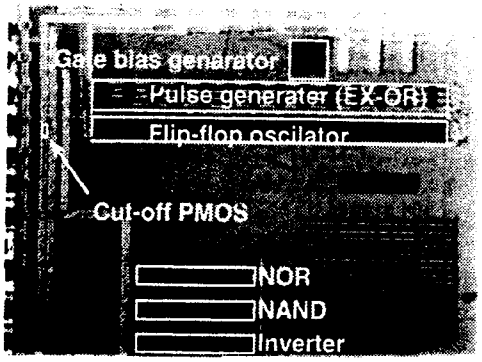

Fig.2 Microphotograph

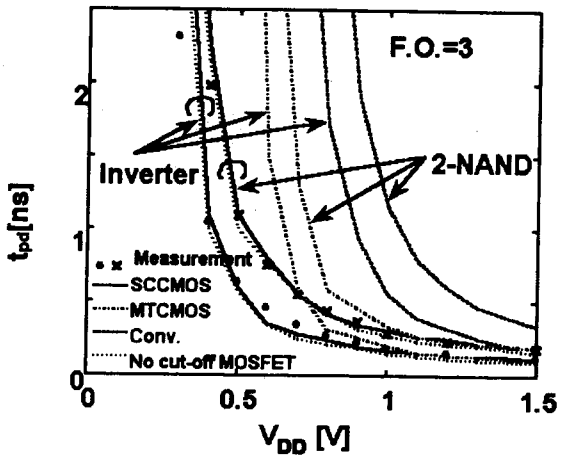

Fig.3 Speed of inverter and NAND with SCCMOS

conjunction with the DTMOS where a backgate is always fixed to a gate voltage.

III. Measurement Results

A test chip to demonstrate the feasibility of the SCCMOS was fabricated using 0.3μm triple metal CMOS process with 0.2V V_{TH} for both PMOS and NMOS, whose microphotograph is shown in Figure 2. The measured operation speed of an inverter and 2-input NAND gate with fanout of three is shown in Figure 3. The gate width of all the MOSFET's in the logic gates is 2.4μm and the gate width of the serially inserted MOSFET is 10μm. It is clear that the SCCMOS further pushes the low voltage operation limit of CMOS logic over the MTCMOS.

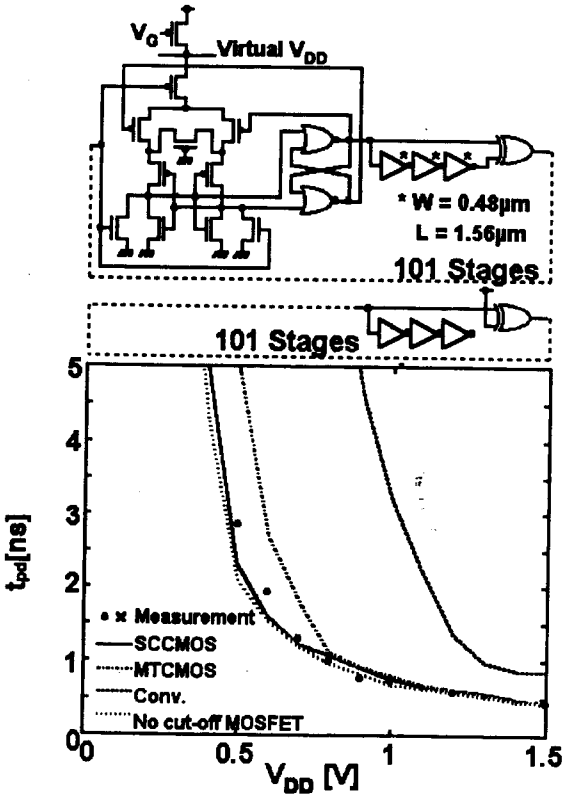

Fig.4 Flip-flop for SCCMOS and operation waveforms

The measured leakage current is below 1pA per gate in a standby mode. The gate bias generator is 100μm x 100μm in size and the power consumption is 0.1μA with the pumping frequency of 10KHz. The active power consumption of the fanout 3 NAND gate is 8fJ per switching.

When the circuit is in a standby mode, the virtual V_{DD} goes down to 0V due to the high leakage of the low-V_{TH} circuit block. Then flip-flops in the low-V_{TH} circuit block lose their stored information in a standby mode. One way to solve the problem at a system level is to scan all the information stored in flip-flops into a memory before entering the standby mode and to restore the information back into flip-flops at resume using scan-path flip-flops. When this does not work, a special flip-flop in Figure 4 can be employed. The operational waveform is also shown in the figure. The basic current-latch flip-flop is known as a low-power flip-flop and extensively used in the industry designs. The flip-flop is made of low-V_{TH} devices for a fast operation and the serial

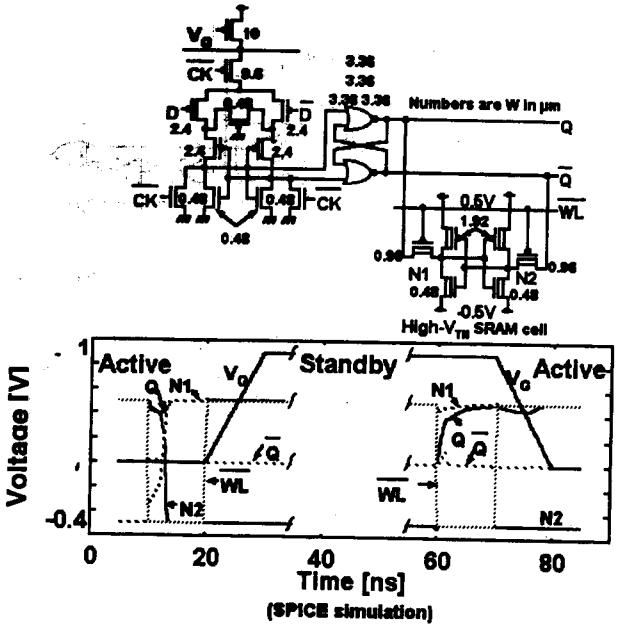

Fig.5 Speed of flip-flop with SCCMOS

cut-off MOSFET is inserted and an SRAM storage element is added to the basic flip-flop.

The SRAM storage element is made of high-V_{TH} MOSFET's (0.6V) to suppress the leakage current in a standby mode. The source voltage of the SRAM cell is set to -0.5V to obtain sufficiently strong drivability in the resume process. If the drivability is low, it can not write the stored information back into the output node of the cross-coupled NOR's. Figure 5 is a measured speed characteristics of the flip-flop. Numbers in the figure signify gate width.

In order to measure the speed of the flip-flop, a flip-flop chain with edge-trigger pulse generators is designed and the delay of the edge-trigger pulse generators is subtracted to get the delay of the flip-flop. Only in this measurement, -0.5V is applied to the p-substrate to prevent the pn-junction to be forward biased. Since the employed process is not a triple-well process, -0.5V backgate bias inevitably increases the V_{TH} of NMOS's up to 0.3V. This is why the flip-flop is slow. With a triple-well technology, the delay of the flip-flop is decreased down to three times the inverter delay with fanout of three.

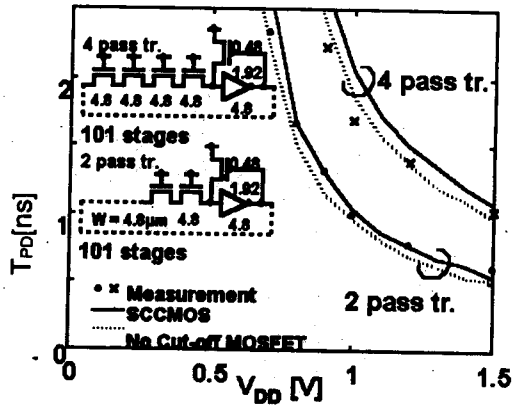

Fig.6 Speed of PTL with SCCMOS

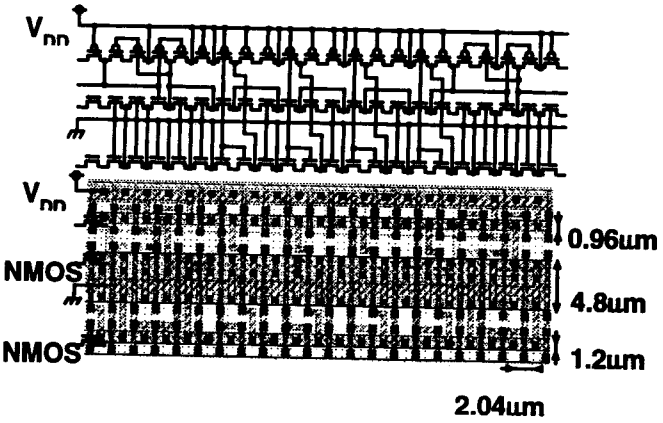

Fig.7 PTL oriented gate array

IV. PTL gate-array Design

Figure 6 shows a measured speed characteristics of pass-transistor logic (PTL) in the SCCMOS scheme. The PTL is known to provide area efficient implementation. The circuit schematic is also shown in the figure, which is single-rail implementation with small feedback PMOS for restoring the V_{TH} drop caused by the series NMOS connection. The operation with 1V V_{DD} is certified.

The PTL test circuit is implemented using a gate-array structure in Figure 7. The basic cell structure is optimized for the single-rail PTL and is simpler than the previously published basic cell structure [5]. SRAM cells can also be efficiently designed with the basic cell as in Figure 7.

V. Conclusion

The SCCMOS can operate around 0.5V supply voltage in the future. The SCCMOS can cut off leakage current below 1pA per gate without speed degradation.

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