High mobility of pentacene field-effect transistors with polyimide gate dielectric layers

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Polyimide gate dielectric layers cured at 180 °C have been employed to fabricate high-quality pentacene field-effect transistors on polyethylenenaphthalate-based films. The surface roughness (root-mean square) of gate dielectric layers characterized by atomic force microscopy is only 0.2 nm, while that of the base film is 1 nm. The transistors with pentacene channel layers deposited on 990 nm polyimide gate dielectric layers attain the on/off ratio of 10^6 and mobility of 0.3 $cm^2/V\,s$. Furthermore, by decreasing the thickness of polyimide gate dielectric layers down to 540 nm, the mobility is enhanced up to 1 $cm^2/V\,s$. © *2004 American Institute of Physics.*
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In the past decade, great progress has been made in organic field-effect transistors and many attractive applications, such as radio-frequency identification tags,[1,2] displays,[3,4] and large-area sensors[5,6] have been proposed and demonstrated. In order to fully enjoy the advantages of organic transistors, namely, mechanical flexibility and low-cost feature for large-area electronics, it is important to develop polymeric gate dielectric materials for organic transistor application. Although organic transistors with solution-processable polymer gate dielectrics have been reported and some of them show good electronic performance close to those with inorganic gate dielectric materials.[4–11] Many organic transistors are still manufactured with inorganic gate insulators.

Polyimide is one of the popular insulating materials widely used in electronics. Organic transistors with polyimide gate insulators in the previous study were not as successful[10,11] mainly due to high curing temperature (~300 °C). However, recent progress in polymer technology makes it possible to commercialize a class of polyimide precursors, which can be cross linked at temperatures as low as 180 °C. This temperature is compatible with many plastic films including polyethylenenaphthalate (PEN), which is much cheaper than polyimide and has good gas-barrier properties to protect organic semiconductors from oxidation and absorption of moisture.

In this work, we have made high-quality organic transistors on PEN films with polyimide gate dielectric layers cured at 180 °C. The transistors with pentacene channel layers deposited on 990 nm polyimide gate dielectric layers show the on/off ratio of 10^6 and mobility of 0.3 $cm^2/V\,s$. Furthermore, the mobility is enhanced up to 1 $cm^2/V\,s$ for those deposited on 540 nm polyimide gate dielectric layers. The chance of device failure occurs due to gate leakage and the initial yields are 1% for the devices with 540 nm polyimide gate dielectric layers.

The cross-sectional illustration of the device is schematically shown in Fig. 1. First, gate electrodes, consisting of 150 nm thick gold and 5 nm thick chromium adhesion layers, are evaporated through a shadow mask on 125 μm thick PEN films (Teonex Q65, Teijin Dupont)[12] in a vacuum system. Then, a high-purity polyimide precursor (KEMITITE CT4112, Kyocera Chemical) was spin coated as gate dielectric layers on the base film with gate electrode patterns. Here, we changed the revolutions of spin coating—1500, 3000, and 6000 rpm—which correspond to the thickness of 1.9 μm, 990 nm, and 540 nm, respectively, after curing. Immediately after spin coating,[13] the film is put into the clean oven (class 100), whose temperature is kept at 90 °C, and the solvent is vaporized for 10 min or more. Following the manufacturer's recommended procedure, the spin-coated film is then heated in the same oven under nitrogen environment at 180 °C for 1 h and cooled down naturally. Although the curing temperature of the present polyimide precursor is as low as 180 °C, the electronic performance is very stable and reliable, as will be shown later in detail. When the temperature is less than 100 °C, the film is taken out from the oven and loaded into the vacuum sublimation system. Then, 50 nm

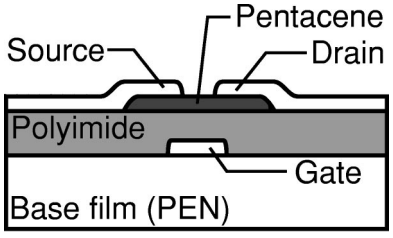

FIG. 1. (a) The cross-sectional illustration of transistors on a PEN-based film. The thickness of each layer is as follows; a PEN-based film 125 μm, gate electrode 150 nm, polyimide gate dielectric layer 990 or 540 nm, pentacene channel layer 50 nm, and source–drain electrode 60 nm.

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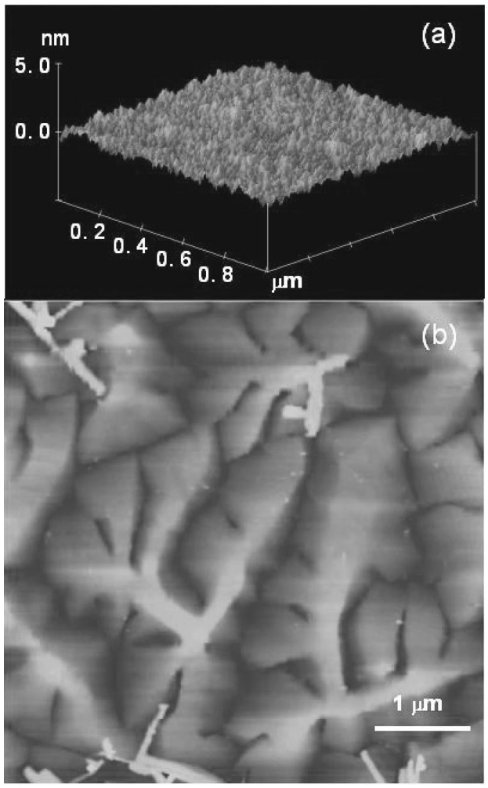

FIG. 2. (a) The surface of polyimide gate dielectric layers prepared on a PEN-based film is characterized by AFM. (b) The surface of pentacene thin films deposited on polyimide gate dielectric layers is also characterized by AFM.

thick pentacene is sublimed through a shadow mask as a channel layer at an ambient substrate temperature. Pentacene is purchased from Aldrich and used without purification. The deposition rate is about 1 nm/min and the background pressure is 3×10^{-5} Pa. Finally, 60 nm thick gold layers, which work as source–drain electrodes, are evaporated through a shadow mask. The channel length (L) and width (W) of transistors fabricated on 990 nm polyimide gate dielectric layers are 100 μm and 1.9 mm, respectively, while L and W on 540 nm polyimide are 50 μm and 1.6 mm, respectively.

The surface of the device is characterized by an atomic force microscope [(AFM) Nanoscope IIIa, Digital Instruments]. As shown in Fig. 2(a), the surface of cross-linked polyimide gate dielectric layers on a PEN-based film is very smooth in nanometer scale [root-mean-square$=0.2$ nm], which is comparable to that of the SiO_2 surface on a Si substrate (typically 0.1 nm in our measurement). Figure 2(b) shows surface of pentacene layers deposited on 990 nm polyimide gate dielectric layers. Large grains (typically a few μm) have been obtained on very smooth gate dielectric layers.

To characterize leakage currents, permittivity of thin polyimide, and yields, we have made capacitor structures by sandwiching 540 nm or other thick polyimide dielectric layers between two gold electrodes: The bottom electrode is 150 nm thick gold films deposited uniformly on a PEN-based film, while the top one is comprised of 260 μm square gold patterns. Leakage currents through polyimide dielectric layers are measured with a precision semiconductor parameter analyzer (Agilent 4156C). The typical traces are plotted in Fig. 3 as a function of electric field. The leakage current

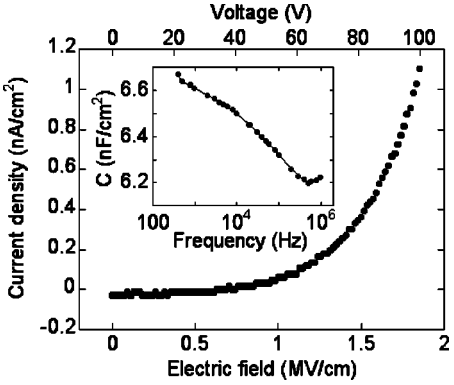

FIG. 3. Current leakage for 540 nm polyimide insulators is measured as a function of electric field. Capacitance is shown at various frequencies on the same structures as the inset.

density is less than 0.1 nA/cm^2 at 40 V and less than 1.1 nA/cm^2 at 100 V. Assuming an active transistor area of less than 0.01 cm^2, transistor gate leakage is therefore less than 10 pA at 100 V or less than 10^{-6} of the drain current. The capacitance–frequency characteristics are measured on the same structures and shown in the inset of Fig. 3.

Yields are one of the central concerns for polymeric gate dielectric layers compared with well-established inorganic insulators, such as SiO_2 or Al_2O_3. The leakage current is measured for one hundred devices for each thickness of polyimide layer, 1.9 μm, 990 nm, or 540 nm. It should be noted that the number of structures with 540 nm polyimide showing a leakage current above the noise level ($\sim$100 fA at 200 mV) is 1%, demonstrating that pinhole-free gate insulating layers have been obtained. Such high yields are crucial to utilize organic transistors for integrated circuits.[14]

The dc current–voltage characteristics of pentacene transistors are measured under an ambient environment with a semiconductor parameter analyzer and a probe station (706f, Micronics Japan). As shown in Fig. 4(a), we monitored source–drain currents (I_{DS}) of pentacene transistors deposited on 990 nm polyimide dielectric layers as a function of source–drain voltage (V_{DS}). A gate voltage (V_{GS}) is changed from 40 to -100 V with a step of -20 V. Figure 4(b) shows a transfer curve of the same device: V_{GS} is swept from 40 to -100 V with application of $V_{DS}=-100$ V.

The measured mobility of pentacene transistors on 990 nm polyimide dielectric layers is 0.3 cm^2/V s, and the on/off ratio attained was about 10^6 if the off current is defined as I_{DS} at $V_{GS}=35$ V. However, for practical use, the off current should be defined as I_{DS} at $V_{GS}=0$ V. In the latter definition, the on/off ratio is about 500. As shown in Fig. 4(c), the mobility deposited on 540 nm polyimide gate dielectric layers is strikingly enhanced up to 1 cm^2/V s and an on/off ratio also up to 900 in the latter definition. Further improvement of mobility and on/off ratio would be possible by purifying pentacene as a source material.

We would like to compare our results with the previous study. As briefly mentioned in the beginning of this letter, quite a few papers[10,11] reported on polyimide gate insulators and these devices did not show good electronic performance. This is mainly because the curing temperature of polyimides reported in the previous work is above 300 °C: The curing process is incompatible with almost all plastic films. Al-

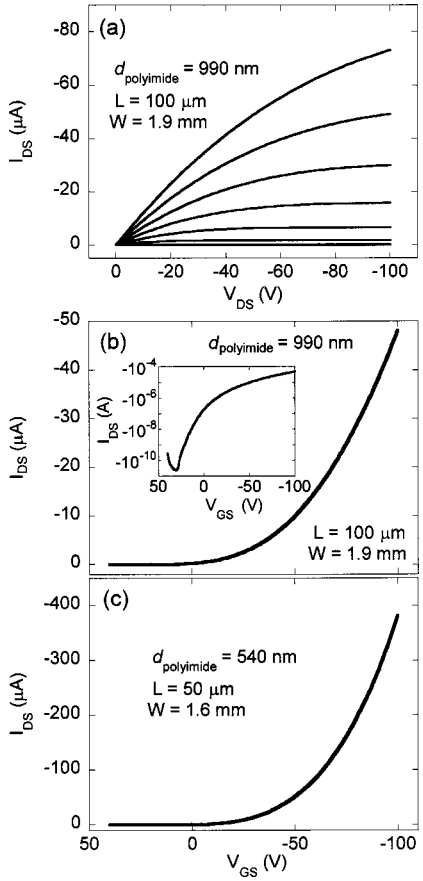

FIG. 4. dc current–voltage characteristics of a transistor ($L=100\ \mu$m and $W=1.9$ mm) on 990 nm gate dielectric layers, is shown in (a). $d_{\text{polyimide}}$ stands for the thickness of polyimide gate dielectric layers. A transfer curve of the same device is shown in (b). The transfer curve for transistor ($L=50\ \mu$m and $W=1.6$ mm) on 540 nm gate dielectric layers is in (c), which is measured at sweeping V_{GS} from 40 to -100 V with application of $V_{DS}=-100$ V.

though polyimide is good at 300 °C, the surface roughness is often induced intentionally to improve adhesion between the polyimide and other films and, therefore, such a rough surface is not favorable to obtain high mobility of organic transistors.

Note that lowering the curing temperature down to 180 °C can solve many problems, and also increase freedom to choose base films. The surface smoothness of base films and that of subsequently formed gate dielectric layers are important to obtain high-performance organic transistors with pentacene channel layers, as discussed in Ref. 15. Indeed, we have carefully used, in the present study, PEN-based films with a smooth surface in the nanometer scale (rms=1 nm). The present average surface roughness (rms =0.2 nm) of polyimide gate dielectric layers is comparable or somewhat better than that of other polymer gate insulators prepared on a Si substrate in Ref. 7, demonstrating excellent planarization effect of polyimide layers. The choice of such smooth base films and gate insulators is crucial to achieve high mobility exceeding 1 cm^2/V s.

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[12] We normally bake PEN film at 190 °C for 1 h. This prebake drastically reduces the thermal shrinkage of the base films during the curing process of polyimide gate insulators.
[13] It is important to minimize the interval between the end of spin coating and the start of baking in order to avoid aggregation of the polyimide precursor or formation of droplets of polyimide precursors, both of which degrade the uniformity of the thickness of polyimide gate dielectric layers.
[14] We have developed an approach to drill contact holes through polymeric insulators by a laser drill machine and realized integrated circuits with organic transistors: S. Iba, Y. Kato, T. Sekitani, H. Kawaguchi, T. Sakurai, and T. Someya (unpublished).
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