Stacked-chip Implementation of On-Chip Buck Converter for Power-Aware Distributed Power Supply Systems

Kohei Onizuka, Hiroshi Kawaguchi, Makoto Takamiya and Takayasu Sakurai
Institute of Industrial Science and Center for Collaborative Research
University of Tokyo, Tokyo, Japan
kohei@iis.u-tokyo.ac.jp

Abstract— **An on-chip buck converter which is implemented by stacking chips and which is suitable for on-chip distributed power supply systems is proposed and the operation is experimentally verified for the first time. The manufactured converter achieves the maximum power efficiency of 62% for an output current of 70mA with a switching frequency of 200MHz with a 2x2mm on-chip LC output filter. The active part and the passive LC output filter are implemented on separate chips fabricated in 0.35-µm CMOS and connected with metal bumps. The optimization and improvement of the power efficiency and implementation structure are also discussed.**

I. INTRODUCTION

Recently System-on-a-Chip (SoC) and System-in-a-Package (SiP) are getting focus as major integration technologies. They are often used for integrating various types of circuit blocks from processors, memories to analog circuits either. The optimum supply voltage (V_{DD}) for each circuit blocks is different each other and the difference tends to increase as the technology scales. For example, memory and analog circuits tend to prefer higher voltage compared with logic blocks. This leads to the multiple-V_{DD} implementation in low-power and high-performance systems. Moreover, supply voltage sometimes is varied in time for achieving lower power consumption, which is called dynamic voltage scaling. Supplying many different and dynamically scaling voltages from outside the package gives rise to much overhead in area and the power line integrity including IR drop and noise also becomes an issue.

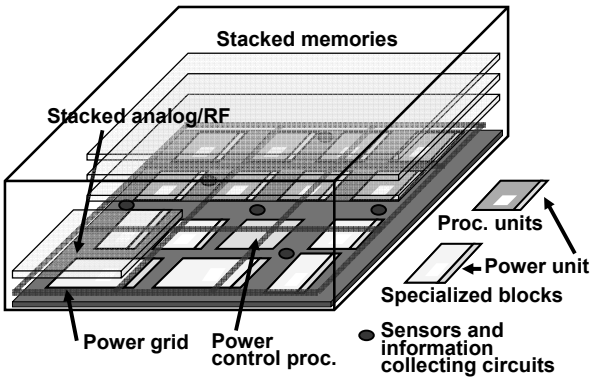

Figure 1. Concept of distributed power supply system.

The distributed on-chip power supply circuits are useful for solving these problems. Fig.1 shows the concept of the distributed power supply. High voltage is distributed by a main power grid and then it is converted to the lower voltages at the vicinity of the target blocks by distributed on-chip voltage converters. This approach reduces cost and power integrity issues.

For DC-DC converters, a linear regulator, a buck converters and a switched capacitor converter are known. A buck converter need large passive elements of inductance and capacitance (LC) for an output filter although it shows the higher power efficiency compared with a linear regulator. A switched capacitor converter also needs large capacitors and one more drawback is that the output voltage levels are limited by the ratios of prepared capacitors, and is not very suitable for low-power dynamic voltage scaling systems.

In case of the buck converter, high switching frequency is preferable for smaller L and C but the power efficiency is degraded by the dynamic power of the switching transistors in the high frequency operation. Low quality factor (Q) of air-core and on-chip inductors also degrades the power efficiency. High inductance is good for high Q but is not easy to obtain on a chip because of the area limitation and even if high magnetic permeability material is introduced on a chip, high-µ is usually lost at more than 200MHz.

A couple of integrated buck converters are reported in recent years. 80-87% efficiency was achieved at a high switching frequency of 233MHz for voltage conversion ratios of 0.75 and 0.79 with off-chip air-core inductors in 90-nm CMOS process [1]. The air-core surface-mount inductors whose quality factor is over 20 contribute to the high power efficiency. The part cost, the assembly cost and area, however, are problems and the approach is not suitable for on-chip distributed power supplies where many inductors are required nearby.

On the other hand, 50% efficiency without Zero Voltage Switching (ZVS) and 65% with Two-Stage ZVS were reported at a switching frequency of 45MHz with a voltage conversion ratio of 0.64 implemented with on-chip integrated output filter in 0.18-µm SiGe process [2]. In this implementation, the output filter is costly because it consumes large area in precious

silicon area which is manufactured by a scaled process. Moreover, in this specific implementation, metal thickness is chosen to be 10 μm, which is again costly and which is not usually available. Therefore, other approaches to implement buck converters for distributed power supply systems are to be sought through.

II. Basic Concept of Stacked-chip Implementation

In order to implement on-chip buck converters for distributed power supply systems, the following two conditions should be met. First, all elements of the converter must be integrated at least in a package. Secondly, the implementation cost must be minimized while the power efficiency is kept high.

To maximize the power efficiency, the power loss must be minimized. The major components of power loss are classified into three parts: dynamic switching loss of the switching transistors, resistive loss of the switching transistors and the resistive loss of the inductor. The total power loss is minimized under the condition that previous three parts are equal and is given by the following expressions [3].

$$P_{loss} = V_{in} I_L \sqrt[3]{24 \frac{R_0 C_0}{\tau_L} D(1-D)} \propto \sqrt[3]{\frac{R_0 C_0}{\tau_L}}, \quad (1)$$

where

$$R_0 C_0 = \left(\sqrt{D R_P C_P} + \sqrt{(1-D) R_N C_N}\right)^2, \quad (2)$$

$$\tau_L = \frac{L}{R_S}. \quad (3)$$

D ($= V_{out}/V_{in}$) is the duty cycle where V_{in} and V_{out} are the input and output voltages, which is not a design parameter but is given by the specification. I_L signifies the output current. R_P, R_N, C_P, C_N denotes effective resistance and capacitance of PMOS (high-side) and NMOS (low-side) switching transistors. L and R_S are the filter inductance and its parasitic series resistance. For planar inductors, the maximum τ_L is fixed and given by the technology. The thicker the metal layer is, the smaller the maximum τ_L is.

As seen from (1), the smaller R_0C_0 and the larger τ_L are better for higher power efficiency. R_0C_0 is shown to be roughly proportional to the product of effective resistance R_T and effective switching capacitance C_{eff} of switching transistors. Here, C_{eff} is expressed as $1.3C_G+C_J$ where C_G and C_J indicate the gate and junction capacitance per unit width. As technology scales, R_T and C_{eff} scale as $1/k^{0.7}$ and $1/k$ where k denotes scaling factor. Therefore, it is better from the power efficiency point of view to use the more advanced technology.

One may argue, however, that the maximum V_{in} can be lower with more scaled transistors. When V_{in} is higher than the maximum V_{DD} for a certain technology, the switching transistors must be cascaded to relax the voltage over-stress. If two transistors are cascaded, R_T increases by a factor of 1.2 and C_{eff} decreases by a factor of 0.4 [3]. As a result, even though we have to use cascaded structure, R_0C_0 decreases as technology scales. Thus, it can be said that it would be better to use the most scaled transistors for high conversion efficiency.

On the other hand, τ_L is mainly determined by the thickness of the metal wire. The thicker, the better. Thus the inductor is not necessarily fabricated by using the most advanced technology which is expensive.

In conclusion, it is reasonable to implement active elements and output filter on separate die whose process technologies are different. Fig.2 shows the basic concept of the stacked-chip implementation of a buck converter. The lower chip fabricated in the advanced technology contains the controller and switching transistors of buck converter and target circuits. The upper chip fabricated in classical and cheap process technology contains LC filter elements such as L's and C's. By stacking two chips face-to-face and connecting via metal bumps, a buck converter for on-chip distributed power supply systems can be fabricated in a well balanced manner over cost and power efficiency.

III. Test Chip Design

To demonstrate the feasibility of the stacked-chip buck converter, an on-chip buck converter is designed in 0.35-μm CMOS for upper and lower chips. The lower chip could be manufactured by 90nm or more advanced technology for the higher efficiency but this test chip is to show the feasibility of the stacked-chip approach. Fig.3 shows the circuit diagram of the buck converter, which is simple but parameters are optimized for the power efficiency. The area of the filter equals to the outer diameter of the filter inductor d_{out}, which is set at

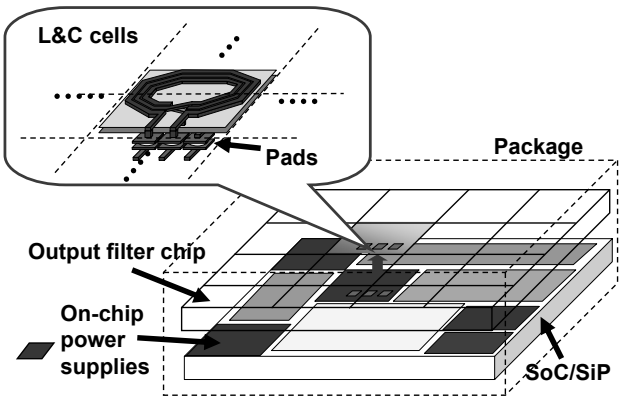

Figure 2. Basic concept of stacked-chip implementation of buck converter.

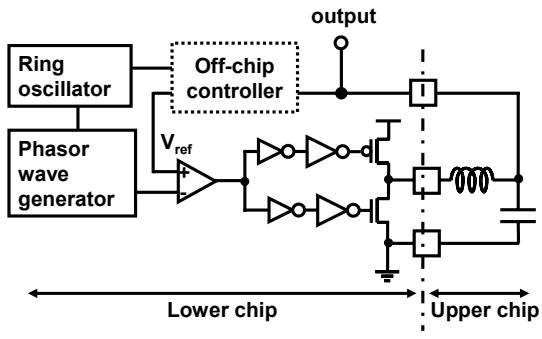

Figure 3. Circuit diagram of stacked-chip implementation of buck converter.

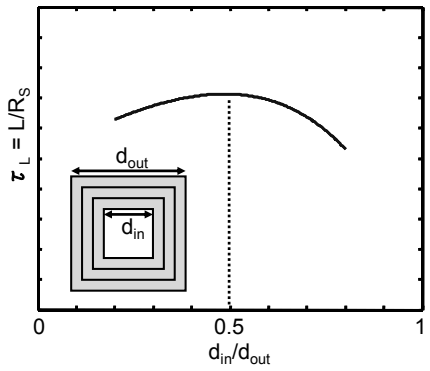

Figure 4. τ_L dependence on d_{in}/d_{out} for square inductor.

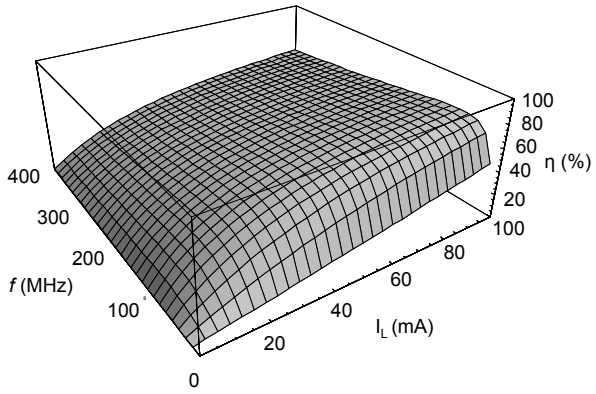

Figure 5. Power efficiency dependence on load current and switching frequency.

2x2sq.mm by assuming that 10mm-square chip can have 25 voltage domains. The inductance is estimated by the simple formula [4]. τ_L is a function of d_{in} / d_{out} as shown in Fig.4. This is because the inductance and the parasitic resistance are proportional to n^2 for fixed d_{in} / d_{out} when n indicates the number of turns. From the calculation result, d_{in} is decided to about $0.5d_{out}$. The open space at the center of the inductor is filled with a MOS capacitor for the output filter. The capacitance achieved is about 1nF. Under this condition, the power efficiency dependence on the output current and the switching frequency for V_{in}=3.3V and V_{out}=2.3V is estimated as Fig.5 using newly derived formulas. Our formula includes the effect of the output voltage drop caused by the filter inductor which is not involved in [5]. It is impossible to choose the switching frequency under 100MHz because the output voltage ripple goes up above 10%. The gate width of the high-side and the low-side transistors are designed to 1000µm and 500µm as a result of the optimization at the output current of 60mA using formulas in [5].

IV. SIMULATION AND MEASUREMENT RESULTS

The test buck converter with the stacked-chip implementation was fabricated and measured. Fig.6 shows the chip microphotograph of the output filter on the upper chip. Fig.7 and Fig.8 shows the measurement setup and its cross-sectional diagram. Here, the pad size is 200x200sq.µm for this experimental setup. Micro bumps whose diameter is 30µm and

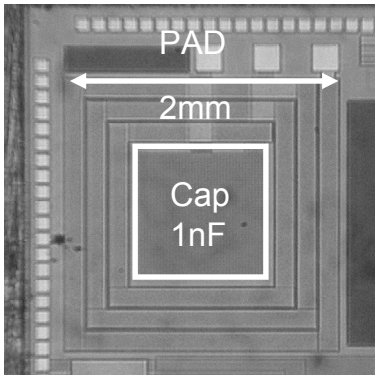

Figure 6. Chip microphotograph of output filter.

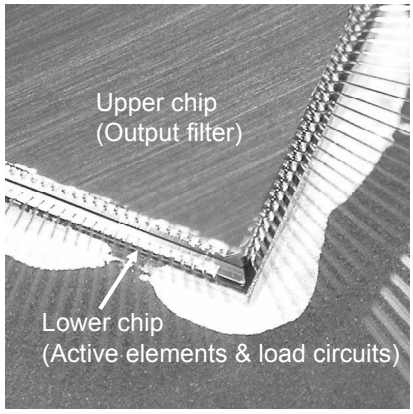

Figure 7. Measurement setup of test chip.

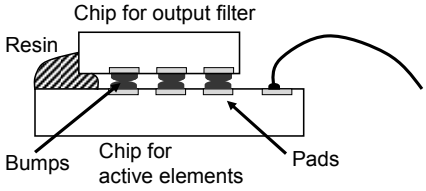

Figure 8. Cross section diagram of measurement setup.

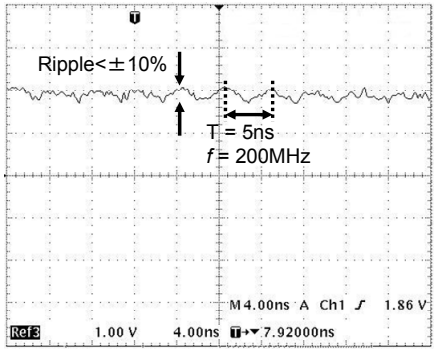

Figure 9. Output voltage waveform for V_{out}=1.86V and I_L=60mA.

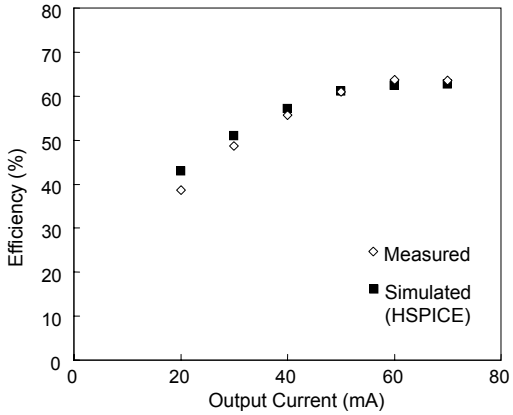

Figure 10. Simulated and measured efficiency for V_{out}=2.3V and f=200MHz.

whose resistance is as low as 14mΩ/bump have been realized in industry environments [6] and can be used instead for further smaller area. Fig.9 shows the output voltage waveform for V_{out}=1.86V and I_L=60mA. The measured voltage ripple is smaller than ±10%, which is comparable with the more expensive solution in [1]. Fig.10 shows the simulated and measured power efficiency with V_{out}=2.3V over the output current, I_L, ranging from 20 mA to 70 mA. The maximum efficiency of 62% is achieved at the output current of 70mA. The measurement result coincides well with the HSPICE simulation result with all the parasitic elements.

V. DISCUSSIONS

To gain higher efficiency, it is valuable to use inductors whose τ_L is higher than on-chip inductors. Inductor cells on plastic or glass substrates realize it by the structure shown in Fig.11. The thickness of the metal wire on those substrates is generally larger than 10μm. The capacitor cells on the upper chip in a classical technology are connected to the lower chip in an advanced technology through the through-hole vias on the substrate. By doing so, high efficiency and cost reduction are achieved. The maximum power efficiency is given as follows when the process technology and D are fixed[3].

$$\eta = \frac{1}{1+\alpha\tau_L^{-1/3}}. \quad (4)$$

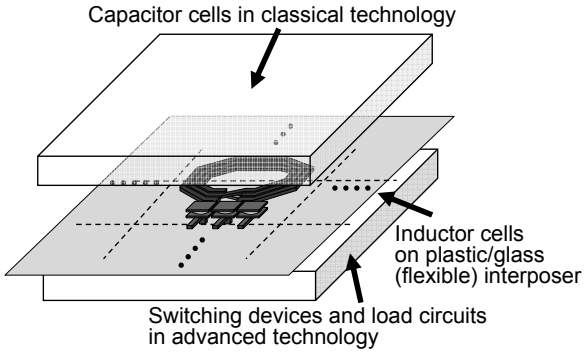

Figure 11. Another stacked-chip implementation to gain high τ_L.

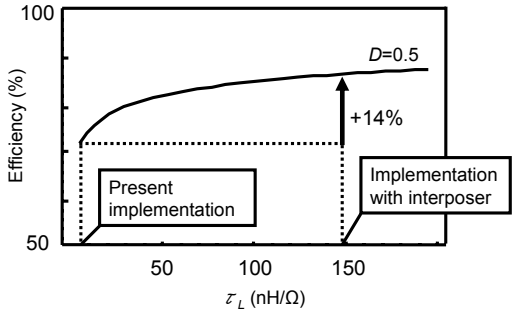

Figure 12. Efficiency dependence on τ_L.

Here, α is a constant.

Fig.12 shows the power efficiency dependence on τ_L for D=0.5 in 90-nm CMOS. τ_L for Cu wires whose thickness is 15μm is increased by x15 compared to the case of on-chip wires. As a result, the efficiency is increased by 14%.

VI. CONCLUSIONS

An on-chip buck converter with stacked-chip implementation is designed and fabricated for the first time, which is suitable for low-cost low-power distributed power supply systems. The switching frequency is optimized and chosen to be 200MHz. The power efficiency of 62% is measured for the output current of 70mA, which verifies the feasibility of this approach. If more advanced assembly technology is used, the efficiency can be further improved.

ACKNOWLEDGMENT

Valuable discussions with K. Osada from Hitachi Ltd., S. Borkar, R. Krishnamurthy, S. Hsu, T. Karnik, G. Schrom from Intel laboratories are appreciated. The chip fabrication is supported by VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Synopsys, Rohm Corporation and Toppan Printing Corporation.

REFERENCES

[1] P.Hazucha, G.Schrom, Jae-Hong Hahn, B.Bloechel, P.Hack, G.Dermer, S.Narendra, D.Gardner, T.Karnik, V.De and S.Borker, "A 233-MHz, 80%-87% Efficient Four-Phase DC-DC Converter Utilizing Air-Core Inductors on Package," IEEE JSSC, vol.40, no.4, pp.838-845, 2005.

[2] S.Svedinpour, B.Bakkaloglu and S.Kiaei, "A Multi-Stage Interleaved Synchronous Buck Converter with Integrated Output Filter in a 0.18μm SiGe Process," IEEE ISSCC, pp.356-357, 2006.

[3] G.Schrom, P.Hazucha, F.Paillet, D.S.Gardner, S.T.Moon and T.Karnik, "Optimal Design of Monolithic Integrated DC-DC Converters," IEEE ICICDT, pp.65-67, 2006.

[4] S.Mohan, Maria del Mar Hershenson, S. Boyd and T.Lee, "Simple Accurate Expressions for Planar Spriral Inductors," IEEE JSSC, vol.34, no.10, pp.1419-1424, 1999.

[5] V.Kursun, S.Narendra, V.De and E.Friedman, "Analysis of Buck Converters for On-Chip Integration With a Dual Supply Voltage Microprocessor," IEEE Trans. On VLSI Sys., vol.11, no.3, 2003.

[6] T.Ezaki, K.Kondo, H.Ozaki, N.Sasaki, H.Yonernura, M.Kitano, S.Tanaka and T.Hirayarna, "A 160Gb/s interface design configuration for multichip LSI," IEEE ISSCC, pp.140-141, 2004.