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Low-Power Control Techniques for Silicon and Organic Circuits with Array Structures

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Abstract— **In upcoming ubiquitous electronics environment, abundant electronics systems will be deployed in a sensor, car, robot, home, town, and even in a farm. The ubiquitous electronics support our comfortable and safe life, and thus require low-power feature. High-performance silicon VLSIs such as microprocessors will still be the mainstream also in the future ubiquitous electronics environment, as the modern life is supported by "the micro electronics". That is, cost reduction and power saving by downsizing will be keys. However, the ubiquitous electronics are not achieved only by the micro electronics. Another technology such as organic electronics has been recently called "macro electronics", and will complement the silicon system. The macro electronics realize a new system as a fusion of the heterogeneous technologies.**

In this paper, we introduce some low-power control techniques for silicon and organic electronics. In particular, we focus on circuits with array structures like silicon static random access memory and organic sensors.

I. Silicon Static Random Access Memory

To meet the requirements of battery-operated portable equipment, low-power techniques for a VLSI has been demanded. In particular, strategies to save power in memory are important. According to the ITRS prediction [1], 90% of the area of a system LSI will be occupied by memory in 2013. Since static random access memory (SRAM) compatible with a CMOS process apparently will play a prominent role as a memory even in a future system LSI, it is important to reduce the leakage current through the large-area SRAM, not only in the standby mode but also in the active mode. However, it is not possible merely to apply an existing leakage cutoff scheme such as the MTCMOS [2] to SRAM, because information stored in the SRAM would be lost if the power line were cut off. The MTCMOS does not address the active-leakage problem in SRAM.

Other than the leakage power, a dynamic power as another component is also important. To save the dynamic power, reducing a supply voltage (V_{DD}) is effective because the dynamic power is proportional to the square of V_{DD}. The low-voltage operation is suitable to the low-leakage design, too, because the leakage is exponentially reduced by the drain-induced barrier lowering (DIBL) as V_{DD} is lowered [3].

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A. *A Row-by-Row Variable-V_{DD} SRAM for Reducing 90% of Active Leakage Power [4]*

In dormant rows of an SRAM, V_{DD} may be kept at a low voltage that just sustains data. Even in the conventional scheme [5], a row decoder generates a wordline signal and an additional cell V_{DD}, but it has no timing constraints. When a row is activated, the cell V_{DD} is set to a high voltage (V_{DDH}). On the other hand, when a row is not accessed (in a dormant row), the cell V_{DD} is lowered to a standby voltage (V_{DDL}). This scheme localizes activation only in the accessed cells, and minimizes cell leakage. However, timing between the cell V_{DD} and wordline voltage of an accessed row is not considered in the conventional scheme. Since a pair of bitlines are precharged to V_{DDH} to read a high-supply-voltage memory cell, the cell V_{DD} is lower than the bitline voltage in a dormant row. At the beginning of readout, if the wordline voltage becomes high before raising the cell V_{DD}, the data stored in the cell might be charged from the bitlines. This situation is similar to a write operation, and thus results in the destruction of the stored data.

In Fig. 1, our proposed self-alignment row-by-row variable V_{DD} (SARRVV) scheme capable of guaranteeing the timing requirement is illustrated. The SARRVV scheme is based on a feedback mechanism that takes into account the timing constraints; there are two feedback signals in each row: V_{SVF} that controls the timing of the falling edge of a cell V_{DD}, and V_{WF} for the rising edge of a wordline.

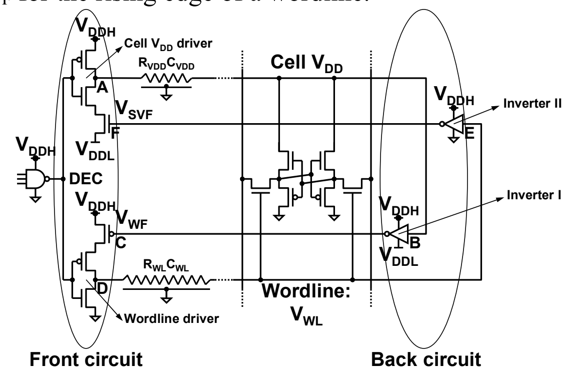

Fig. 1. Self-alignment row-by-row variable V_{DD} (SARRVV) scheme.

A 16-kb (256 columns × 64 rows) SARRVV SRAM test chip is shown in Fig. 2. Fig. 3 shows the simulated and measured leakage power of the cell array as a function of V_{DDL}. The leakage power has two components: bitline leakage and cell leakage. The SARRVV can reduce the cell leakage power by 95% at V_{DDL} of 0.3 V by exploiting the DIBL effect. The bitline leakage component is much less

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affected by V_{DDL}. However, if the channel length is expanded by only 10%, the bitline leakage is dramatically reduced since the long channel suppresses the short-channel effect. In total, a 90% reduction of the active-leakage power is achievable.

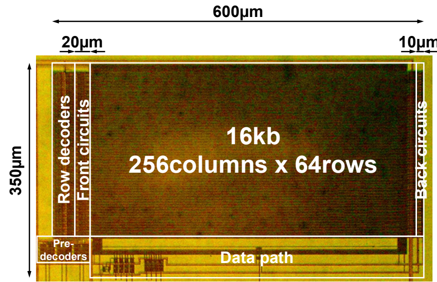

Fig. 2. SARRVV SRAM test chip in 0.15-μm FD-SOI process.

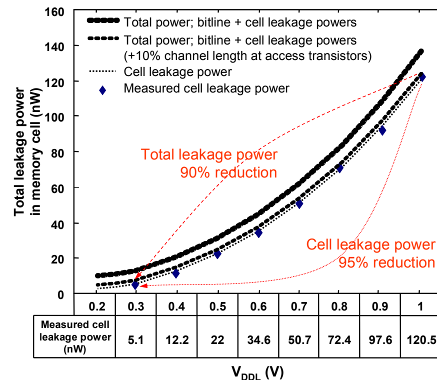

Fig. 3. Leakage power characteristics in SARRVV SRAM.

B. 0.3-V DVS SRAM [6]

In order to save a power of a system on a chip (SoC), dynamic voltage scaling (DVS) that adaptively controls an operating frequency and supply voltage (Vdd) has been implemented [7]. However, a minimum operation voltage (Vmin) is becoming higher as a fabrication technology is scaled down, since operation margins of memory cells in an embedded SRAM are degraded under both read and write conditions due to threshold-voltage (Vth) variation of MOSFETs. Vmin will be restricted by the Vth variation, which hinders wide-range power scaling of a future SoC with DVS capability.

In a typical DVS environment, a high supply voltage (Vmax) is applied externally, and then only a variable supply voltage (Va) from a DC/DC converter is provided to logic and SRAM modules in an SoC. Va is adaptively controlled, which is between Vmin and Vmax. In our proposed DVS SRAM, both Va and Vmax are provided to the SRAM; the usage of the supply voltages is different. The wordline (WL) and bitline (BL) voltages and other voltages of the memory cells are switched according to the read and write conditions in TABLE I.

Our optimum voltage control scheme improves operation margins in both read and write operations. A supply voltage of memory cells is set to Vmax in the read operation to maximize the read margin. Alternatively in a write cycle, a WL voltage is set to Vmax to obtain the write margin.

Fig. 4 illustrates a block diagram of the proposed SRAM to which the optimum voltage control scheme is applied. In the proposed SRAM, the voltage controls are done by a block-by-block basis since Vdd lines in the memory cells are along with bitlines (BLs) [8]. Vdd selectors are implemented in order to change the voltages (Vmc and WL voltage). Level shifters are introduced just after X decoders to amplify the WL voltages to Vmax in a write cycle. The output voltage of the Vdd selector for WLs (Vwl) is provided to an AND gate of GWL and Clwl, which controls local WL (LWL) voltages.

TABLE I. Voltage controls in the conventional and proposed SRAMs.

Part \ State	Conv.	Proposed		
		Read	Write	Non-access
Peripheral Vdd	Va	Va	Va	Va
BL pre-charge level	Va	Va	Va	Va
WL swing	Va	Va	Vmax	-
MC Vdd	Va	Vmax	Va	Va
MC Vbp	Va	Vmax	Vmax	Vmax

Vmax: Maximum supply voltage
Va: Variable supply voltage under DVS environment
BL: Bitline
WL: Wordline
MC: Memory cell

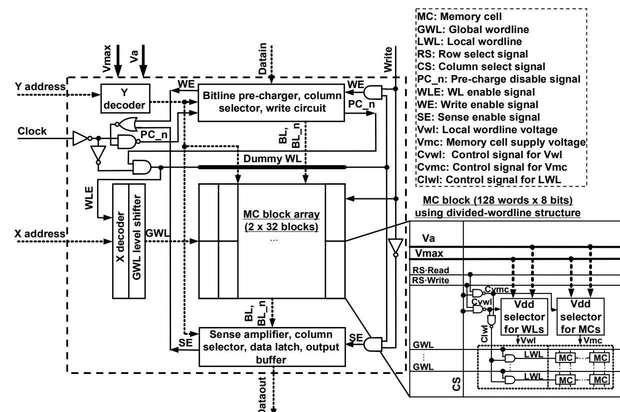

Fig. 4. Block diagram of the proposed 64-kb DVS SRAM with the optimum voltage control scheme.

A 64-kb SRAM test chip was designed and fabricated to verify the feasibility of the proposed scheme. Fig. 5 shows a micrograph of the test chip and a layout of a memory-cell block.

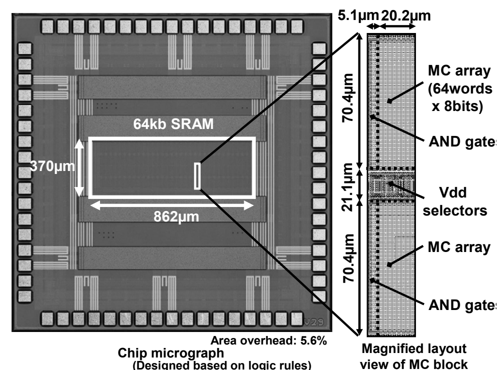

Fig. 5. Chip micrograph (90-nm node) and layout of a memory-cell block.

Fig. 6 (a) shows power dependences on an operating frequency (P-f curves). Va is implicitly adjusted according to the operating frequency. The performance penalty by applying the proposed scheme is less than 1% when Va is 1.0 V. Va must not be lowered than 0.66 V in the conventional

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scheme, which results in a higher power at a frequency of less than 300 MHz. The proposed scheme in the measurement allows the lower-voltage operation at the lower frequency, and we confirmed that the 100-MHz 0.45-V operation has an advantage of 30% power reduction compared with the conventional scheme. As indicated in Fig. 6 (b), power savings becomes higher as a memory capacity increases and process technology is scaled down. A power saving of 57% in a 90-nm 64-Mb SRAM and 74% in a 65-nm 64-Mb SRAM can be achieved at 1/6 of the maximum operating frequency.

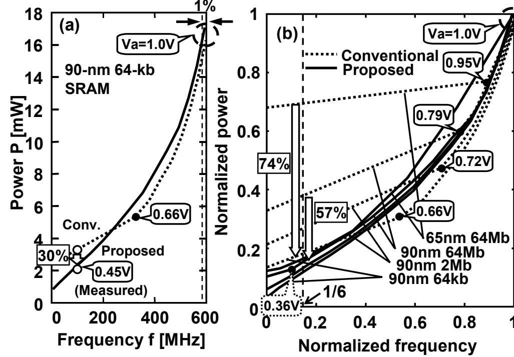

Fig. 6. P-f curves in (a) 90-nm 64-kb SRAM and (b) various capacities and process technologies.

C. 0.4-V 486-kb FD-SOI SRAM Using Inter-Die Variability Compensation Scheme [9]

To suppress inter-die variability, a body-bias control scheme has been proposed in a classical bulk process [10]. In a bulk process, however, body bias is limited to around 0.6 V due to forward junction leakage; the threshold-voltage compensation turns out in a small range. To make matter worse, a reverse bias incurs gate-induced drain lowering (GIDL) in a short-channel bulk process. Another backgate-bias control scheme in a fully-depleted silicon on insulator (FD-SOI) process adaptively changes backgate bias of memory cells in read and write operations [11], but the backgate bias itself and backgate contacts impose a cycle-time penalty and area overhead.

Fig. 7 (b) and Fig. 7 (c) are measured Id-Vgs curves of an nMOS and pMOS, respectively, when a substrate bias (Vsub) is applied from a substrate. The forward bias increases the nMOS threshold voltage (Vtn) and decreases the pMOS threshold voltage (|Vtp|), whereas the reverse bias exhibits the opposite characteristics. Note that this substrate-bias control changes threshold voltages of all nMOSes and pMOSes on the substrate; therefore, there is no area overhead in a memory cell (see Fig. 7 (d)). In a future advanced process, the substrate bias can be lowered because a buried oxide is thinning.

Fig. 8 depicts a block diagram of the proposed substrate-bias control circuit. The Vt detector outputs information on an inter-die variation as a "Detect" signal. If a die is at the FS (SF) process corner, "Detect" becomes a lower (higher) voltage than Vdd/2. Hence, to sense process variation, we should compare "Detect" with Vdd/2.

Fig. 9 is a chip micrograph of the proposed 486-kb substrate-bias SRAM. When Vsub = –4 V, we confirmed that the 486-kb SRAM works fine at 0.42V. Fig. 10 exhibits the leakage powers with and without the proposed substrate-bias control scheme. We can save the leakage power by 41%. Note that the low-voltage operation is also effective to gate leakage and negative-bias temperature instability (NBTI) in a future process.

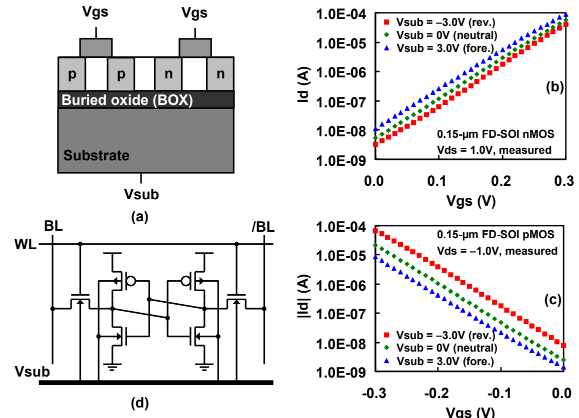

Fig. 7. FD-SOI devices: Id-Vgs characteristics of (a) nMOS, and (b) pMOS when Vsub is changed, (c) structure, and (d) memory cell.

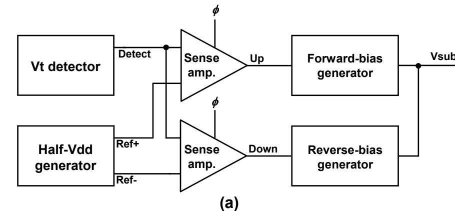

Fig. 8. Proposed body-bias control. FS (= fast nMOS and slow pMOS) and SF (=slow nMOS and fast pMOS) corner can be detected by Vt detector.

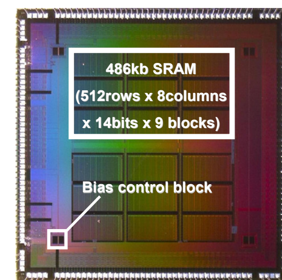

Fig. 9. A 486-kb test chip in 0.15-μm FD-SOI process.

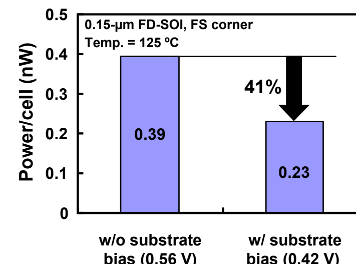

Fig. 10. Leakage powers.

D. Dependable SRAM with 7T/14T Memory Cells [12]

This SRAM can dynamically control its reliability, speed and power. In other words, a quality of information can be

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changed in terms of reliability, speed and power; we call this concept "quality of a bit (QoB)". The proposed 7T/14T memory cells are shown in Fig. 11; two pMOSes connect the internal nodes in the pair of memory cells ("N00 and N10", "N01 and N11"). Compared with the conventional 6T memory cell, the area overhead of the 7T cell is 11%, in the case of the logic design rule.

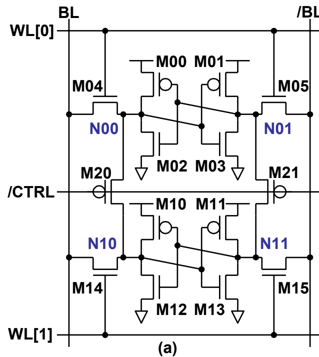

Fig. 11. Dependable 7T/14T memory cells.

Our proposed SRAM has three modes shown in TABLE II. In the normal mode, one-bit datum is stored in one memory cell as usual, which is the most area-efficient. In the high-speed mode and dependable mode, one-bit datum is stored in two memory cells by combining a pair of memory cells; but the quality of the information is different from the normal mode. The "higher-speed" or "more dependable" information can be obtained whereas the memory capacity becomes a half. The quality of the information is scalable in our proposed memory cell.

TABLE 2. Three modes in 7T/14T memory cell.

	# of MCs comprising 1 bit	# of WL drives	/CTRL
Normal	1 (7T/bit)	1	"H"
High-speed	2 (14T/bit)	2	"L"
Dependable	2 (14T/bit)	1	"L"

In particular, the dependable mode realizes the high dependability, which is a salient feature of the proposed SRAM. The additional transistors are activated, but either WL[0] or WL[1] is asserted. By doing so, a larger static noise margin (SNM) for a read operation can be obtained because a β ratio is doubled. In addition, SNMs in a cell pair are averaged out by connecting the internal nodes; this means that a small SNM is statistically saved by the other marginal cell at a high possibility. Thus, low-voltage readout can be achieved. Note that the dependable mode is not suitable to a write operation because the conductance of the access transistor is not sufficient. Instead, in the write operation, the high-speed mode should be exploited; the conductance of the access transistors is doubled, and variation is suppressed. Thereby, the write margin in the high-speed mode becomes larger than that in the dependable mode.

Fig. 12 is a micrograph of a dependable 64-kb SRAM test chip with the proposed memory cells. Fig. 13 shows the measured bit error rates (BERs) of the 7T and 14T cells. The minimum operating voltage of the 14T cell is improved by 0.12 V at the first-fail voltage, compared with the 7T cell. Fig. 14 illustrates the readout and write-in powers, at the operating frequency of 40 MHz. Note that they include power in peripheral circuits, and the memory capacity of the 14T cells is a half of the 7T cells. The respective readout and write-in powers are lowered by 43% and 48%.

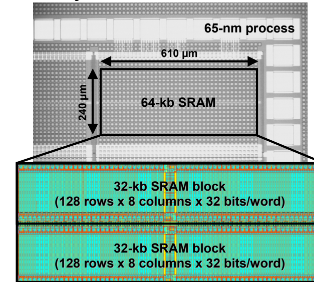

Fig. 12. Chip micrograph and layout in 65-nm CMOS process.

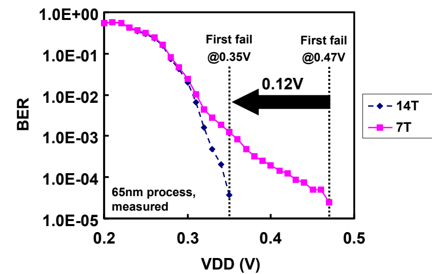

Fig. 13. Measured BERs of 7T and 14T cells at room temperature.

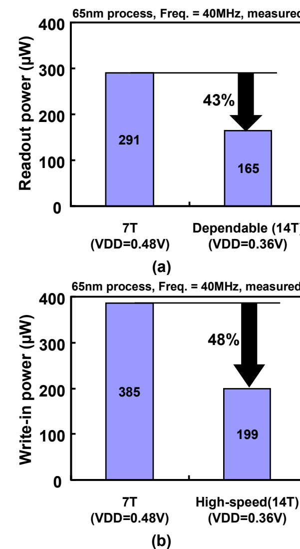

Fig. 14. (a) readout power and (b) write-in power.

E. Video Memory with Majority Logic and Data-Bit Reordering for 45% Bitline Power Reduction [13]

A two-port SRAM is suitable for real-time video processing because it can make one read and one write within a single clock cycle [14], [15]. In general, a read port has a single read bitline for area efficiency; the proposed SRAM also has the same structure as that shown in Fig. 15 (a). Two nMOS transistors for a read wordline (RWL) and a read bitline (RBL) are added to the conventional single-port 6T

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SRAM, which frees a static noise margin in a read operation [16], [17]. Therefore, a large β ratio (ratio of a driver transistor (N0 and N1) size to an access transistor (N2 and N3) size) is not required; the two nMOS driver transistors can be minimized.

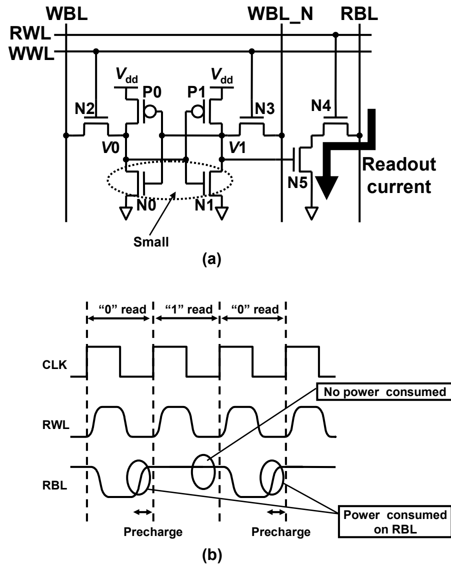

Fig. 15. 8T two-port SRAM cell: (a) schematic and (b) operation waveforms in read cycles.

Fig. 15 (b) depicts simplified operation waveforms in read cycles. Since the precharge scheme is adopted and an RBL is precharged to a supply voltage (V_{dd}) before the beginning of a clock cycle, the charge and discharge power are dissipated on the RBL when "0" (V0= "0", and V1="1") is read out. In contrast, no power is consumed on the RBL when "1" is read out, which implies that it is better for low-power operation to write as many "1" as possible.

Fig. 16 (a) shows a block diagram of the proposed SRAM with the majority logic. To maximize the number of "1"s, a majority-logic circuit counts the number of "1"s and decides if input data should be inverted in a write cycle, so that "1"s are in the majority. The inversion information ("1" denotes inversion) is stored in an additional flag bit, as depicted in Fig. 16 (b). In a read cycle, the procedure is reversed. Output data are inverted if a flag bit is true, so that the original data can be read.

In addition to the majority logic, we exploit statistical similarity in video data for further power reduction. A pixel has strong correlation with adjacent pixels, which means that more significant bits in adjacent pixels are lopsided to either "0" or "1" with higher probability. We reorder the data bits of the adjacent pixels in each digit group to improve the majority-logic function. Herein, we designate the rearrangement of the digits "data-bit reordering".

Fig. 17 shows the combination of data-bit reordering and the majority logic. In a write cycle, data comprised of m pixels (8m bits) are reordered in each digit group. If the number of "0"s in a digit group is equal to or larger than that of "1"s, the bits in the digit group are inverted. Alternatively, if the number of "0"s is smaller than that of "1"s, they are not inverted. The majority logic and data-bit reordering maximize the number of "1"s in image data and optimize the RBL power.

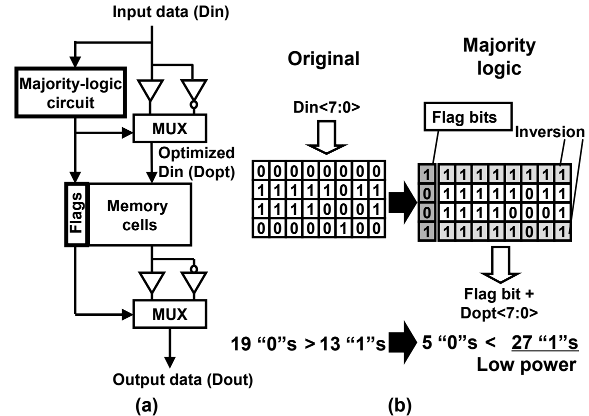

Fig. 16. Majority logic: (a) block diagram, and (b) concept of flag bit.

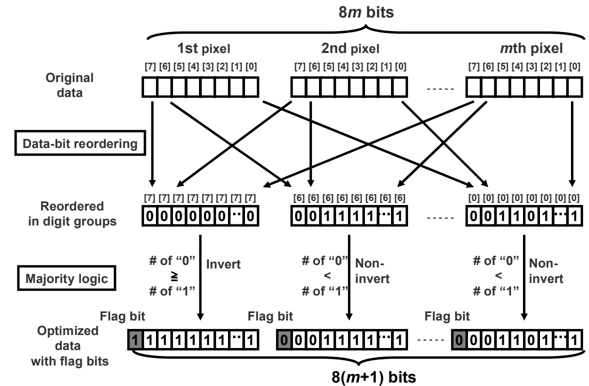

Fig. 17. Combination of data-bit reordering and majority logic.

Fig. 18 shows a chip micrograph of the proposed 68-kb SRAM. The additional area overhead derived from the flag bits, majority-logic circuit, and MUXs is 7%. The measured minimum access time is 3.3 ns at a supply voltage of 1.0 V in the proposed SRAM, whereas it is 3.2 ns in the conventional SRAM. The speed overhead is 0.1 ns.

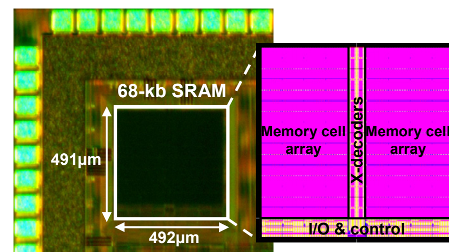

Fig. 18. A chip micrograph and its layout in 90-nm process.

Fig. 19 shows the measurement result of leakage current per memory cell. Since a "1" storage cell (V0="1" and V1="0") reduces the gate leakage at N4 and the bitline leakage from the RBL (see Fig. 15 (a)), the total leakage current in a "1" storage cell is 36% smaller than that in a "0"

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storage cell. We can maximize the number of "1"s using the majority logic. Consequently, the proposed SRAM can reduce the leakage power as well as the charge/discharge power.

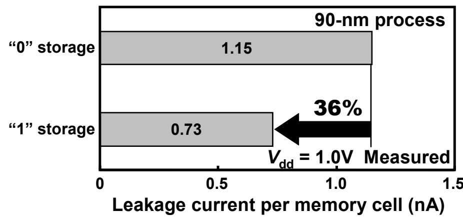

Fig. 19. Measured leakage current per memory cell.

In Fig. 20, the measured readout power in the proposed SRAM, including the power of the peripheral circuits and leakage power, is exhibited along with that of the conventional SRAM case. In a video memory, power reduction in a read operation is technically more important because readouts are made more frequently than write-ins. In the total readout power, our proposed SRAM saves 28% over the conventional SRAM.

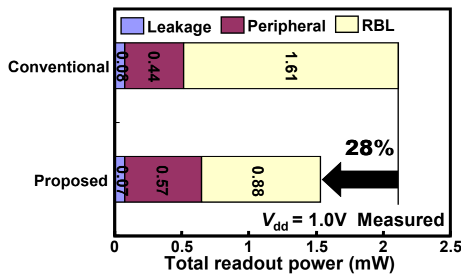

Fig. 20. Total readout power in 100-MHz operation.

II. LARGE-AREA ORGANIC SENSORS

Organic circuits are attractive attention for complementing high-performance yet expensive silicon VLSIs. By using organic field-effect transistors (OFETs), large-area circuits can be made on a plastic film. It is believed that fabrication cost of OFETs will be low possibly with roll-to-roll process and printing technologies. This means that low cost per area will be expected in future. Besides, thanks to a plastic substrate, organic circuits are mechanically flexible. These features are suitable for a large-area sensor application, which can complement small-area silicon ICs.

In large-area sensors, a passive matrix without switches is not preferable since it turns out to a large leakage. Fig. 21 shows a typical passive matrix. Leakage currents due to wordline-voltage mismatches and bitline-voltage drops flow through sensors over a whole matrix. Thus, leakage power quadratically increases as the matrix size increases.

Meanwhile, speed of an OFET is slow; however, OFET circuits have a definite advantage over silicon VLSIs as abovementioned when cost-per-area is considered. They may not compete with silicon VLSIs when cost-per-function is considered. The carrier mobility of our OFET is about 1 cm^2/Vs, which is three orders of magnitude lower than that of silicon. Therefore, hierarchical structure to speed up organic circuit is effective. The hierarchical structure also decreases circuit power that quadratically worsens as sensor area increases.

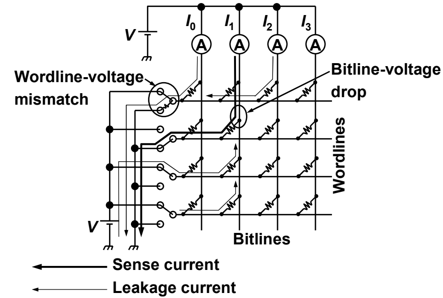

Fig. 21 Passive matrix.

A. *Electronic Artificial Skin with Active Matrix [18]*

The importance of pressure sensing is increasing in applications of an area sensor and robot for a next generation. In this work, by combining the pressure-sensor array with row decoders and column selectors, a customized OFET IC is accomplished as an electronic artificial skin (e-skin system) in Fig. 22.

Fig. 22 Photograph of e-skin system.

A cross section of a sensor cell is illustrated in Fig. 23 (a). The device structure of the OFET looks similar to an upside-down silicon MOSFET, but the channel layer is made of Pentacene. On the OFET sheet, a through-hole sheet, pressure-sensitive conductive rubber sheet, and top electrode sheet are laminated to form the sensor cells, whose circuit diagram is shown in Fig. 23 (b). Hereafter, we call the sensor cell "sencel" for short. The through-hole sheet with a round diameter of 100 μm is prepared by the conventional method of making flexible circuit boards in combination with chemical etching, mechanical drilling, and plating. It should be noted that this through-hole connects pressure-sensitive conductive rubber with an access OFET, and is totally different from a laser via that connects a gate and drain of an OFETs. The pressure-sensitive conductive rubber sheet is a 0.5-mm thick silicone rubber containing graphite particles. The upper top electrode sheet has a Copper (Cu) electrode layer suspended by Polyimide (PI). A WL and BL mean a wordline and bitline, respectively.

Fig. 24 shows the measured I_{DS} dependence on pressure.

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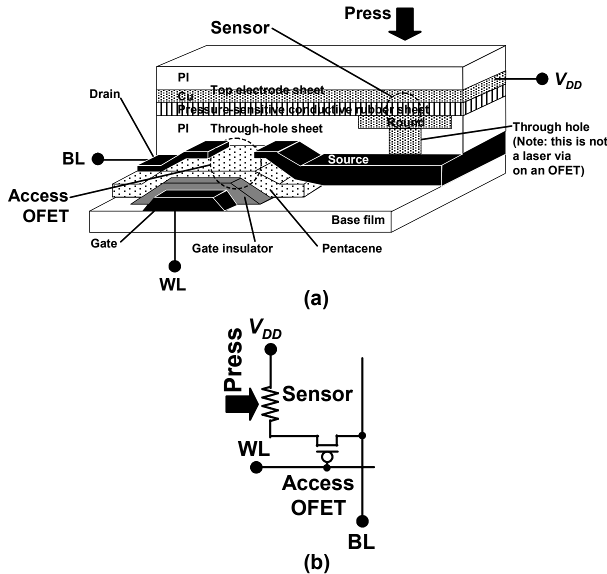
The resistance of the pressure-sensitive conducting conductive rubber rapidly changes from 10 MΩ to 1 kΩ when a certain pressure is given. The off-resistance of the pressure-sensitive conductive rubber is sufficiently larger than the drain resistance and the on-resistance is much smaller than the drain resistance. The measured dynamic power of the sencel matrix is 100 μW for the 16×16 sencels. The static power is 20 μW when 100% of the area is pressed.



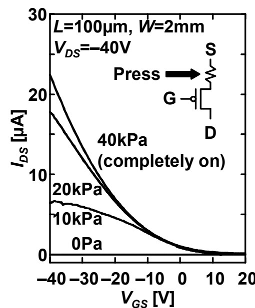


Fig. 23 (a) Cross section and (b) circuit diagram of sensor cell.

Fig. 24 Current dependence on pressure.

B. A Sheet-Type Scanner with Double-Wordline and Double-Bitline Structure [19]

In this subsection, a sheet-type canner, to which double-wordline and double-bitline structure is implemented, is described. The hierarchical structure does not only improve the speed but also saves the power of the sheet-type canner. Fig. 25 is a sheet-type scanner comprised of OFETs and organic photodiodes (OPDs). A pixel size is 1.27×1.27 mm^2, which corresponds to 20 dpi. Namely, 64×64 pixels occupy 80×80 mm^2 in area. The total thickness of the sheet-type scanner is 0.4 mm, and the total weight is 1 g. The sheet-type scanner is so thin and flexible that it can take an image of a round object such as a label on a wine bottle, which is impossible for the conventional commercial scanners. Fig. 26 (b) is the scanned image "F".

In order to improve speed and make the scanner practical, a double-wordline and double-bitline structure is implemented to the organic circuits for the first time. The structure can be applied not only to the scanner but also to other organic large-area sensor, and save power as well as circuit delay. Fig. 27 shows the circuit schematic of the proposed double-wordline and double-bitline structure in the sheet-type scanner. Only p-type OFETs are used as well as the e-skin system. A supply voltage, V_{DD}, is 40 V. An array of 64×64 pixels is divided into 8×8 blocks so that each block has 8×8 pixels. Every pixel has an OPD and pixel selector.

Fig. 25 Photograph of sheet-type scanner.

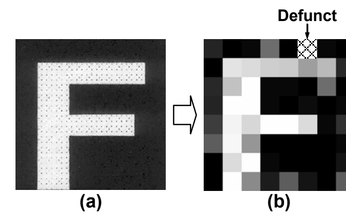


Fig. 26 (a) Original image, and (b) scanned image.

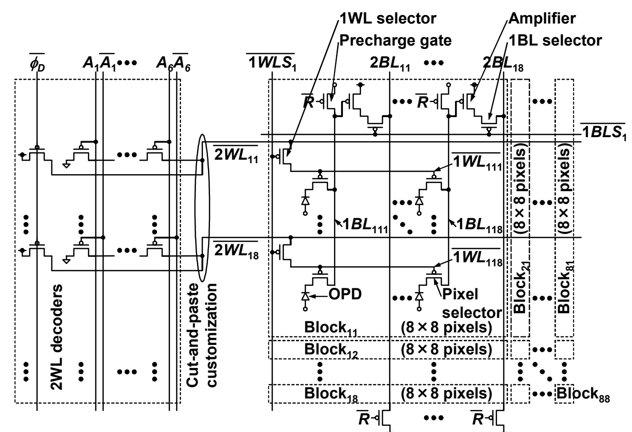


Fig. 27 Double-wordline and double-bitline structure.

A /1WL (first wordline) connects to a /2WL (second wordline) through a 1WL selector (first-wordline selector). A /1WL activates gates of aligned pixel selectors to specify a local row address. A 1WL selector selects a /1WL with /1WLS (first-wordline select signal). A 2WL decoder (second-wordline decoder) drives a /2WL.

The similar notations are used for the bitlines. A 1BL (first bitline) is a local bitline in a block. A precharge gate precharges a 1BL with /R (precharge signal), and this signal

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also pre-discharges a 2BL (second bitline) before readout operation. An amplifier amplifies a 1BL voltage. A 1BL selector (first-bitline selector) selectively transfers the amplified voltage to a 2BL with a /1BLS (first-bitline select signal).

The double-wordline structure potentially reduce dynamic power by the same factor as well as the wordline delay since the circuits operate on a block-by-block basis, where a capacitance associated with the operation is lower than the single-wordline scheme. In the conventional scheme, the total power measures 2.5 mW at the 39-ms cycle time while that in the proposed structure is 900 μW at the 7-ms cycle time, which means a 2.8-times improvement in power. If the cycle time in the proposed structure is set to 39 ms as long as the cycle time in the conventional scheme, the power reduces to 350 μW, which indicates that the proposed structure saves the power by a factor of seven.

C. Other Organic Actuators [20] [21]

The left photograph in Fig. 28 is an organic Braille sheet display for blind persons. OFET SRAM keeps display information, and drives plastic actuators. The right hand is a wireless power transmission sheet for ubiquitous electronics. 25.4×25.4 mm^2 coils detect multi objects, and supply inductive power to them. Plastic MEMS are used for large current drive.

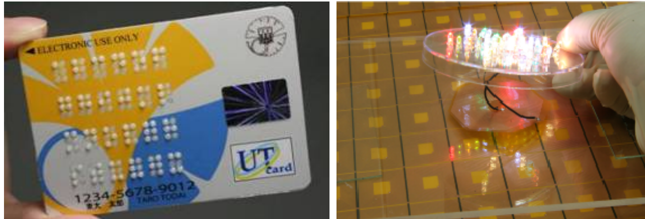

Fig. 28 Braille sheet display and wireless power transmission sheet.

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