Observation of one-fifth-of-a-clock wake-up time of power-gated circuit

Takayuki Miyazaki Tran Quang Canh Hiroshi Kawaguchi Takayasu Sakurai

Institute of Industrial Science, University of Tokyo
4-6-1 Komaba, Meguro-ku, Tokyo, 153-8505 Japan

Abstract

The wake-up time of Zigzag Super Cut-off CMOS (ZSCCMOS) is measured using a functional block for the first time. The measurement method is established and the measured wake-up time is 16% of the cycle time for a 16-bit Brent-Kung adder. The wake-up time corresponds to three 2-input NAND delay. Delay overhead and leakage current reduction of ring oscillators are also measured for the first time. Leakage reduction by a factor of 100 to 1000 is possible for dormant circuit blocks. Thus ZSCCMOS is shown to be effective as a clock-gating substitute.

I. Introduction

As technology scales, the power supply voltage, V_{DD} must be lowered. In order to maintain the circuit speed in the low V_{DD} region, the threshold voltage, V_{TH} must be lowered accordingly. The subthreshold leakage current increases exponentially as V_{TH} is lowered and the leakage power becomes dominant even in an active mode being more than 40% of the total power [1, 2].

In the era when charging-discharging power component is dominant, the clock-gating is one of the most effective ways to reduce active power consumption by stopping clock delivery to dormant circuit blocks [3]. This approach, however, does not reduce leakage power. On the other hand, techniques such as Variable-Threshold Voltage CMOS (VTCMOS) and Multithreshold-Voltage CMOS (MTCMOS) were proposed to reduce leakage current [4, 5]. These techniques suffer from long wake-up time, that is the time to recover from a standby mode to an active mode. The fastest wake-up time already reported is two clock cycles [6]. Unless the wake-up time is less than a fraction of a clock cycle, the clock-gating signal can not be used to put dormant blocks to a low leakage state. Zigzag Super Cut-off CMOS (ZSCCMOS) has been proposed as such clock-gating substitute technique [7].

Figure 1 shows the basic scheme of ZSCCMOS together with the timing chart. From the active mode to the standby mode, Phase-forceB signal is asserted and then power-gating switches, MN and MP are turned off. The Phase-forceB signal 'forces' all the internal nodes to '0' and '1'. MP is inserted for those gates whose outputs are '0', and MN is inserted for those gates whose outputs are '1' after the phase forcing. When $Stby_P$ and $Stby_NB$ are overdriven by V_{OD}, the internal nodes are kept at '0' and '1' just after the phase forcing without leakage since MP and MN are cut off deeply. The wakeup is considered to be fast because the internal node values are not changed at the recovery from a standby to an active mode. All transistors including MP and MN are made with low V_{TH} and thus ZSCCMOS works under very low voltage region. Even with the negative bias to the gates of MN and the positive bias to the gate of MP, the reliability of these power-gating switches is assured because V_{SSV} and V_{DDV} are not different from V_{SS} and V_{DD} much and the voltage stress across the gate insulator is within V_{DD} if V_{OD} is limited to one third of V_{DD}. NBTI (Negative Bias Temperature Instability) is not an issue because the gate bias to MP (PMOS) is positive rather than negative.

The wake-up time of the ZSCCMOS circuit, however, has not been measured yet using a functional circuit block. In this paper, a ZSCCMOS adder is designed and the wake-up time is measured by establishing the wake-up time measuring method. Delay overhead and leakage current reduction of ring oscillators are also measured for the first time. The ZSCCMOS concept can be applicable to other power-gating styles such as MTCMOS and BGMOS [8] and thus the measurement method established in this paper can be applicable to broader sets of circuits.

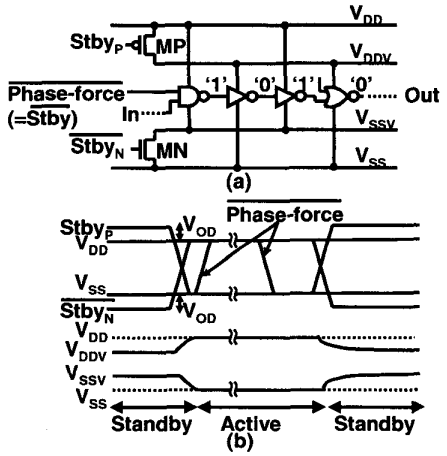


Fig. 1 (a) Basic diagram, and (b) timing chart of ZSCCMOS.

II. Delay and Leakage Current Reduction of ZSCCMOS

A. Circuit Design

Inverter ring oscillators with and without ZSCCMOS are manufactured and measured. The schematic diagram of the manufactured ring oscillator with the ZSCCMOS scheme is

shown in Fig. 2 (a). Widths of the power-gating switches are approximately 3% of the total transistor widths. The power-gating switches are overdriven to $V_{DD}+V_{OD}$ and $V_{SS}-V_{OD}$, respectively for MP and MN. V_{OD} is the overdrive voltage that determines leakage current at the standby mode. The CMOS process provides only high-V_{TH} transistors. In order to emulate low-V_{TH} devices to enable leakage current measurement, a leakage emulator in Fig. 2 (b) is employed, which effectively emulates the low-V_{TH} devices other than a speed measurement and the details of which is described in [9]. Figure 3 shows the chip micrograph of the test chip.

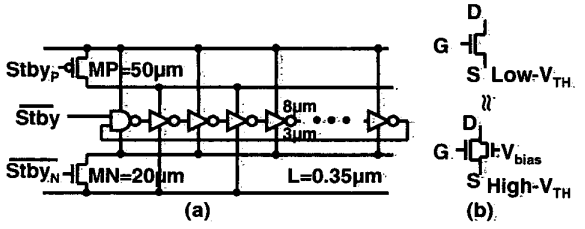


Fig. 2 (a) Schematic diagram of ZSCCMOS ring oscillator, and (b) low-V_{TH} emulator.

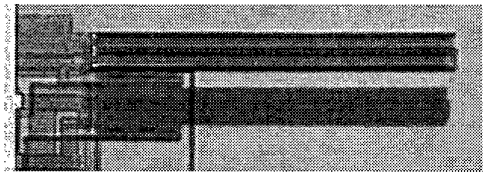


Fig. 3 Chip micrograph of inverter ring oscillators.

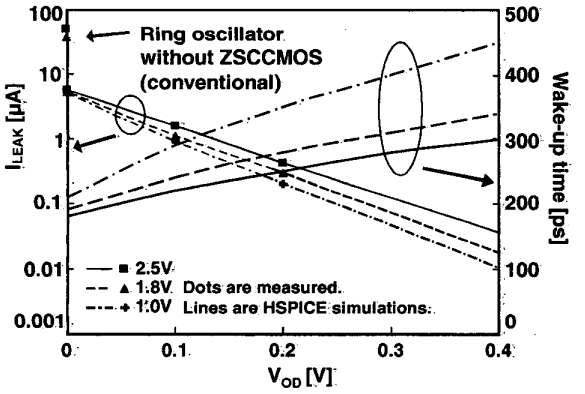


Fig. 4 Leakage current and wake-up time of ZSCCMOS ring oscillator compared with conventional one.

B. Measurement Results

Figure 4 shows the measured leakage current vs. the overdrive voltage, V_{OD}. V_{TH} is emulated to be 0.1V. It is measured that the leakage current is exponentially reduced by increasing V_{OD} while the wake-up time is not very sensitive to V_{OD}. The measurement result is in agreement with the HSPICE simulation result shown as lines in the figure. It is interesting to note that even with V_{OD} of 0V, it is possible to reduce the leakage by a factor of ten due to the off-transistor stacking effect. The leakage can be reduced by a factor of 100 to 1000

Since there is a slight trade-off between the wake-up time and the leakage current, multiple modes like shallow sleep and deep sleep can be implemented with various V_{OD} but even from the deep sleep it is possible to wake up in a clock cycle. The wake-up time from the shallow sleep is less.

Figure 5 shows the measured delays per stage of the ZSCCMOS ring oscillator and conventional ring oscillator. The delay overhead of the ZSCCMOS circuit is at most 2.9%.

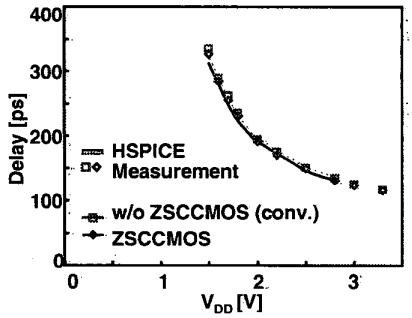


Fig. 5 Delay of ZSCCMOS and conventional ring oscillator.

III. Wake-up Time of ZSCCMOS Adder

A. Circuit Design

A 16-bit Brent-Kung adder is designed [10] using the ZSCCMOS scheme, whose core part is shown in Fig. 6. All cells are composed of 2-input NANDs. The power-gating switches shown in Fig. 6 (c) are shared among gates in the whole adder. The sizes of cut-off switches are 100µm and 50µm for MP and MN respectively, which approximately 5% of the total gate width of the circuit. The total area is 240µm x 130µm in 0.18-µm 5-metal CMOS process and the area overhead is 3.2%.

In front of the core part of the adder, there are half adders used to generate propagate and generate signals for each bit. At the end of the block, there are half adders to generate the sum. In this design, the half adders are composed of complex gates which are easy to insert power-gating switches. If multiplexers with transmission gates are used, there are sneak leakage paths [11]. Although these sneak paths can be avoided by phase forcing where input to each gate is forcibly set to '0' or '1' by changing input driving inverters to NAND or NOR, the area and delay overheads are considerable. Thus, the clocked-CMOS type multiplexer shown in Fig. 7 (a) is better be used. The power-gating switch is either NMOS or PMOS depending on input vector at standby, and the input vector is determined by the block level phase forcing. Figure 7 (b) shows the required cut-off switch when S=1. The case for S=0 is obtained by swapping input signals, A and B.

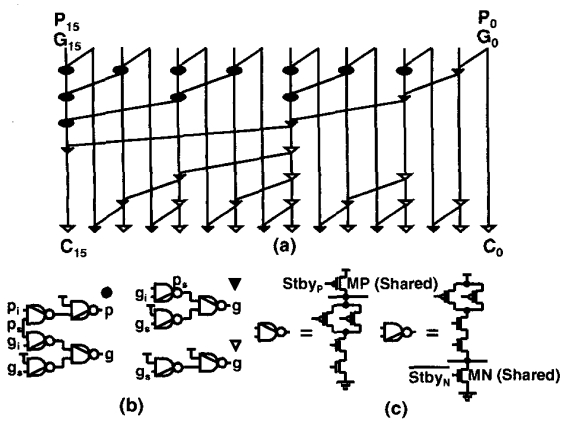
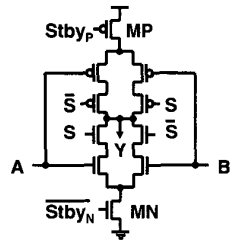


Fig. 6 Brent-Kung adder in ZSCCMOS scheme; (a) schematic, (b) gate level implementation, and (c) MOSFET representation.



S=1

A	B	MP	MN
1	1	Needed	Omit
1	0	Needed	Omit
0	1	Omit	Needed
0	0	Omit	Needed

(b)

Fig. 7 (a) Schematic of clocked-CMOS type multiplexer, and (b) table of required cut-off switch when S=1.

B. Wake-up time measurement method

The setup for wake-up time measurement is shown in Fig. 8, which is based on an on-chip latch-to-latch measurement. When CK1 is '0', the circuit is in a standby mode and the gate of the power-gating switches is over-driven to $V_{DD}+V_{OD}$ and $V_{SS}-V_{OD}$, respectively for MP and MN. When CK1 turns from '0' to '1', the circuit starts to recover from the standby mode.

The 16-bit adder start to change its internal logic values when CK1 delayed by Delay1 triggers the Phase-forceB signal so that the critical path of the adder is activated. The conventional current starved inverter chain is used as this voltage-controlled variable delay line, whose two control voltages are supplied from outside the chip. The delay dependence of the variable delay line on the two control voltages is calibrated using a voltage controlled oscillator using the same delay line fabricated elsewhere on the same chip. The same delay line is also used to measure the total delay, Delay2 by latched pass-fail measurement whose timing chart is shown in Fig. 9.

If the Phase-forceB signals to the adder are fed before the circuit fully recovers from the standby mode, that is, if Delay1 is too short, a slight extra extension of Delay2 is observed as shown in Fig. 10 (a), and V_{SSV} and V_{DDV} show a little hump due to charge sharing as shown in Fig. 10 (b). It is expected that Delay2 decreases gradually until a certain point, where it starts to increase. Delay1 that gives the corner delay of Delay2 is the wake-up time, which minimizes the wake-up procedure.

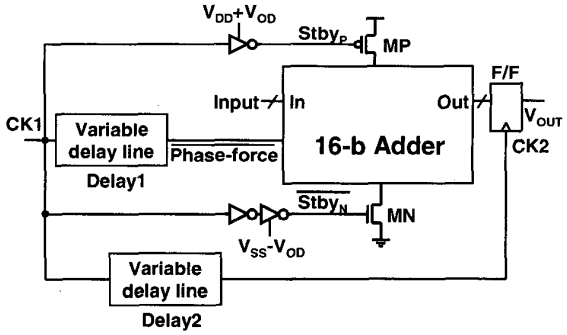


Fig. 8 Setup for wake-up time measurement.

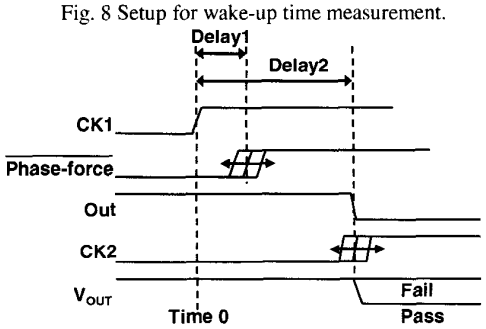


Fig. 9 Timing chart of wake-up time measurement.

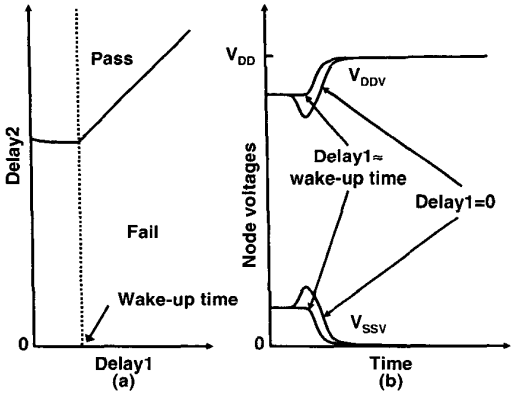


Fig. 10 (a) Expected measurement result with respect to Delay2, and (b) expected waveforms of V_{DDV} and V_{SSV}.

C. Measurement Results

The micrograph of the test chip is shown in Fig. 11.

The measurement result shows that the wake-up time of the designed adder is 0.3ns with V_{OD} of 0.2V and the delay of the adder is 1.9ns at V_{DD} of 1.5V as shown in Fig. 12 (a). The delay

of the adder corresponds to the minimum clock cycle time of the generation. Thus the wake-up time can be said 16% of a clock cycle time. Since the fastest wake-up time already reported is two clock cycles [6], this is the fastest wake-up time for a power-gated functional circuit (see TABLE I). The critical path of the adder consists of about sixteen 2-input NAND equivalent stages and the wake-up time is about three 2-input NAND delay.

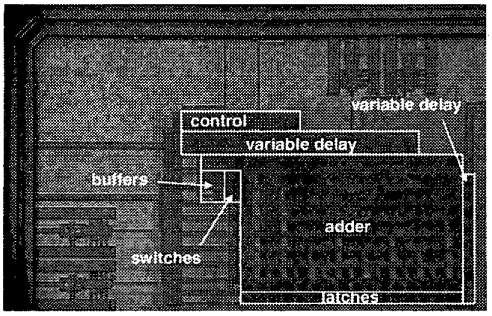


Fig. 11 Micrograph of adder with on-chip measurement circuit.

TABLE I Wake-up time comparison

Wake-up time (1)	Clock cycle time (2)	(1)/(2)
0.3ns	1.9ns	16%
J. Tschanz et al. [6]		200%

The maximum leakage reduction is reached when V_{OD} is about one third of V_{DD} above which a gate insulator will break due to the overstress to MP and MN. Assuming V_{DD} and the subthreshold swing, s factor given in the ITRS 2003, the future trend of the maximum possible leakage reduction is estimated as shown in Fig. 12 (b). More than a factor of 10^3 reduction in leakage current will be possible for 15 years. The decrease of the leakage factor around year 2010 is due to the decrease of the s factor. If the s factor is decreased, small overdrive voltage, V_{OD} can decrease the leakage effectively.

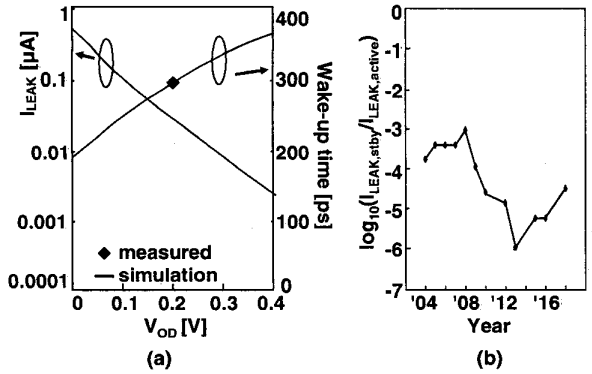


Fig. 12 (a) Leakage current and wake-up time of adder, and (b) future trend of maximum possible leakage reduction.

Conclusions

Through the ring oscillator measurement, the delay overhead of ZSCCMOS is shown about 3% and the leakage current is reduced by a factor of 100 to 1000. The wake-up time of an adder is measured to be equivalent to three 2-input NAND delay with area overhead of about 3%. It is concluded that ZSCCMOS meets the wake-up time requirement to be used as a clock-gating substitute in leakage dominant era.

Acknowledgement

The chips are fabricated through the program of VLSI Design and Education Center (VDEC), University of Tokyo in collaboration with Rohm Corporation, Toppan Printing Corporation, Hitachi Ltd. and Dai Nippon Printing Corporation. The research is supported by STARC. The authors would like to express appreciation to K. Mashiko, A. Hashiguchi, S. Furuichi, M. Nomura and H. Yamamoto for valuable discussions.

References

[1] J. Kao, S. Narendra, and A. Chandrakasan, "Subthreshold leakage modeling and reduction techniques," Proc. of Int. Conf. on Computer-Aided Design, pp. 141-148, 2002.

[2] S. Borkar, "Design challenges of technology scaling," Micro, pp. 23-29, July/Aug 1999.

[3] L. Benini and G. De Michelli, "Automatic synthesis of low power gated clock finite state machine," Trans. Computer –Aided Design, vol. 15, pp. 630-643, Jun. 1996.

[4] T. Kuroda, T. Fujita, S. Mita, T. Nagamatsu, S. Yoshida, F. Sano, M. Norishima, M. Murota, M. Kako, M. Kinugawa, M. Kakumu, T. Sakurai, "A 0.9V 150MHz 10mW 4mm^2 2-D Discrete Cosine Transform Core Processor with Variable-Threshold-Voltage Scheme," in ISSCC Dig. Tech. Papers, pp. 166-167, Feb. 1996.

[5] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solid-State Circuits, vol. 30, no. 8, pp. 8470854, Aug. 1995.

[6] J. Tschanz, S. Narendra, Y. Ye, B. Bloechel, and S. Borkar, "Dynamic sleep transistor and body bias for active leakage power control of microprocessors," IEEE Journal of Solid-State Circuits, vol. 38, no. 11, pp. 1838-1843, Nov. 2003.

[7] K. S. Min, H. Kawaguchi, and T. Sakurai, "Zigzag Super Cut-off CMOS (ZSCCMOS) Block Activation with Self-Adaptive Voltage Level Controller: An Alternative to Clock-Gating Scheme in Leakage Dominant Era," in ISSCC Dig. Tech. Papers, pp.400-401, Feb. 2003.

[8] T. Inukai, M. Takamiya, K. Nose, H. Kawaguchi, T. Hiramoto, and T. Sakurai, "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," CICC, pp. 409-412, May 2000.

[9] T. Miyazaki and T. Sakurai, "Evaluating High Leakage Effects of Low V_{TH} Circuits using High V_{TH} Devices," Int. Conf. on Microelectronic Test Structures, Mar. 24, 2004.

[10] B. P. Brent and H. T. Kung, "A Regular layout for parallel adders," Trans. on Computers, vol. 12, no. 3, Mar. 1982.

[11] B. H. Calhoun, F. A. Honore, and A. Chandrakasan, "Design Methodology for Fine-Grained Leakage Control in MTCMOS," in proc. ISLPED, pp. 104-109, Aug. 2003.